4T-Decay Sensors: A New Class of Small, Fast, Robust, and Low-Power, Temperature/Leakage Sensors

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ABSTRACT

We present a novel temperature/leakage sensor, developed for high-speed, low-power, monitoring of processors and complex VLSI chips. The innovative idea is the use of 4T SRAM cells to measure on-chip temperature and leakage.Using the dependence of leakage currents to temperature, we measure varying decay (discharge) times of the 4T cell at different temperatures. Thus, decaying 4T sensors provide a digital pulse whose frequency depends on temperature. Because of the sensors' very small size, we can easily embed them in many structures thus obtaining both redundancy and a fine-grain thermal picture of the chip. A significant advantage of our sensor design is that it is insensitive to process variations at high temperatures. It is also relatively robust to noise. We propose mechanisms to measure temperature that exploit the sensor's small size and speed to increase measurement reliability. Decaying 4T sensors also provide a measurement of the level of leakage at their sensing area, allowing us to adjust leakage-control policies. Our 4T sensors are significantly smaller, faster, more reliable, and power efficient compared to the best previously proposed designs enabling new approaches to architectural-level thermal and leakage management.

Categories and Subject Descriptors

B.7 [Integrated Circuits]: Types and Design Styles.

General Terms

Measurement, Design.

Keywords

Temperature, Architecture, Sensor, Leakage, 4T SRAM.

1. INTRODUCTION

In modern processors and systems-on-chip, power consumption is rapidly increasing as chips get larger, feature sizes smaller, and operating frequencies higher, despite the drop in operating voltages [10]. Because all this power is converted to heat, we also experience an exponential rise in heat density [10]. Recent research focused on ways to manage heat dissipation using architectural techniques [1,2,3]. These temperature–reduction techniques, greatly depend on the use of temperature sensors**,** which provide them with the necessary feedback. Having sensed the chip's thermal status, there are several ways to deal with the temperature problem but all of them have an effect on performance. The trade-off is temperature decrease for performance loss. It is clear that accurate and detailed identification of the thermal status of the processor is critical for the selection of the most appropriate thermal management scheme. In addition, recent work on temperature modeling of processors [1] has revealed significant temperature variations across the chip. This argues for a large number of inexpensive sensors (in size and power consumption) to be able to optimize and *localize* thermal management schemes.

Another significant problem in deep submicron technologies is the problem of leakage [10]. Recent work attacks the leakage problem using architectural techniques [12,13,14,15] but does not fully address leakage variation with temperature. Many of these techniques would benefit from run-time adjustments to account for leakage change.

Current proposed CMOS temperature sensors [4,5,6,7], although very succesful in accurately measuring temperature, are still too large and too power-hungry to be deployed in large numbers across a chip.

Our work addresses the need for a plethora of on-chip sensors for sophisticated temperature- and leakage-management techniques. We propose a novel thermal/leakage sensor, which can be easily integrated in any VLSI system as it provides a digital output, making it easy to interface, and is very small. The sensor is based on 4T RAM cells, exploiting the dependence of leakage currents to temperature. The novelty of our approach is to relate varying decay times of the 4T cells to different temperatures. We study the behavior of these sensors and show that they can be made very small (30 transistors occupying *one tenth* of the area of previous proposals) and low-power (100 μW to 335 μW but with a much faster response than previous proposals), while sensing a wide range of temperatures. A significant advantage of 4T-decay sensors is that they are insensitive to process variations at high temperatures and relatively robust to noise. These attributes make the 4T-decay sensors especially well suited for widespread deployment on chips. Finally, we propose sampling/measuring mechanisms that amplify decay-time differences (which become increasingly small at high temperatures) to reliably measure temperature or leakage.

Structure of this paper

The rest of this paper is organized as follows. In Section 2 we summarize related work while in Section 3 we describe the operation of our sensor and present its characteristics. Section 4

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examines the behavior of the 4T sensor in the face of process variation and noise and shows that it is affected little. We discuss how to use 4T sensors for temperature measurements in Section 5 and in Section 6 we discuss the impact of our mechanisms on architectural techniques for thermal/leakage management. Finally in Section 7, we offer our conclusions.

2. RELATED WORK

The basic concept behind temperature sensors is to have an analog circuit, whose output current or voltage changes proportionally to temperature and a mixed signal circuit, which transforms analog output to digital output, e.g., a pulse [4]. Modern temperature sensors must be based on a low-power design, for two reasons: first low power consumption means low heat dissipation and consequently the sensor monitors the chip's temperature and not its own, second small power requirements means that many sensors can be used across the chip. The restriction of using the same fabrication step, only MOS transistors, is an additional problem because of the small temperature sensitivity they exhibit in contrast to bipolar transistors. Size is another important issue, a typical temperature sensor is expected to cover an area equivalent to 10-20 simple gates (approximately 80 transistors), making it easy to include in any structure without significant area cost. Syal et al. [5] proposed differential thermal sensors based on CMOS technology, which compare the temperature from two points of the silicon surface and produce a proportional output current. The biasing circuitry of this sensor has to be thermally isolated from the sensing transistor while the output of the sensor itself has to be interfaced in order to become digital, making the overall circuit substantially larger. Also, the interface circuit is heavily depended on a mixture of negative and positive temperature coefficient resistors not easy to fabricate in a CMOS fabrication line. Szekely et al. [6] developed a family of sensors, one with current output and one with frequency output. The frequency output sensor is based on the current output circuit and a current-to-frequency converter making the total size of the sensor prohibitive in designs where many sensors must be used. Moreover, the total power dissipation of 200 μW at a frequency of 1200 KHz, is another aspect one must take under consideration. The ring-oscillator-based temperature sensors is another category of CMOS sensors [7,8]. The main problem of these sensors is their large area size and low accuracy.

3. 4T-DECAY THERMAL/LEAKAGE SENSORS

The sensor we propose exploits the relationship between leakage current and temperature. Specifically, subthreshold leakage current increases exponentially with temperature:

$$I_{Leakage} = k \cdot e^{-q \cdot Vt/(a \cdot Kb \cdot T)}$$

where q and K_B are physical constants, a and k are device parameters, and T is absolute temperature. Although T, here, refers to substrate temperature it is practically indistinguishable from ambient temperature given the intended resolution of these sensors. Leakage current also depends on Vt but in our design this effect is minimized.

Our sensor is based on charging a 4T DRAM cell, then waiting for it to decay (lose its charge because of leakage). When this happens the sensor circuit generates a pulse which recharges the cell in order to restart the process. The frequency of the pulse is inversely proportional to the decay time. Assuming that temperature changes slowly compared to the decay time of a 4T cell, the decay time is simply a function of the sensor temperature. We chose a 4T design instead of a 1T design because it can be charged much faster due to its positive feedback. The sensor circuit is shown in Figure 1.

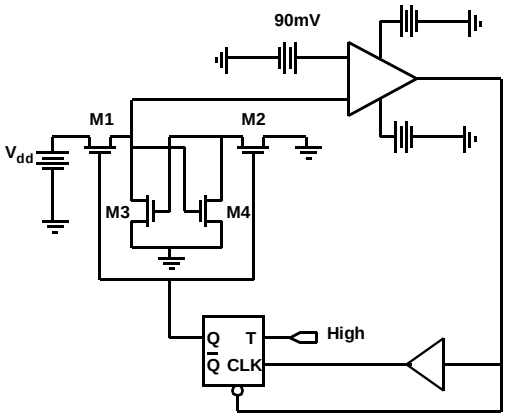

Figure 1. 4T Temperature/leakage sensor

A 4T sensor consists of four parts: a 4T cell, a comparator, a buffer and a T flip-flop. When the cell is not charged the voltage comparator output is at a logical high. In this case the T flip-flop, enabled by the comparator, toggles its output which in turn opens the "wordline" transistors and charges the cell. When the cell is charged the comparator resets the flip-flop and stops further charging of the cell; the comparator then waits for the cell's charge to leak. The output of our circuit is the output of the buffer, benefiting in this way from the buffer's high fan-out value.

A basic assumption we make is that the only leakage current that affects the cell's decay is that of the M3 transistor. This, however, is true because the W/L of the wordline transistors is substantially smaller than that of M3 making their leakage current negligible (W/L=4/1 for wordline transistors and W/L=30/5 for leakage transistors). Another assumption we make is that the threshold voltage remains fixed, which of course is not true. When temperature increases the threshold voltage drains away. However, the product of $a \cdot K_B$ is much larger than q so leakage is much more affected by temperature than the variation of the threshold voltage. In other words, our sensor is far more sensitive to temperature than to threshold voltage variations.

Besides threshold voltage there are other factors such as carrier mobility and transistor capacitance, that are affected by temperature. At low temperatures, 0^o to 30^o C, leakage effects are still very weak and the compound effect of the variation in all other factors dominates the decay behavior of the 4T cell. However, as temperature rises, leakage currents become the dominant factor and determine the overall behavior of the sensor. The cross over point for the leakage-dominated decay behavior was found to be at 30^o C in our design. We expect this point to shift to lower temperatures in future process generations which have inherently higher leakage. We consider this temperature as the operational threshold temperature for our sensor. Using the sensor above 30^o C is not a limitation since most modern VLSI chips operate at substantially higher temperatures and we are mostly interested at monitoring high temperatures.

3.1 Simulation Results

To evaluate our design we used the Orcad Pspice suite v 9.2. The transistors were based on the BSIM v 3.2 models [11]. For our design we performed a parametric transient analysis. Our

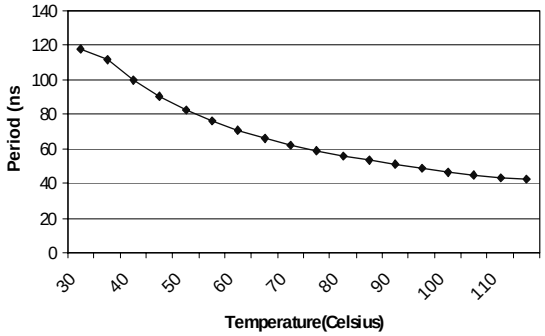

Figure 2. Sensor's Characteristic

Table 1. Power and frequency data

Sensor Analysis @ 85 Celsius	
Power	**Watts**
buffer	3.01E-09
Flip Flop	2.20E-06
Cell	1.19E-04
Comparator	1.00E-04
Total (W)	221.00E-04
Frequencies	**MHz**
Min Frequency (@ 30 Celsius)	8.46
Max Frequency (@ 125 Celsius)	23.7
Average Frequency	15

Table 2. Comparison of Temperature Sensors

Sensor	Power @ 85 Celsius	Max Frequency	Min Frequency	Size/Process
Szekeley	200 μW	1290Khz@ 0 Celsius	580 Khz @ 100 Celsius	0.02mm^2 / 1 μm
Paris [7]	—	—	—	0.5mm^2 / 1 μm
Szekeley (TFO)	20 mW	—	—	0.03mm^2 / 1 μm
Syal 1	50 μW	8MHz @ 80 Celsius	5.5MHz @ 0 Celsius	0.013mm^2 / 0.18 μm
Syal 2	140 μW	—	—	0.016mm^2 / 0.18 μm
4T Decay	221 μW	23.7MHz @ 125 Celsius	8.46MHz @ 30 Celsius	0.0017mm^2 / 0.18 μm

parameter was temperature ranging from 30^o to 115^o C, for 700 μs with a step of 0.1 ns. Figure 2 shows the simulated effect of temperature on the period of our sensor's output.

Table 1 shows a power analysis of the sensor at 85^o C along with its maximum and minimum frequency response. A comparison of our sensor with other leading proposals is given in Table 2. Sensors proposed for the 1 μm technologies —shaded in Table 2— do not directly compare with those for the 0.18 μm but we list them for completeness. Compared to previously proposed sensors, the 4T-decay sensor needs only 30 transistors, is an order of magnitude smaller, and consumes at most 221μW at 85^o C, — fairly low if we take into account its relatively high frequency response of up to 24 MHz.

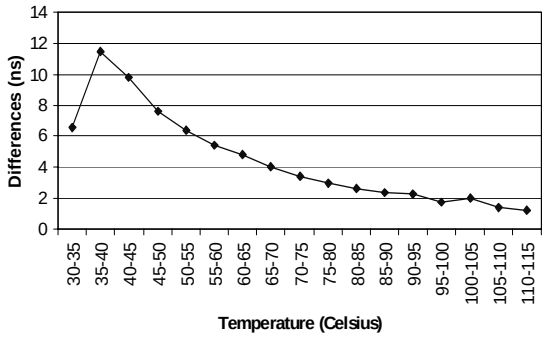

Figure 3. Successive Decay Time differences

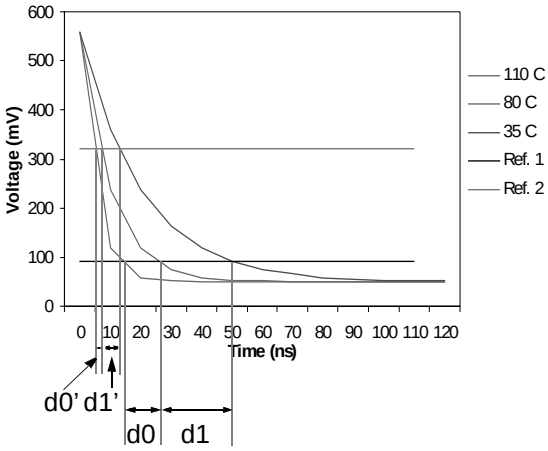

Figure 4. Discharge of the 4T cell (voltage drop of its high node) at three temperatures showing the resulting decay times for two different comparator reference voltages

3.2 Sensor Resolution

Our approach is based on measuring the decay time of the 4T cell at different temperatures. In our case decay time is the time it takes the high node of the cell to drop below a reference voltage. Decay times are not only shorter at higher temperatures but they converge asymptotically to the same value (as it is evident in Figure 2). Thus, the difference between successive decay times becomes increasingly small as we move to higher temperatures. Figure 4 plots decay-time differences for every 5^o C. The initial anomaly in the plot (the increase in difference from about 6ns to 11ns) is due to other effects that dominate in this temperature range besides leakage as we discussed in Section 3.Although, in Section 5 we show how to amplify decay-time differences for reliable measurements, here we discuss factors that directly affect such differences.

A deciding factor is the comparator's reference voltage. The lower the reference voltage, the greater the differences we observe in decay times. The reason for this is illustrated in Figure 5 which shows the discharge of the 4T cell at various temperatures. As we move the reference voltage lower the distance between the discharge curves increases, spreading out the decay times at various temperatures (e.g., decay times d0 and d1 for Ref. 1 in Figure 4). The opposite happens when we move the reference voltage higher: decay times are squeezed together (e.g., d0' and d1' in Figure 4), making it difficult to distinguish them at high

temperatures.The minimum usable reference voltage depends on the comparator used —in our study we were limited by the available library comparators— but also from the fact that the high node never reaches ground but floats closely above it. Going below this minimum results in infinite decay times at all temperatures.

A different factor affecting decay-time differences is the transistors' W/L ratios. Modifying these ratios changes the shape of the discharge curves. We note that this opens a wide range of possible designs and optimizations, but we do not expand on these further in this paper.

4. PROCESS VARIATION, SELF CALIBRATION, AND NOISE

An important feature in our sensor design, not found in competing sensors, is that its output is not affected by process variation, except by negligible amounts at low temperatures.

The variability manifested in L_{drawn}, T_{ox} and N_{sub}, can drastically affect the leakage current. According to Srivastava et al. [9] the effect of the variation in gate length has a severe effect on leakage current, while the variation in channel dose has little impact. However, in our circuit there is a physical self-calibration: as L_{drawn} and T_{ox} change, affecting the leakage current, the cell's capacity also changes keeping a balance in the period needed for the cell to decay. This counterbalancing effect is especially effective at working temperatures. For temperatures higher than 40^o C, no calibration needs to be done as the dependence on the process variation results in negligible variation of the decay time (less than 2% impact). Figure 5 and Figure 6 plot the sensor's characteristics and the relative decay-time error for L_{drawn} and T_{ox} variations respectively. In both figures the top three overlapping curves are the decay-time characteristics for no-process-variation, for 10%, and 20% process variation. These curves overlap for almost all of the temperature range. The bottom two curves in each figure show the relative difference in decay times for the 10% and 20% process variation compared to the no-process-variation decay-times.

For low temperatures, process variation has a visible effect (Figure 5 and Figure 6) although still very small (at most 2% difference in decay times). If, however, the utmost accuracy is needed for these temperatures one must have a way to calibrate the sensors. We tackle this problem by making the assumption that a sensor whose output is in a range near the mean of the output of other sensors, works correctly. Since 4T sensors are cheap (small and low-power) we can afford to use them redundantly and this makes this approach feasible. Initial calibration can be performed assuming homogeneous chip temperature. Sensors whose frequency deviates significantly from the mean can be disabled. In more complex sensor sampling mechanisms, such as those discussed in the next section, the frequency of a faulty sensor can be adjusted by other means to match that of other sensors. Of course there is a trade-off between redundancy and power efficiency, using more sensors we can better identify faulty sensors but we add on the overall power consumption. Because the differences in decay times due to process variation are exceedingly small even at low temperatures we do not consider sensor calibration (for process variation) necessary in our design.

4.1 Noise

Temperature sensors are in general sensitive to noise on power and ground lines [6]. The 4T sensor is also susceptible to such noise and the quantity that is most affected is the charge in the 4T cell. However, small changes in the initial charge do not result in

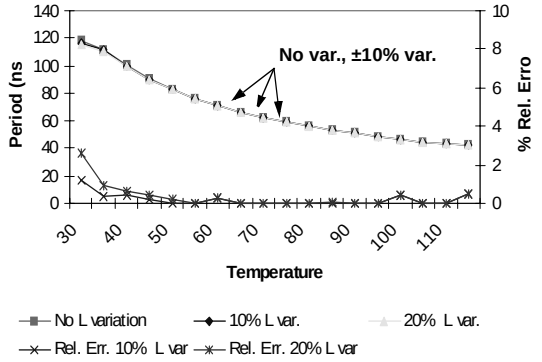

Figure 5. Period variation with ±10% L_{drawn} Process Variation

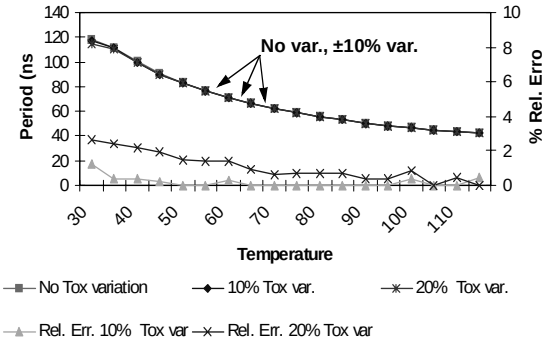

Figure 6. Period variation with ±10% T_{ox} Process Variation

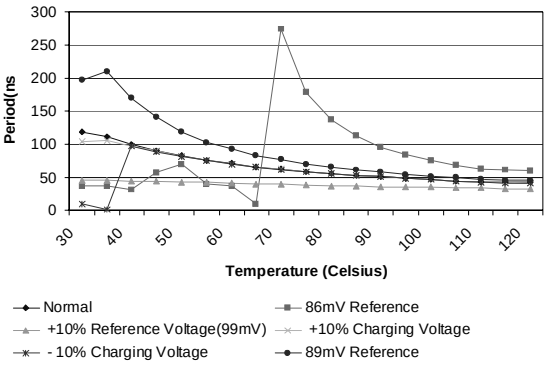

Figure 7. Period Variation with Noise in Power Lines

drastic changes in decay time. As it is depicted in Figure 7 even a ±10% variation in charge voltages results in less than 2% variation in decay times for temperatures greater than 40^o C —a more-than-acceptable error.

More seriously, 4T sensors are sensitive to noise on the comparator's reference voltage, as it can easily be seen in Figure 7 (reference voltage variations). Fortunately, the design of the sensor results in a safe behavior. Noise that drives the reference voltage up results in the sensor reporting shorter decay times which translates into higher-than-actual temperature readings. In Figure 7, increasing the reference voltage by 10% (from 90mV to 99mV) consistently yields decay-times below the minimum decay-time of the base case. We consider this safe in the sense that temperature-control mechanisms might be unnecessarily engaged but no

damage to the chip will occur. Noise that drives the reference voltage down, however, is dangerous since the sensor could then report lower-than-actual temperatures. This could potentially result in chip damage if safeguards are bypassed due to false readings. This is avoided in our design by using a reference voltage very close to the minimum possible as we discussed in Section 3.2. In our case, we use 90mV whereas the comparator stops working below 86mV. Thus, if the sensor yields unexpectedly long decay times we can safely ignore them as transient faults. For reference voltage variations between 89mV and 86mV one can easily detect a fault since decay times suddenly become substantially larger than those without any variation, implying instantaneous temperature drops of tens of degrees.

Noise on the reference voltage line has a small time window to affect the correct operation of the sensor: it is dangerous only when the cell's voltage approaches the reference voltage. Thus, even in noisy environments we expect transient faults not to be common.

5. TEMPERATURE MEASUREMENT

The first step in measuring temperature using 4T sensors is to measure decay times with enough resolution to be able to ascertain whether they increase, or decrease and by how much. As we discussed in Section 3.2, decay-time differences become increasingly difficult to distinguish at higher temperatures: above 100^o C they are less than 2 ns per 5^o C (Figure 4). In this section we propose mechanisms that not only enhance resolution of the sensors at high temperatures but also increase their reliability.

The key observation is that we can amplify decay-time differences before we measure them. This is feasible because of the 4T sensor's very high speed (compared to other sensors). We amplify decay-time differences by measuring the *aggregate* decay time of multiple consecutive charge-decay cycles (temperature practically remains constant during many charge-decay cycles). Aggregating multiple decay times in a single measurement also increases reliability since the effect of transient phenomena on decay time is averaged-out.

The sampling mechanism we propose is shown in Figure 8. The 4T output pulse feeds an asynchronous 5-bit counter which counts a small number of charge-decay cycles. The counter is set (externally) to some value and counts down to zero. At that point it produces a signal and resets itself to its initial state. As an example, in Figure 8, the counter counts 20 charge-decay cycles. A larger counter (16-bit cycle counter in Figure 8) counts the aggregate decay time in clock cycles. When the decay counter signals the end of the 20 charge-decay cycles, the value of the clock-cycle counter is copied to a measurement register and the clock-cycle counter is reset to zero. Measuring aggregate decay time allows us to distinguish arbitrary small differences. For example, multiplying decay times by a factor of 20, gives us a difference of 23ns for the decay times at 110^o and 115^o C, whereas before that difference was close to 1 ns. With a clock of 2 GHz or more, common today in many processors, amplified differences correspond to many tens of cycles.

We can further amplify decay-time differences increasing the number of charge-decay cycles until we can distinguish them at a desired *temperature resolution*. Practically, this means that we can go as low as 1 degree resolution if we go to large enough numbers of charge-decay cycles but at the same time we increase the error in the measurements. Despite the increased latency for a reading —the response time in Figure 8 grew twenty-fold to 2233 ns— the sampling mechanism is still quite fast for architectural-level thermal management —temperature increases very slowly [1].

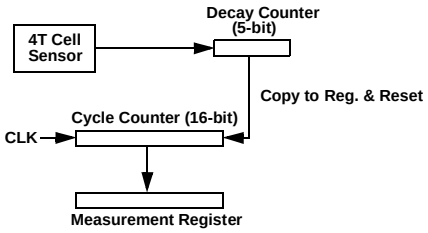

Figure 8. Decay-time measuring mechanism for multiple charge-decay cycles

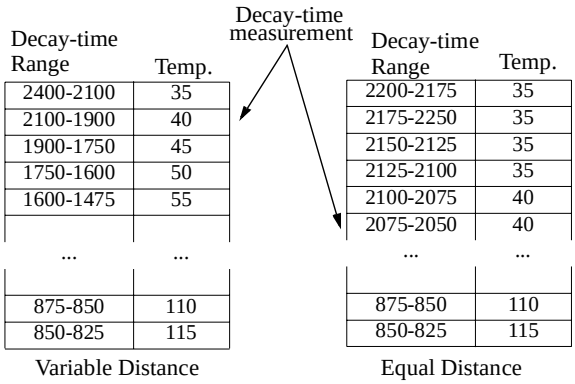

Figure 9. Mapping tables with variable-distance and equidistant decay-time ranges. Decay-time ranges are approximate and scaled for 20 charge-decay cycles.

The combination of a fast sensor and slow-rising temperatures also allows us to keep the sensor from operating constantly. Skadron et al. [1] take temperature measurements every 10K 1-ns cycles; similarly, we can activate the sensor periodically reducing its average power consumption. Two advantages in this case are: i) that the sensor operates for so little (and so fast) that it does not thermally affect its environment to the slightest, and ii) its exposure to noise is further reduced making it less prone to faults. Furthermore, periodic operation of the sensors gives us the opportunity to *time-share* the sampling mechanism among multiple sensors, reducing the overall cost of monitoring. Thus, we can maintain the significant advantages of speed, size and power consumption, to easily embed a plethora of sensors in larger structures (e.g., in a cache), while sharing a single sampling mechanism.

5.1 Translating Decay Time into Temperature

The second step in measuring temperature is to translate a reliable decay-time reading into a temperature reading. This is done by indexing a mapping table which relates decay-time ranges to temperatures. Such a table, for example, can yield a temperature of 40^o C for decay-times ranging from 2100 to 1900 ns. Finer temperature resolution can be achieved as discussed previously but because decay-time ranges get smaller with higher resolution, measurement errors increase. To avoid a complex decoder the mapping table can be constructed to list temperatures corresponding to equidistant decay-time ranges as it is shown in Figure 9.

The mapping table is set-up either at run-time using an auxiliary sensor of a different design as guide or at initialization time by precomputed data. In the former case, the table starts out with default values and it is modified as we observe new temperatures

(and new decay-times). In the latter case, run-time adjustments are also possible, again using an auxiliary sensor.

By keeping track of the previous reading, the current reading, and the time between them we can also compute the rate of temperature change. Finally, the translation of decay-times to leakage is equally straightforward, if instead of temperatures we list leakage values in the mapping table.

6. IMPACT ON ARCHITECTURAL TECHNIQUES

The 4T-decay sensor compares favorably in many respects with previous proposals, but we believe that its main advantage is that it is cheap; cheap in terms of size, power consumption, and requirements for its use.This has a significant impact on architectural techniques that now can have numerous sensors at their disposal in order to make more informed decisions. Three characteristics of the 4T sensor significantly affect temperature-control techniques:

- Speed: The very fast response of the 4T sensors (even when we measure aggregate decay-times) allows us to take fast and numerous measurements, when we need them. For example, at low temperatures, we can take measurements infrequently but as things heat up we can increase the measurement rate to keep a tight control on heat build-up.
- Size: the small size of the 4T allows us to embed it in or close to many structures that we wish to monitor independently. Thus, we can have sensors inside other structures, for example function units, to control them independently, or we can have multiple sensors on the border of a large memory structure so we can identify how it is heated up spatially.
- Power Consumption: the low power consumption of the 4T sensor allows us to use it freely without exceeding power budgets or thermally affecting its environment.

4T sensors can also provide leakage measurements to adjust leakage-saving techniques to ever-changing leakage conditions. In the Cache Decay [14] and related work [12,15] a simplifying assumption was that leakage currents were constant. The trade-off of power-savings for performance-loss was only balanced for a specific leakage rate. In reality, this balance changes in time as heat rises. More interestingly, the balance changes also in space as a large cache, for example, is not heated homogeneously, but rather irregularly. 4T sensors can help in two ways: first they can help set a decay interval that maximizes leakage-power savings for a specific temperature; second, they can help identify parts of the cache that heat up and need leakage-control, as opposed to cool parts of the cache that do not leak much and do not benefit from leakage-control. The same approach can be invaluable in techniques that control leakage in the processor core such as Transmeta's Long-Run2 technology [16].

7. CONCLUSIONS

We describe a novel temperature/leakage sensor based on the decay of 4T SRAM cells. The main idea is to charge a 4T SRAM cell and then wait for it to decay (lose this charge) due to leakage currents. Measuring the decay time of the cell we obtain a measure for temperature, since leakage depends on temperature. The most important advantage of this new sensor is that it is *cheap* (in size and power consumption), especially if sampling mechanisms are shared among many sensors.

A welcomed characteristic of the sensor is that the effect of process variation on its response is negligible. This is because the sensor is self-calibrating: process variations that affect leakage currents also affect the capacity of the cell in a counterbalancing manner. Thus, no calibration is needed for working temperatures, further enhancing its ease-of-use. As for noise, we show that the sensor can err on the safe side and we can easily detect dangerous faulty readings and ignore them.

The availability of fast, small and robust thermal sensors enables a new level of accuracy and functionality in architectural techniques to control temperature and leakage. Numerous 4T-decay sensors can provide a fine-grained picture of the monitored circuit's thermal/leakage status, both in time, but more importantly, in *space*. Having accurate feedback on the thermal status of the chip is crucial to make the best decision on which the counter-measure to apply to deal with a thermal emergency with minimal impact on performance. Moreover, significantly more efficient leakage-management techniques can be developed with 4T-decay sensor feedback.

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