Today (2/20) [537]

Virtual Memory

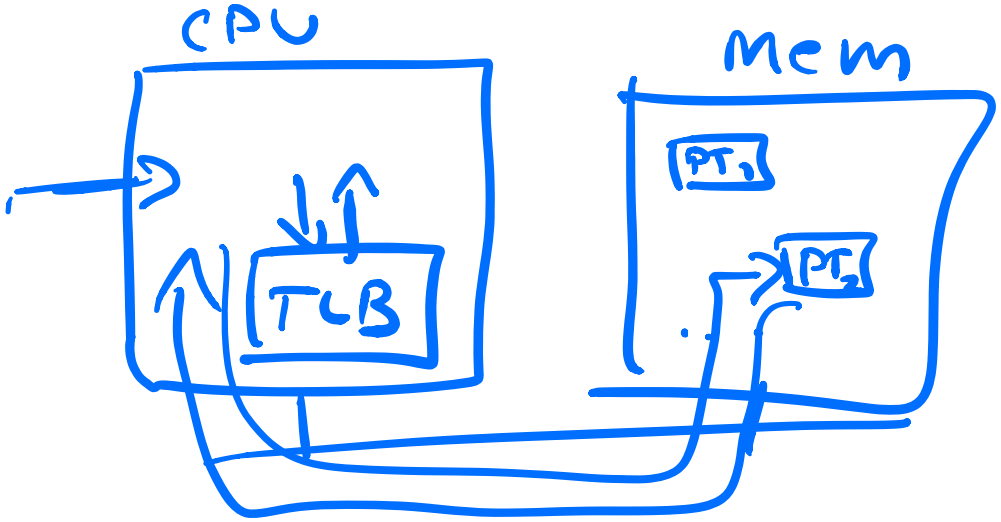
=> Page Tables — array-based called "linear" P.T.

-> Problems

-> Paging: too slow

=> extra memory ref => Page Table

solution: TLB "address translation cache"

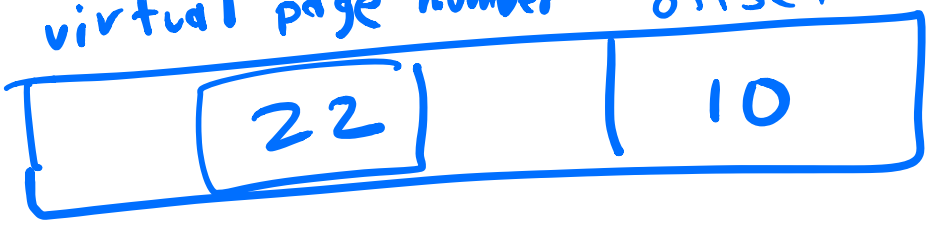


=> Problem #2: Page Tables too big

=> Problem #3:
what if amt mem. accessed by prog > amt. of phys mem?
=> use "disk":
[slower, larger Storage medium]

Problem #2: Page Tables are too (Linear) big

32-bit virt. addr space:



Page size: 1 KB

— ... is the page

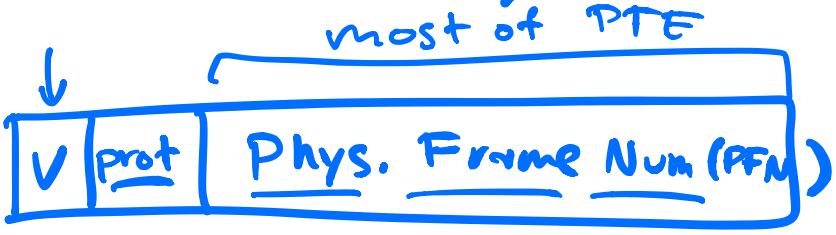
=> how big is the PT table?

array: [one entry per VPN]

pages: 2^{22} ~ 4M

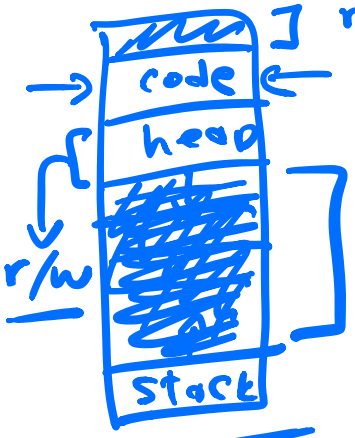
=> about 4 million entries

Page Table Entry (PTE)



valid or not

V.A.S.



not valid

read/execute only (shared)

not valid => goal: not waste phys mem.

PTE: [4 bytes]

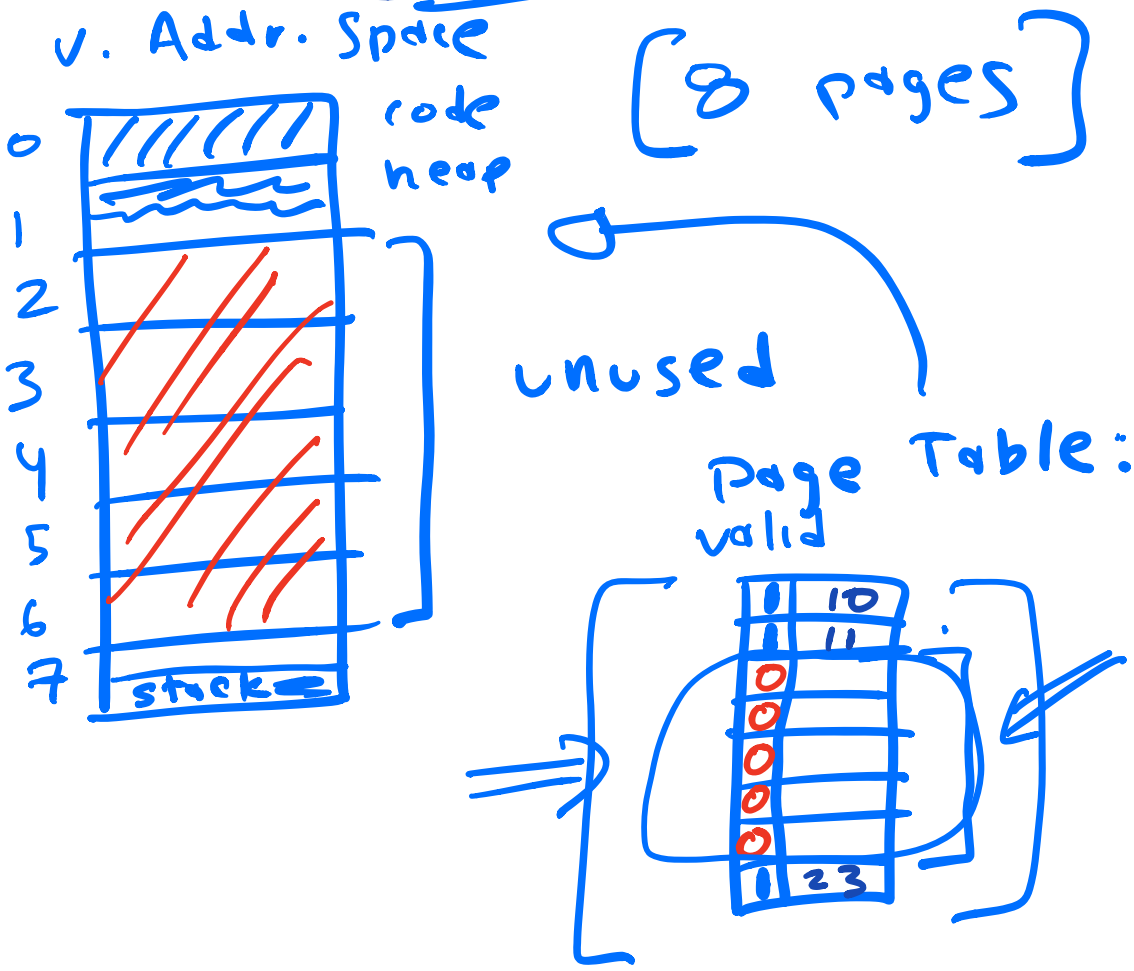
Size (Page Table): ~4M * 4b

⇒ ~16 MB

one Page Table / Process:

assume 100 processes

⇒ 1600 MB of PTs!!)



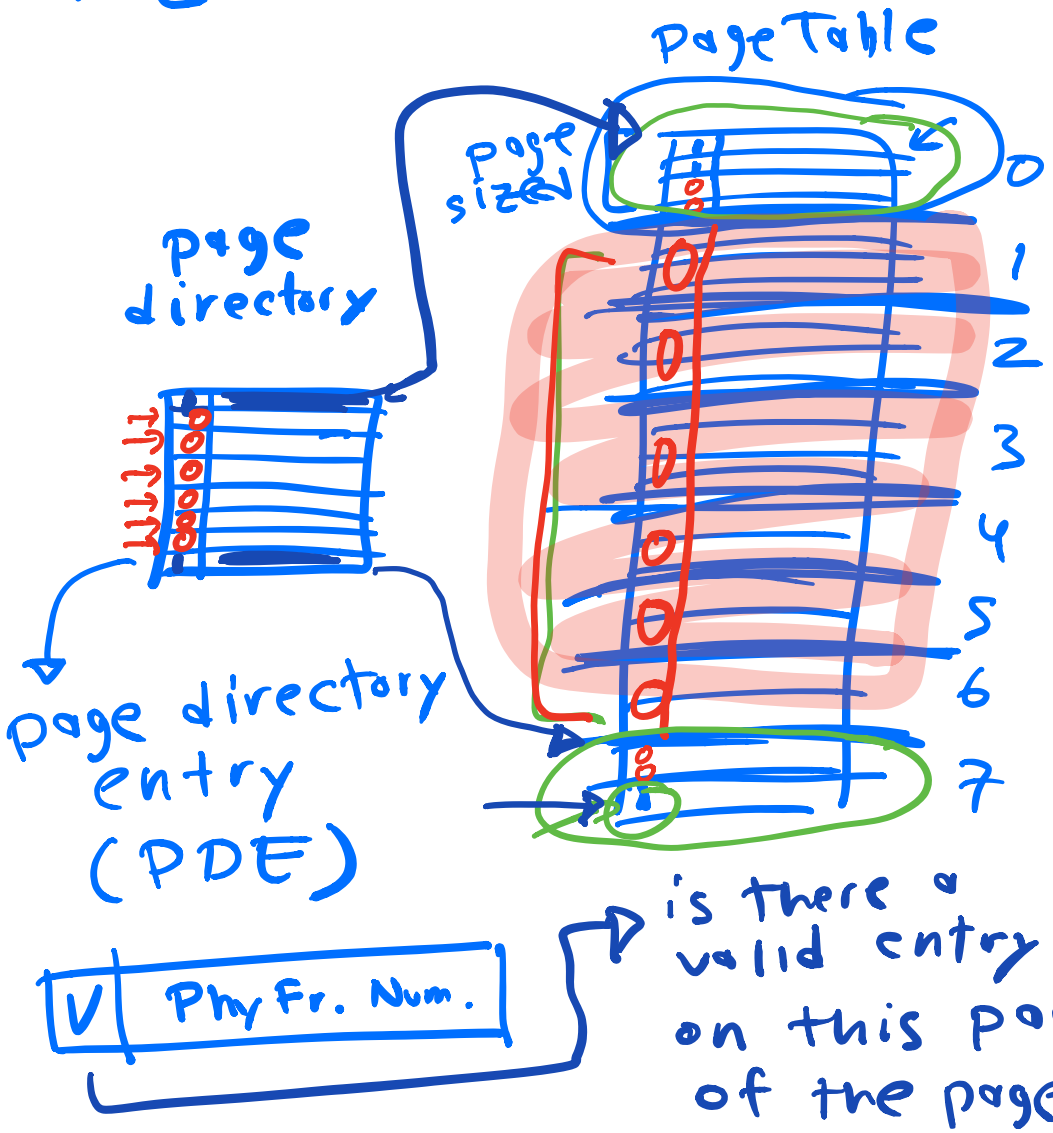
Solutions:

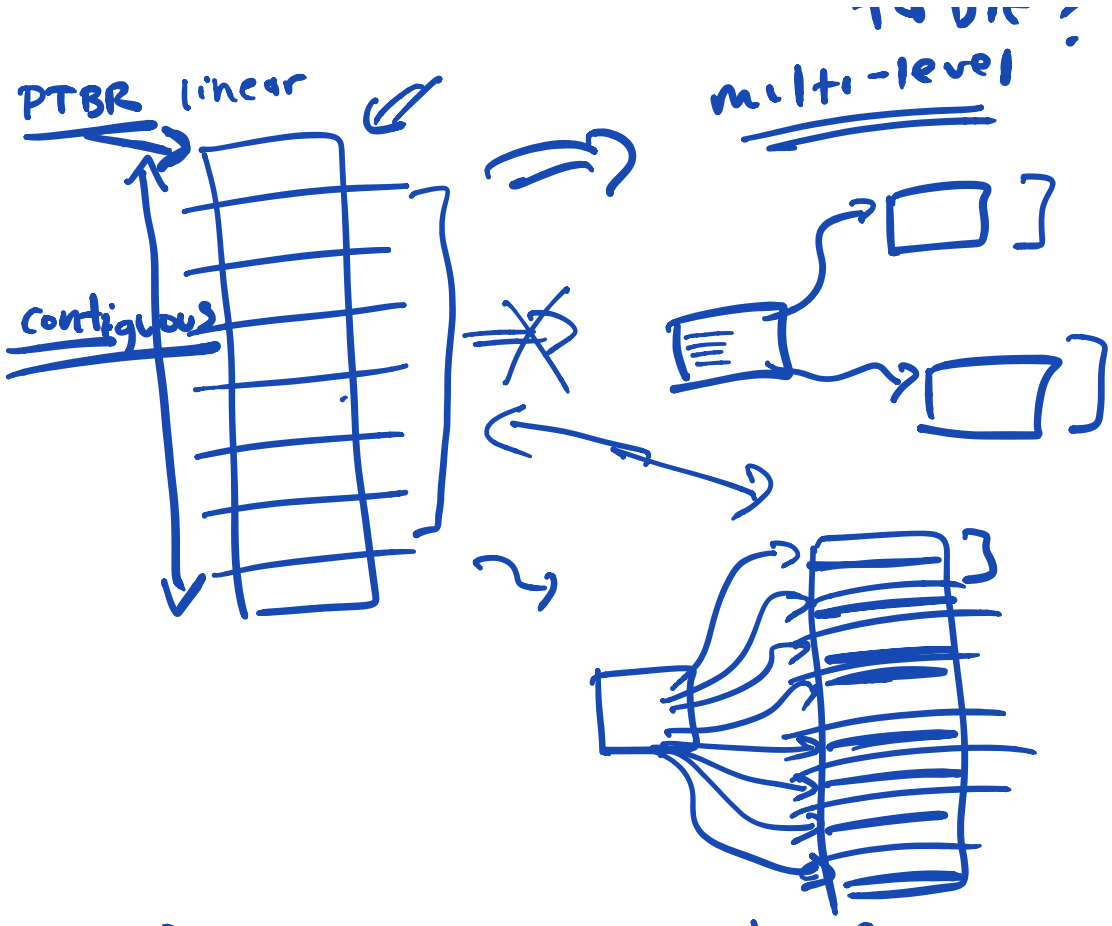
→ Multi-level Page Table

→ Hybrid: Segmentation + Paging

→ Inverted: one per system

▷ just data structures

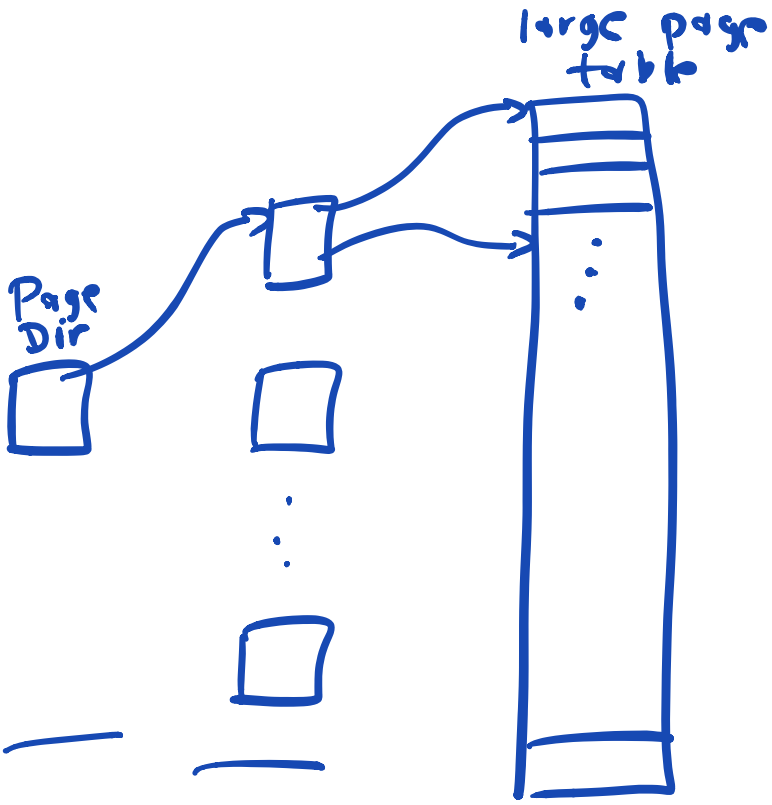




Q) why is OS mgmt of phys memory easier w/ multi-level PTs? (vs. linear?)

⇒ before

[tradeoff: space vs. time
⇒ M.L.P.T. (slower but smaller)]



Point of Discussion:

Best Broadway Musical?

HAMILTON

~~Sponge Bob the Musical~~

Book of Mormon

Cats

Lion King

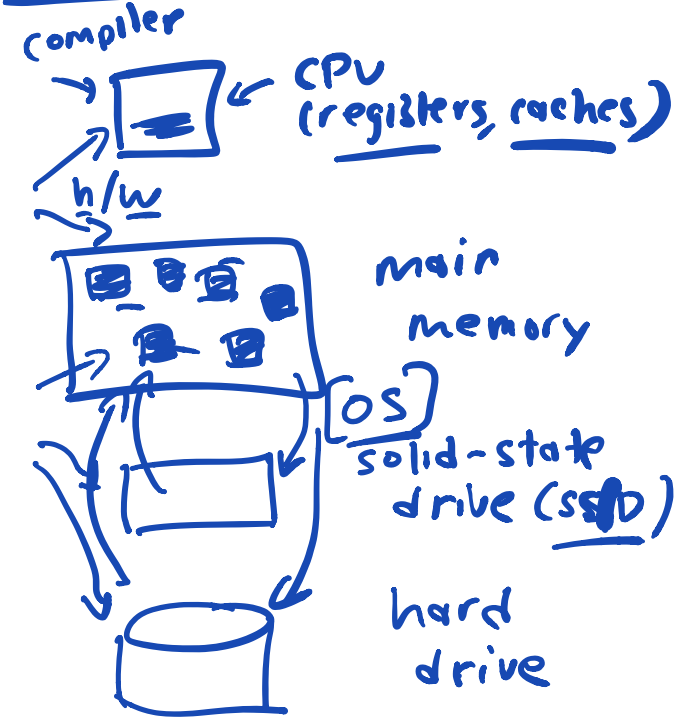
Wicked

Phantom of the Opera

=> [Read book, do homework problem on own]

Problem #3: virt. mem accessed by programs ? phys mem of system

Memory Hierarchy:



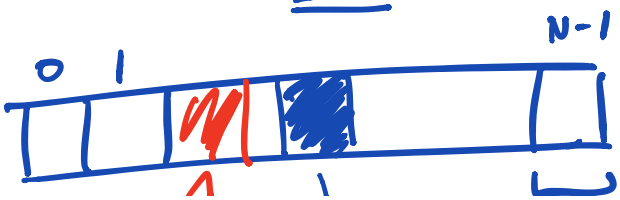
fast expensive small

large slow cheap

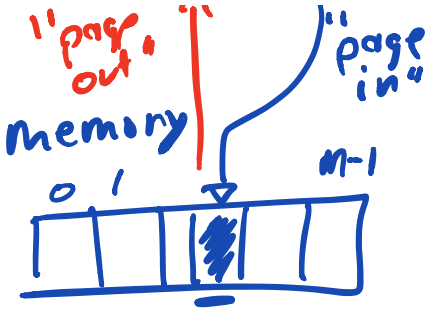
Mechanisms

Policy

-> swap space (on disk)

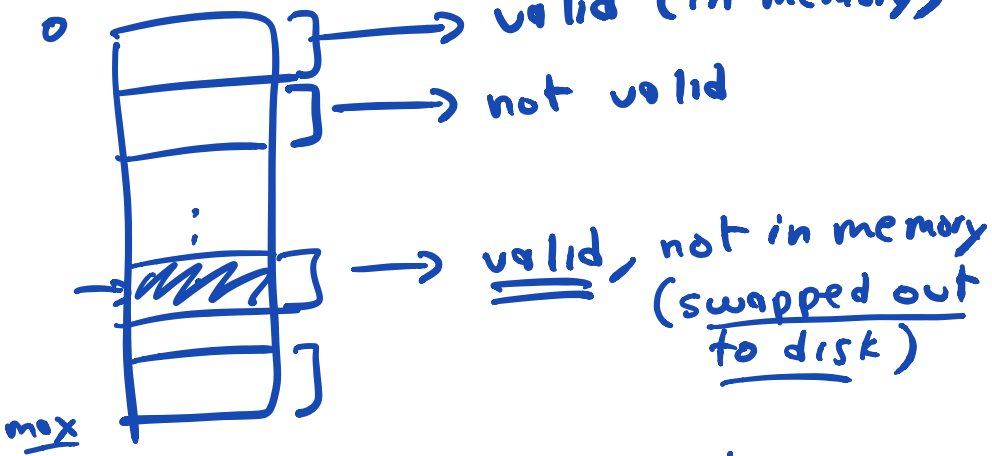


larger, slower

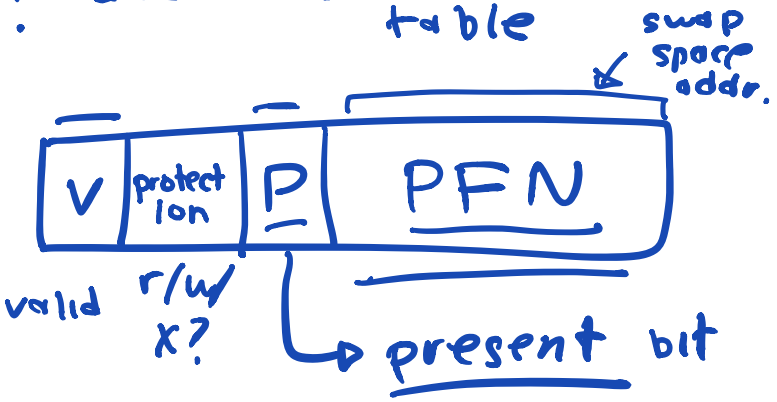


blocks => page sized (4 KB)

$[M < N]$



Track? add some info to page table

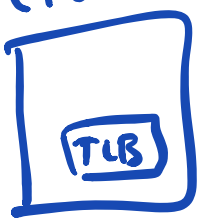


V=1, P=1 => valid, PFN is location

[V=1, P=0] => valid, page on disk somewhere

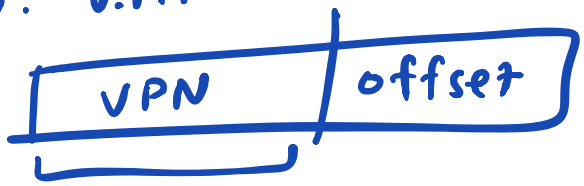
=> page miss
(page fault)

CPU



every mem. ref:

H/W: V.A. int addr.



consults TLB:

TLB hit: [PFN | offset]
||
access memory

TLB miss:
=> Fetch PTE
=> extract PTE
is valid? NOT => Seg. Fault
is prot OK? NOT => prot fault
is present? NOT => page fault

[OS: page fault handler

=> Find free phys. frame

if NOT,

page out existing page (swap)

=> [page replacement policy]

=> bring in desired page,

update PTE => present=1, PFN=___

[retry inst]

Policy:

Page Replacement:

when OS needs to kick out page, which one?

=> Least Recently Used (LRU)

=> Frequently (LFU)

=> Most Recently Used (MRU)

=> Random

=> FIFO

easy to implement

(Use History to predict future)

"better" & harder to build

Comparison: Optimal Policy

=) kick out the page that will be used furthest in future →

Example: mem size: 3 (pages)

hit or miss? what's in mem?

page →	1	1	2	0	1	3	0	1	2	0
FIFO	m	h	m	m	h	m	h	m	m	m
	1	1	1,2	1,2,0	1,2,0	3,0,2	3,0,2	1,3,0	2,1,3	2,1,3
LRU				1	1	2	0	1	0	1
			1	2	0	1	3	0	1	2
MRU	1	1	2	0	1	3	0	1	2	0
hit or miss	m	h	m	m	h	m	h	h	m	h
Opt?	—			—		—		—		—

How to implement "approximate" LRU?

=) why approximate?

LRU requires knowledge of access time of

each page

=) timestamp (page

=) h/w updates on each mem access

=) replacement: (LRU)

search, finding Least R.U. page

(SLOW)

approximate LRU:

"not recently used"

h/w: when page accessed, sets bit =) (reference bit)

OS: replacement

-> scans through pages

if ref bit = 0,
kick out: replace

if ref bit = 1,
set ref bit to 0
cont. scanning

ref bit 0 0 1 0 . . . 0 1

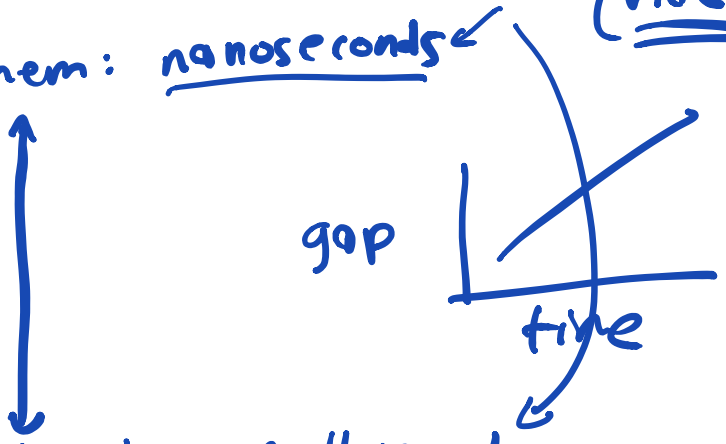
1) Technical Piece

2) Admin.

Problem w/ swapping:
"Disk" too slow

=)(p2b]
→last solo
→(video]⇐

mem: nanoseconds



hard drive: milliseconds

Solution: Buy more memory
(don't swap)

More memory always lead
to better "hit rate"?

1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5

FIFO
3

$FIFO_4$

Belady's Anomaly

Some policies, no problem:

LRU: LRU_4 contains LRU_3