CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

Prof. Gurindar Sohi

TAs: Junaid Khalid and Pradip Vallathol

Midterm Examination 2

In Class (50 minutes)

Friday, October 19, 2012

Weight: 17.5%

NO: BOOK(S), NOTE(S), OR CALCULATORS OF ANY SORT.

The exam has nine pages. **Circle your final answers**. Plan your time carefully since some problems are longer than others. You **must turn in the pages 1-8**.

LAST NAME: _____

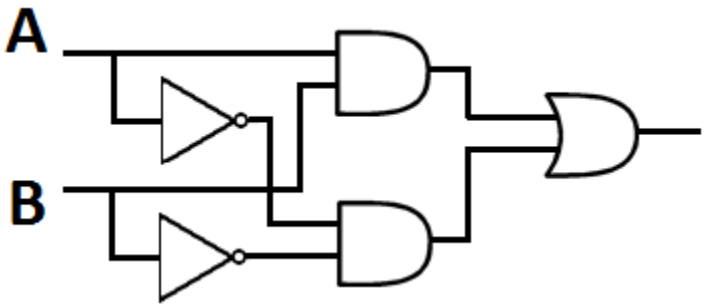
FIRST NAME: _____

ID# _____

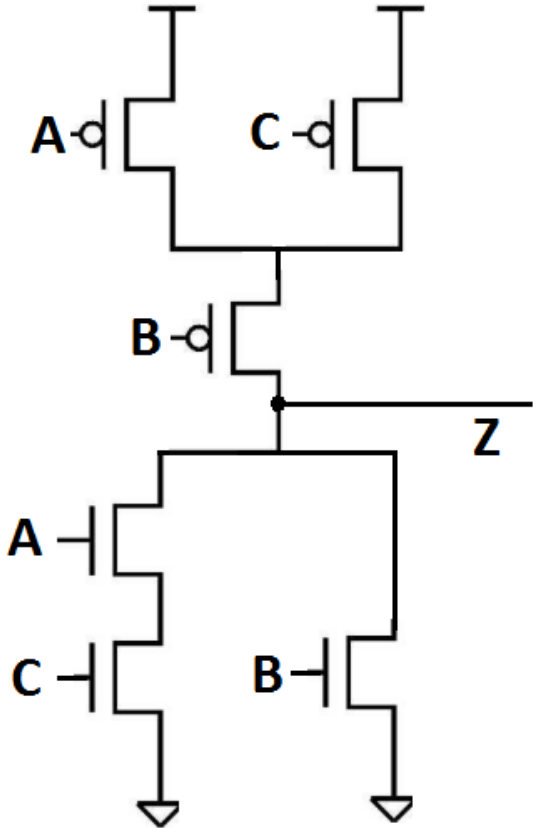
Problem	Maximum Points	Points Earned
1	2	
2	4	
3	2	
4	2	
5	5	
6	3	
7	3	
8	6	
9	3	
Total	30	

Problem 1: Draw the logic circuit for the following logic expression using 2 input AND gates, 2 input OR gates and NOT gates.

Z = ((A AND B) OR (NOT (A) AND NOT (B))) **(2 Points)**

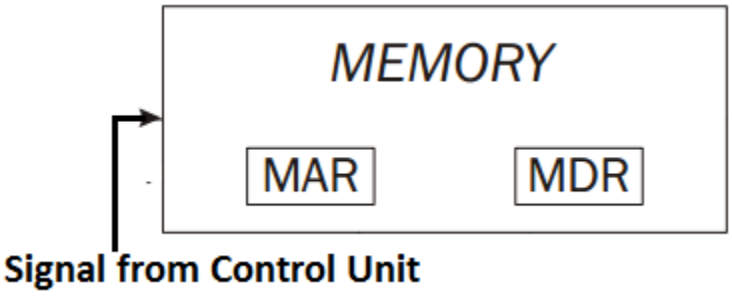


Problem 2: Complete the truth table for the following transistor level circuit: **(4 Points)**



INPUTS			OUTPUT
A	**B**	**C**	**Z**
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Problem 3: The figure below is the block diagram of the memory unit in a Von Neumann model.



List the steps required to

a) Read from a location **X** in memory. **(1 point)**

- Write the Address X into MAR
- Send Read signal to Memory
- Read Data from MDR

b) Write a value **A** to location **Y** in memory. **(1 point)**

- Write the data A into MDR
- Write the Address Y into MAR
- Send Write signal to Memory

Problem 4: What is the addressability of a memory whose total size is 1024 bytes and needs 9 bits of address to access a location in memory? **(2 points)**

(1024 * 8) / (512) = 16

Problem 5: Consider the State Diagram shown in Figure 1 (a). Each state is denoted as S_1S_0, and the values on the arrows represent the input IN, which causes the transition every clock cycle.

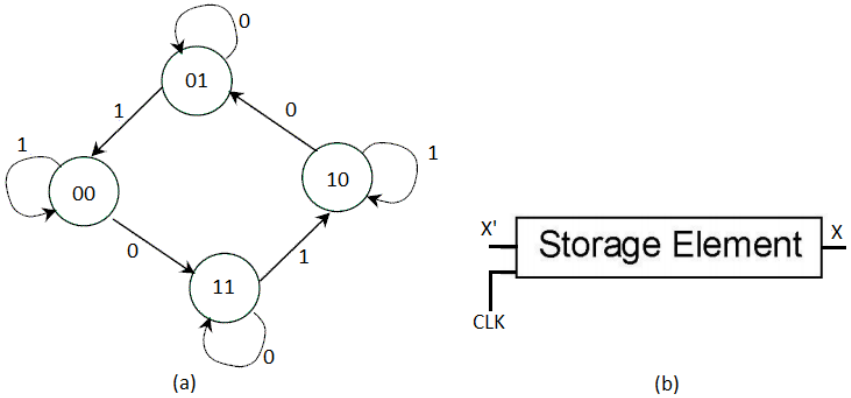
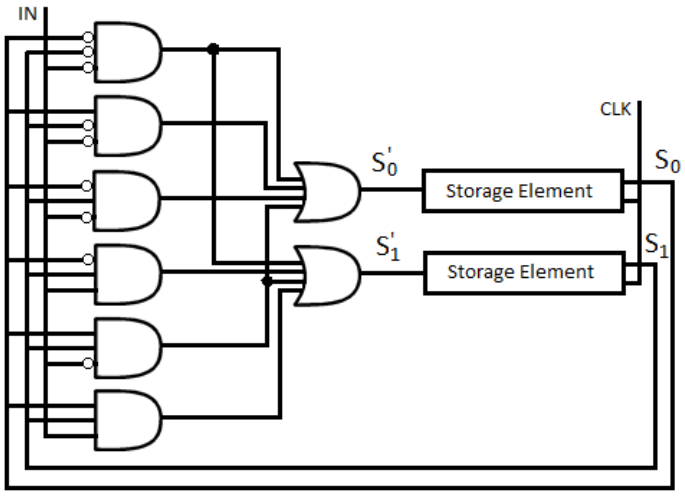


Figure 1

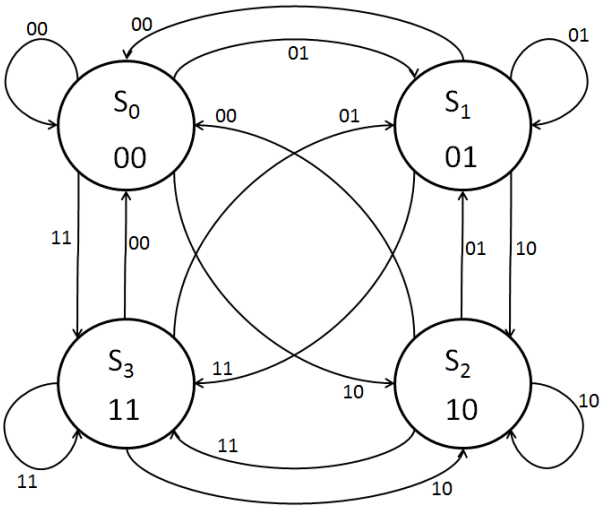
a) Fill in the following truth table for the Next State (S_1'S_0'). **(2 points)**

S_1	S_0	IN	S_1'	S_0'
0	0	0	1	1
0	0	1	0	0
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0

b) Show the logic circuit of the Finite State Machine (using combinational logic and flip-flops). Use any kind of logic gates. Use the representation shown in Figure 1 (b) for any 1-bit flip-flop required in the circuit (input CLK is the clock).



Problem 6: Consider a system with two switches S0 and S1, each controlling a bulb, B0 and B1, respectively. Every clock cycle, each bulb is switched ON or OFF depending on the state of its corresponding switch. Consider the state of switches as inputs (ON = 1, OFF = 0) and the state of the bulbs as outputs (ON = 1, OFF = 0). Draw a state diagram which shows all possible state transitions, the inputs which cause these transitions and the output at each state. Consider that the switches and the bulbs are turned OFF in the initial state. **(3 Points)**



Problem 7: Consider a 32 bit instruction that has the following format:

OPCODE	Destination Register	Source Register 1	Source Register 2	Unused bits (8 bits)

If the ISA supports 499 OPCODES, answer the following:

a) How many bits are required to represent the OPCODE field in the instruction? **(1 point)**

9 bits

b) How many registers are supported by the ISA? **(2 points)**

Number of bits for registers = (32 - 9 - 8)/3 = 5

32 registers

Problem 8: Circle the correct answer for the following:

i. How many output lines will a six-input decoder have? **(1 point)**

a. 32
b. 36
c. 64
d. 128

ii. After the fetch phase, PC and IR in the Control Unit of a Von Neumann Model contain, respectively: **(1 point)**

a. Address of the next instruction and the Current instruction
b. Address of the current instruction and the Current instruction
c. Address of the current instruction and the Next instruction
d. Address of the next instruction and the Next instruction

iii. How many gated D-latches are present in 4 16-bit registers? **(1 Point)**

a. 16
b. 24
c. 64
d. 128

iv. How many select lines will a 16 input multiplexer have? **(1 point)**

a. 1
b. 2
c. 4
d. 8

v. Which of the following can be used to implement a NOT gate? **(1 point)**

a. NAND gate
b. NOR gate
c. Either NAND or NOR
d. Neither NAND nor NOR

vi. The decode phase of the instruction cycle always examines the OPCODE field in the instruction. True / False **(1 point)**

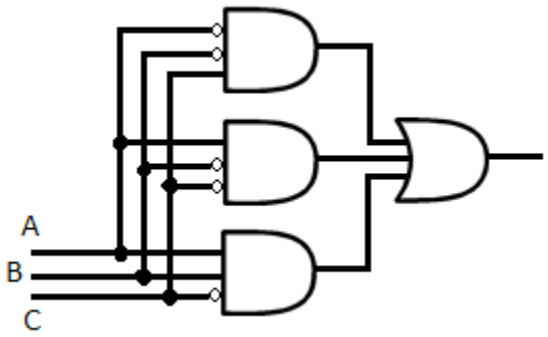
Problem 9: For the given truth table:

Inputs			Output
A	**B**	**C**	**Z**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

a) Write the two level AND-OR logic expression for Z as a function of inputs A, B and C. (Do not simplify the expression) **(1 Point)**

(NOT(A) AND NOT(B) AND C) OR (A AND NOT(B) AND NOT(C)) OR (A AND B AND NOT(C))

b) Draw the logic circuit diagram to implement the above logic expression using NOT gates, 3-input AND gates and 3-input OR gates. **(2 Points)**



Extra page for hand written work, if needed. This page is not required and will NOT affect your grade. You don't even need to hand this page in.