CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Examination 2
In Class (50 minutes)
Friday, October 21, 2016
Weight: 17.5%

NO: BOOK(S), NOTE(S), CALCULATORS OR ELECTRONIC DEVICES OF ANY SORT.
The exam has **eight pages**. You **must turn in the pages 1-8. Circle your final answers**. Plan your time carefully since some problems are longer than others. Use the blank sides of the exam for scratch work.

LAST NAME: _____

FIRST NAME: _____

Section: _____

ID#: _____

Problem	Maximum Points	Points Earned
1	2	
2	4	
3	3	
4	4	
5	5	
6	2	
7	3	
8	7	
Total	30	

Problem 1 (2 points)

Use DeMorgan's Law to reduce the number of NOT gates in the expression:

$Z = \overline{((\bar{A} \; AND \; \bar{C}) OR \; \bar{D})}$. Show your work for full credit.

Problem 2 (4 points)

Fill out the following truth table (Table 1) for point Z in the transistor-level circuit diagram (Refer Figure 1)
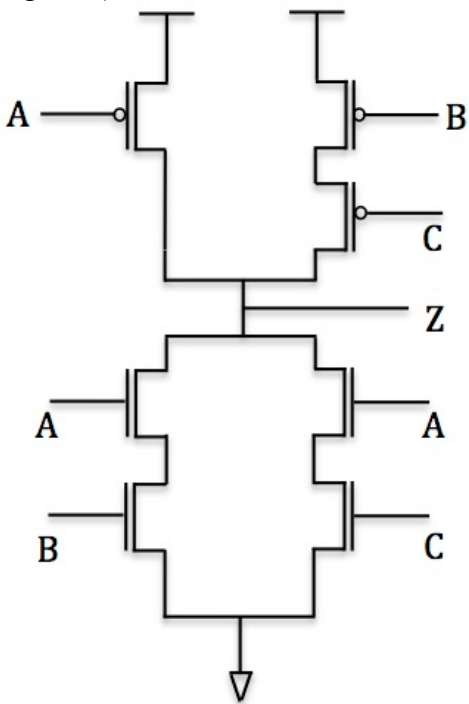

Figure 1

A	B	C	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Table 1 (for Problem 2)

Problem 3 (3 points)

Figure 2 shows the output of a 1-to-2 decoder connected to the D input of a gated D Latch. The input to the decoder (In) and the Write Enable (WE) Signal of the D Latch varies with every time unit as shown in the Table 2. Specify the value of the "out" and the "D" signals for each set of inputs. The first two time units (0 and 1) have been filled in the Table 2.

Figure 2

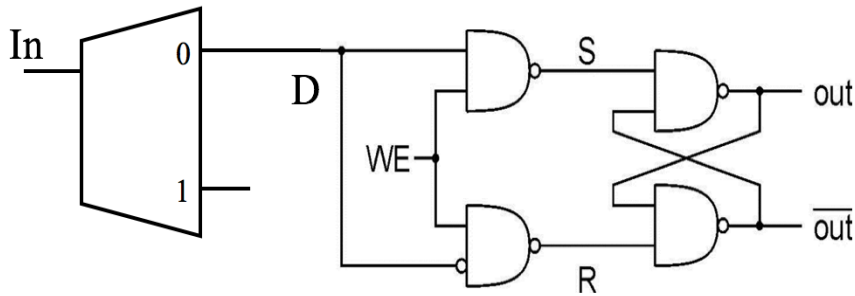| Time	0	1	2	3	4	5	6	7
In	0	1	0	1	1	0	1	0
WE	0	1	1	1	0	1	0	1
D	1	0						
out	1	0						

Table 2

Problem 4   **(4 points)**

An architecture has the following format for a 16-bit ISA

Opcode	Destination Register	Source Register 1	Source Register 2

Each register field is 3-bits wide, and the rest of the bits are used for the Opcode field. Assume that registers are numbered starting at 0.

a) What is the maximum number of unique opcodes in the ISA?

b) Assume that the ISA implements only 25 operations. The Control Unit uses a n-input decoder to decode these 25 different operations. What is the minimum value of n? How many output lines of the decoder are unused?

c) Assume that ADD instruction has an Opcode of 0x01, fill in the binary representation of the following instruction in the table below:

ADD r3, r2, r1: where r1, r2 are source register 1 and 2 respectively, and r3 is the destination register.

Opcode	Destination Register	Source Register 1	Source Register 2
_____	_____	_____	_____

Problem 5 (5 Points)

Consider the state diagram shown in Figure 3. Each state is denoted as S_1S_0, and the values on the arrows represent the input IN, which causes the transition every clock cycle.
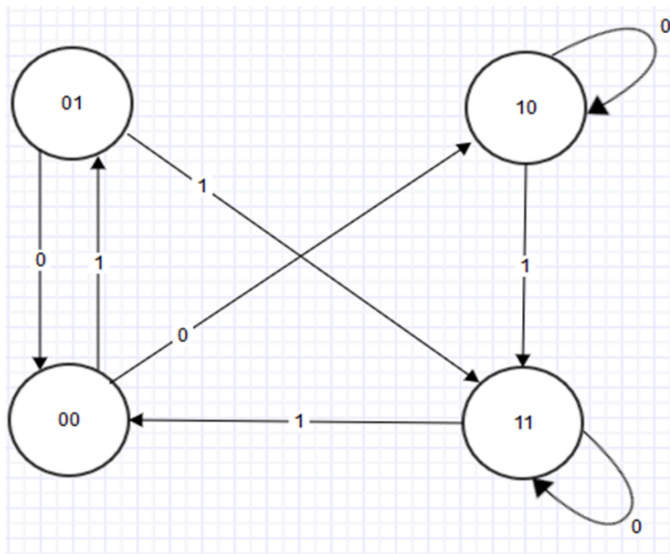

Figure 3

S_1	S_0	IN	S_1'	S_0'
0	0	0	1	0
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 3

a) Fill in the truth table for the next state ($S_1'S_0'$). The first row has been filled for you as an example. (Refer Table 3)

b) Show the logic circuit of the Finite State Machine (using combinational logic and flip-flops) which implements the above state diagram. Use any kind of logic gates. Use the representation shown in Figure 4 for any 1-bit flip-flop required in the circuit (input CLK is the clock).
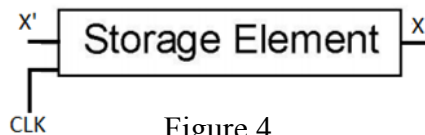

Figure 4

Problem 6   (2 points)

Suppose you want to use an 8-input Mux to select one of the inputs from A, B, C, D, and E. The output X of the mux is shown in Table 4, where S[2:0] are select lines. Label the inputs to the Mux (as one of A, B, C, D or E) in Figure 5. (Multiple gates may have the same input)

S[2]	S[1]	S[0]	X
0	0	0	B
0	0	1	C
0	1	0	D
0	1	1	E
1	0	0	A
1	0	1	A
1	1	0	A
1	1	1	A

Table 4

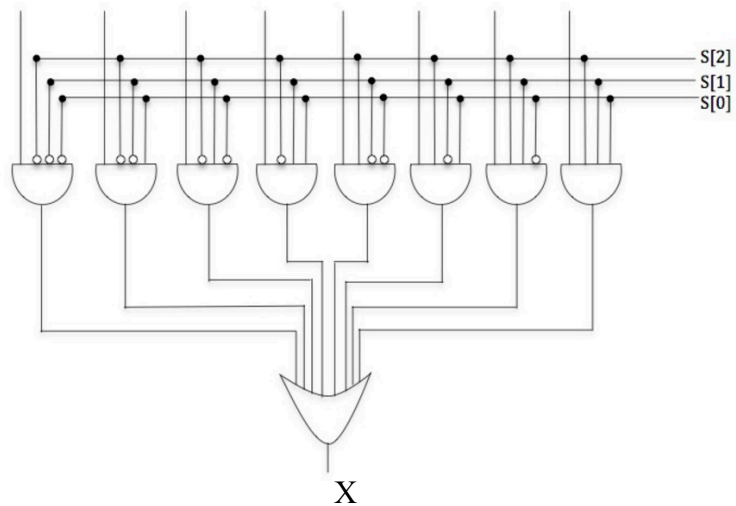Figure 5

Problem 7   (3 points)

Figure 6 shows a 1-bit full-adder, connected to a 2-to-4 decoder. The 1-bit full adder adds the value of bits S0, S1, and Cin, and outputs two bits: the sum (Sum) and the carry-out (Cout) bits. For example, when S0 = 0, S1 = 0, and Cin = 1, Sum = 1 and Cout = 0. The output of the adder is connected to the 2 control lines A[0] and A[1] of the decoder, as shown. Given that the outputs of the decoder are as shown in Figure 6, what are the corresponding values of S0, S1, and Cin? Explain your answer for full credit.
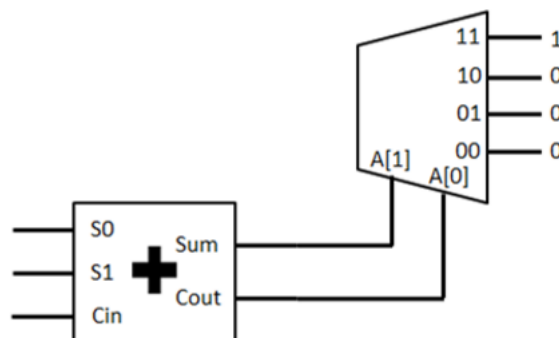

Figure 6

Problem 8

a) A memory uses 8 bits to represent its address space, and the memory has an addressability of 16 bits. What is the total size of the memory in bytes? **(2 points)**

b) A multiplexer has n+1 select lines. How many input lines does the multiplexer have? **(1 point)**

c) A control instruction like JMP can change the sequence of instruction execution. True/False? **(1 point)**

d) The following table contains a list of events performed during the FETCH cycle. Which of the following options correctly specify the order in which these events occur? (SELECT ONE OPTION from A, B, C or D) **(1 point)**

i.	Read memory location whose address is in MAR, and store value in MDR
ii.	Load contents of PC into MAR
iii.	Load IR with contents of MDR

    A. i, ii, iii
    B. ii, i, iii
    C. i, iii, ii
    D. iii, ii, i

e) For the following, match the term to the appropriate definition **(2 points)**

    A. Control unit
    B. Instruction
    C. Program counter
    D. Driver

	The fundamental unit of work that specifies the operation to be performed and data to be used.
	A program that controls access to a device.
	Contains the address of the next instruction to be executed.
	Interprets the instructions, telling other components what to do.