

CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Examination 2

In Class (50 minutes)

Friday, October 21, 2016

Weight: 17.5%

NO: BOOK(S), NOTE(S), CALCULATORS OR ELECTRONIC DEVICES OF ANY SORT.

The exam has **eight pages**. You **must turn in the pages 1-8**. **Circle your final answers**. Plan your time carefully since some problems are longer than others. Use the blank sides of the exam for scratch work.

LAST NAME: _____

FIRST NAME: _____

Section: _____

ID#: _____

Problem	Maximum Points	Points Earned
1	2	
2	4	
3	3	
4	4	
5	5	
6	2	
7	3	
8	7	
Total	30	

Problem 1

(2 points)

Use DeMorgan's law to reduce the number of NOT gates in the expression:

$$Z = \overline{((\bar{A} \text{ OR } \bar{C}) \text{ AND } \bar{D})}$$

Show your work for full credit.

$$Z = (A \text{ AND } C) \text{ OR } D$$

Problem 2

(4 points)

Fill out the following truth table (Table 1) for point Z in the transistor-level circuit diagram (Refer Figure 1)

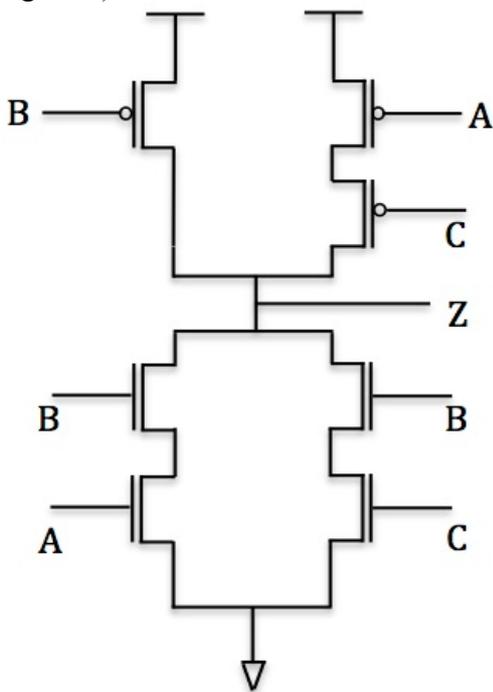


Figure 1

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Table 1 (for Problem 2)

Problem 3

(3 points)

Figure 2 shows the output of a 1-to-2 decoder connected to the D input of a gated D Latch. The input to the decoder (In) and the Write Enable (WE) Signal of the D Latch varies with every time unit as shown in the Table 2. Specify the value of the "out" and the "D" signals for each set of inputs. The first two time units (0 and 1) have been filled in the Table 2.

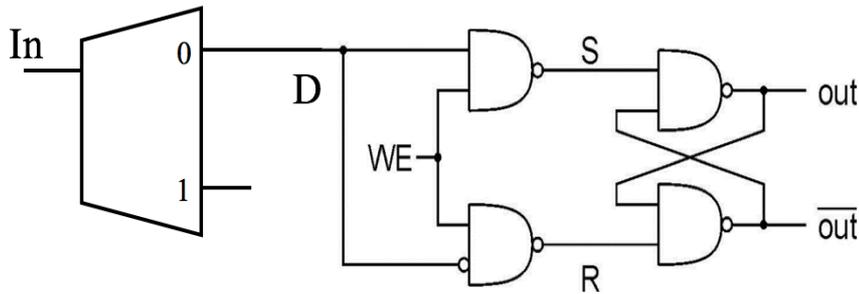


Figure 2

Time	0	1	2	3	4	5	6	7
In	0	0	0	1	1	0	0	0
WE	0	1	0	0	1	0	1	0
D	1	1	1	0	0	1	1	1
out	1	1	1	1	0	0	1	1

Table 2

Problem 4**(4 points)**

An architecture has the following format for a 16-bit ISA

Opcode	Destination Register	Source Register 1	Source Register 2
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Assume that the Opcode field is 4-bits wide, all register fields have equal width (i.e. an equal number of bits), and registers are numbered starting at 0.

- a) What is the maximum number of registers that can be represented in the ISA? Why?

12/3 = 4-bit to represent each register => 16 registers

- b) Assume that the ISA only implements 15 operations. The Control Unit uses an n-input decoder to decode these 15 different operations. What is the minimum value of n? How many output lines of the decoder are unused?

n = 4. (16-15 =) 1 output lines are unused

- c) Assume that ADD instruction has an Opcode of 0x2, fill in the binary representation of the following instruction in the table below:

ADD r2, r3, r1: where r3, r1 are source register 1 and 2 respectively, and r2 is the destination register.

Opcode 0010	Destination Register 0010	Source Register 1 0011	Source Register 2 0001
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Problem 5

(5 Points)

Consider the state diagram shown in Figure 3. Each state is denoted as S_1S_0 , and the values on the arrows represent the input IN, which causes the transition every clock cycle.

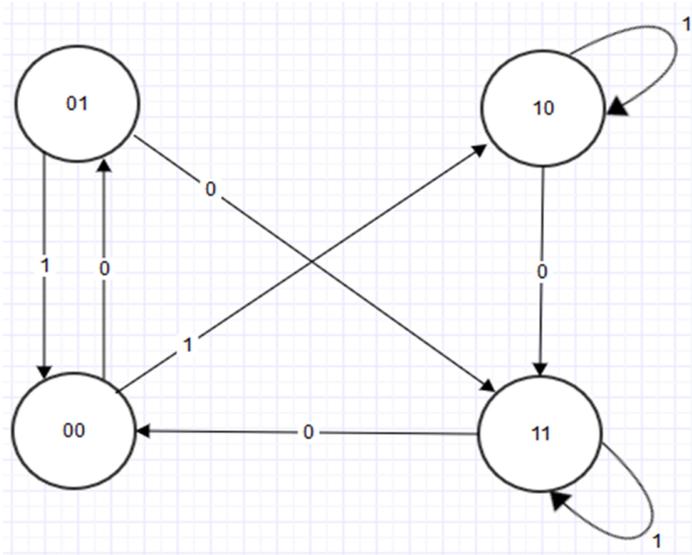


Figure 3

S_1	S_0	IN	S_1'	S_0'
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

Table 3

- Fill in the truth table for the next state ($S_1'S_0'$). The first row has been filled for you as an example. (Refer Table 3)
- Show the logic circuit of the Finite State Machine (using combinational logic and flip-flops), which implements the above state diagram. Use any kind of logic gates. Use the representation shown in Figure 4 for any 1-bit flip-flop required in the circuit (input CLK is the clock).

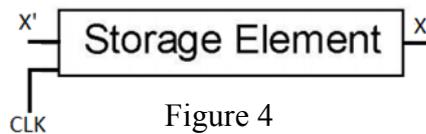


Figure 4

Problem 6

(2 points)

Suppose you want to use an 8-input Mux to select one of the inputs from A, B, C, D, and E. The output X of the mux is shown in Table 4, where S[2:0] are select lines. Label the inputs to the Mux (as one of A, B, C, D or E) in Figure 5. (Multiple gates may have the same input)

S[2]	S[1]	S[0]	X
0	0	0	A
0	0	1	A
0	1	0	A
0	1	1	A
1	0	0	B
1	0	1	C
1	1	0	D
1	1	1	E

Table 4

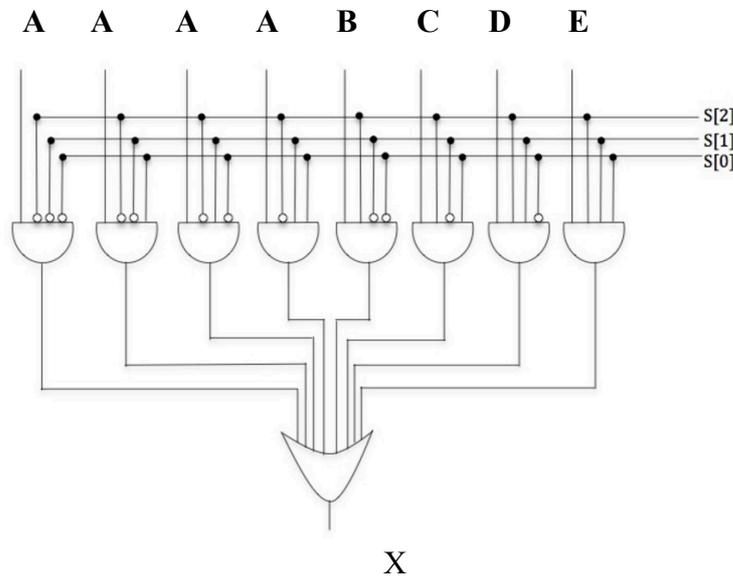


Figure 5

Problem 7

(3 points)

Figure 6 shows a 1-bit full-adder, connected to a 2-to-4 decoder. The 1-bit full adder adds the value of bits S0, S1, and Cin, and outputs two bits: the sum (Sum) and the carry-out (Cout) bits. For example, when S0 = 0, S1 = 0, and Cin = 1, Sum = 1 and Cout = 0. The output of the adder is connected to the 2 control lines A[0] and A[1] of the decoder, as shown. Given that the outputs of the decoder are as shown in Figure 6, what are the corresponding values of S0, S1, and Cin? Explain your answer for full credit.

S0 = 0, S1 = 0, Cin = 0

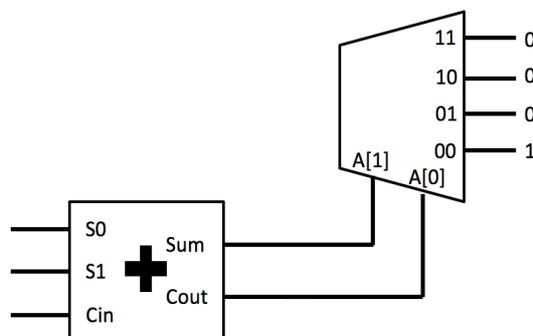


Figure 6

Problem 8

- a) A memory uses 6 bits to represent its address space, and the memory has an addressability of 32 bits. What is the total size of the memory in bytes? **(2 points)**

$2^6 * 32 \text{ bits} = 2048 \text{ bits} = 256 \text{ bytes}$

- b) A control instruction like JMP can change the sequence of instruction execution. True/False?

(1 point)

True

- c) A multiplexer has n-1 select lines. How many input lines does the multiplexer have? **(1 point)**

$2^{(n-1)}$

- d) The following table contains a list of events performed during the FETCH cycle. Which of the following options correctly specify the order in which these events occur? (SELECT ONE OPTION from A, B, C or D) **(1 point)**

i.	Load contents of PC into MAR
ii.	Load IR with contents of MDR
iii.	Read memory location whose address is in MAR, and store value in MDR

- A. i, ii, iii
- B. ii, i, iii
- C. i, iii, ii**
- D. iii, ii, i

- e) For the following, match the term to the appropriate definition **(2 points)**

- A. Control unit
- B. Instruction
- C. Program counter
- D. Driver

D	A program that controls access to a device.
A	Interprets the instructions, telling other components what to do.
B	The fundamental unit of work that specifies the operation to be performed and data to be used.
C	Contains the address of the next instruction to be executed.