CS838 HW #4: NetFPGA and Verilog

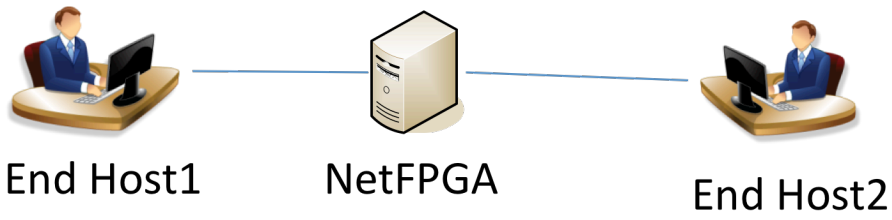
In this assignment, you will learn how to program in verilog and modify NetFPGAs. The goal of this assignment is to calculate a checksum over every packet received and drop packets that fail the check. A standard router performs a checksum on every packet it receives and disregards those that fail the check sum. You should calculate your checksum after the router has performed its check.

Your check sum should verify that the number of bits set in each packet is divisible by 4.

Getting started:

To complete this homework, you should create a module which examines and drops packets. The rate limiter module is an excellent starting point. Also, the NetFGPA wiki contains excellent documentation on writing and wiring modules.

Implementation and testing:



For this homework, you will each be provided with a NetFPGA device and 2 end hosts (similar to the above figure). You can test your code by sending packets between the two end hosts and checking to see if the packets get dropped. You should run ethereal or tethereal to get a dump of the packets and verify how many bits are set in the packet.

What to sumbit:

You should submit your new module, as well as a README file explaining the module.

NetFPGA Resources

As you start to work on this project, you may find the following links useful.

- CS838 NetFPGA Tutorial
- NetFPGA Website
- NetFPGA Wiki
- NetFPGA Guide
- Walkthrough the Reference Designs
- The Verilog Golden Reference Guide