

# Alaa R. Alameldeen

Research Scientist  
Intel Labs  
Hillsboro, Oregon, USA

## CONTACT INFORMATION

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**Home Page:** <http://www.cs.wisc.edu/~alaa/>, <http://www.cecs.pdx.edu/~alaa/>

## RESEARCH INTERESTS

Computer architecture, including (but not limited to):

- Processor microarchitecture.
- Multiprocessor and chip multiprocessor systems design.
- Energy-efficient architectures and memory systems.
- Cache compression.
- Performance evaluation of multi-threaded commercial workloads.

## EDUCATION

### Ph.D. in Computer Sciences, March 2006

Department of Computer Sciences, University of Wisconsin-Madison, Madison, WI, USA.  
Advisor: Prof. David A. Wood.

### M.Sc. in Computer Sciences, December 2000

Department of Computer Sciences, University of Wisconsin-Madison, Madison, WI, USA.  
Ph.D. Minor in Business, May 2002. GPA: 3.93 / 4.0.

### M.Sc. in Computer Science, July 1999

Faculty of Engineering, Alexandria University, Alexandria, Egypt. GPA: 4.0 / 4.0.

### B.Sc. in Computer Science and Automatic Control, June 1996

Faculty of Engineering, Alexandria University, Alexandria, Egypt. GPA: 3.95 / 4.0.

## RESEARCH EXPERIENCE

**Research Scientist.** Intel Corporation, Oregon Microarchitecture Lab, April 2006-Present

- Conducting forward-looking research for future Intel processors. Research focuses on energy-efficient architectures and memory systems.

**Graduate Research Assistant.** University of Wisconsin-Madison, Department of Computer Sciences, June 2000-March 2006.

- Member of the Wisconsin Multifacet project ([www.cs.wisc.edu/multifacet/](http://www.cs.wisc.edu/multifacet/)) co-directed by Professors Mark D. Hill and David A. Wood.
- Participated in developing Multifacet's commercial workload simulation infrastructure.
- Studied and advocated a statistical methodology for multi-threaded workload evaluation.
- Designed and evaluated compressed cache systems for uniprocessors and chip multiprocessors for my Ph.D. dissertation. Advisor: Professor David A. Wood.

**Graduate Researcher.** Computer Science Department, Alexandria University, Alexandria, Egypt, September 1996-July 1999

- Research Focus: Computer vision.
- Designed and compared sequential methods for recovering structure and motion of a rigid object from an image sequence for my masters dissertation. Advisor: Professor Mohamed A. Ismail.

## TEACHING EXPERIENCE

**Adjunct Faculty.** Portland State University, Department of Electrical and Computer Engineering, September 2008-Present. Teaching two graduate-level, quarter-based computer architecture courses, Advanced Computer Architecture I (<http://www.cecs.pdx.edu/~alaa/ece587/>) and Advanced Computer Architecture II (<http://www.cecs.pdx.edu/~alaa/ece588/>).

**Graduate Teaching Assistant.** University of Wisconsin-Madison, Department of Computer Sciences, August 1999-May 2000. Leading discussion sections, grading and consulting for two computer science undergraduate classes.

**Graduate Teaching Assistant.** Alexandria University, Department of Computer Science, Alexandria, Egypt, September 1996-June 1999. Instructor, leading discussion sections, consulting, grading and lab supervision for many computer science undergraduate classes.

**Graduate Instructor.** Alexandria University, Scientific Computation Center, Alexandria, Egypt, July 1996- August 1999. Taught 2-3 week introductory computer courses.

## OTHER WORK EXPERIENCE

**System Analyst and Programmer.** Alexandria University, Scientific Computation Center, Alexandria, Egypt, July 1998-March 1999. Designed and implemented the database system for the Spinning Testing Lab in CATGO (General Organization for Cotton Arbitration and Testing), Alexandria, Egypt using MS Access.

**Undergraduate Intern.** Standardata Egypt, Alexandria, Egypt, July 1995-September 1995: Training on Unix, C Programming and Screen/Printer Arabic Language Interface Programs.

**Undergraduate Intern.** AMAC, Alexandria, Egypt, July 1994-September 1994: Training on Systems Operation and Programming in COBOL for an IBM/360 Compatible System.

## PUBLICATIONS

(To access these documents, please visit <http://www.cs.wisc.edu/~alaa/alaa.publications.html>)

### JOURNAL PUBLICATIONS

1. Alaa R. Alameldeen, Zeshan Chishti, Chris Wilkerson, Wei Wu, and Shih-Lien Lu, "Adaptive Cache Design to Enable Reliable Low-Voltage Operation," IEEE Transactions on Computers Volume 60, No. 1, pages 50-63, January 2011.
2. Keith A. Bowman, Alaa R. Alameldeen, Srikanth T. Srinivasan, Chris B. Wilkerson, "Impact of Die-to-Die and Within-Die Parameter Variations on the Clock Frequency and Throughput of Multi-Core Processors," IEEE Transactions on Very Large Scale Integration Systems, Volume 17, No. 12, pages 1679-1690, December 2009.
3. Chris Wilkerson, Hongliang Gao, Alaa R. Alameldeen, Zeshan Chishti, Muhammad Khellah and Shih-Lien Lu, "Trading off Cache Capacity for Low Voltage Operation," IEEE Micro Special Issue: Micro Top Picks from Architecture Conferences 2008, Volume 29, No. 1, pages 96-103, January-February 2009.
4. Alaa R. Alameldeen and David A. Wood, "IPC Considered Harmful for Multiprocessor Workloads," IEEE Micro, Volume 26, No. 4, pages 8-17, June-August 2006.
5. Milo M.K. Martin, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood, "Multifacet's General Execution-Driven Multiprocessor Simulation (GEMS) Toolset," Computer Architecture News (CAN), September 2005.
6. Alaa R. Alameldeen and David A. Wood, "Addressing Workload Variability in Architectural Simulations," IEEE Micro Special Issue: Micro's Top Picks from Microarchitecture Conferences, Volume 23, No. 6, pages 94-98, November-December 2003. 15 of 72 submissions accepted (21%).
7. Alaa R. Alameldeen, Milo M.K. Martin, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill and David A. Wood, "Simulating a \$2M Commercial Server on a \$2K PC," IEEE Computer, February 2003, pages 50-57.

## **REFEREED CONFERENCE PUBLICATIONS**

1. Alaa R. Alameldeen, Ilya Wagner, Zeshan Chishti, Wei Wu, Chris Wilkerson, and Shih-Lien Lu, "Energy-Efficient Cache Design Using Variable-Strength Error-Correcting Codes," 38<sup>th</sup> Annual International Symposium on Computer Architecture (ISCA-38), pages 461-471, San Jose, CA, June 2011. 40 of 208 submissions accepted (19%).
2. Chris Wilkerson, Alaa R. Alameldeen, Zeshan Chishti, Wei Wu, Dinesh Somasekhar, and Shih-Lien Lu, "Reducing Cache Power with Low-Cost, Multi-Bit Error-Correcting Codes," 37<sup>th</sup> Annual International Symposium on Computer Architecture (ISCA-37), pages 83-93, Saint Malo, France, June 2010. 44 of 245 submissions accepted (18%).
3. Zeshan Chishti, Alaa R. Alameldeen, Chris Wilkerson, Wei Wu, and Shih-Lien Lu, "Improving Cache Lifetime Reliability at Ultra-Low Voltages," 42<sup>nd</sup> Annual International Symposium on Microarchitecture (MICRO-42), pages 89-99, New York City, NY, USA, December 2009. 52 of 209 submissions accepted (25%).
4. Chris Wilkerson, Hongliang Gao, Alaa R. Alameldeen, Zeshan Chishti, Muhammad Khellah and Shih-Lien Lu, "Trading off Cache Capacity for Reliability to Enable Low Voltage Operation," 35<sup>th</sup> Annual International Symposium on Computer Architecture (ISCA-35), pages 203-214, Beijing, China, June 2008. 37 of 259 submissions accepted (14%).
5. Keith A. Bowman, Alaa R. Alameldeen, Srikanth T. Srinivasan, and Chris B. Wilkerson, "Impact of Die-to-Die and Within-Die Parameter Variations on Throughput Distribution of Multi-Core Processors," International Symposium on Low Power Electronics and Design (ISLPED), Portland, Oregon, USA, August 2007.
6. Alaa R. Alameldeen and David A. Wood, "Interactions Between Compression and Prefetching in Chip Multiprocessors," 13<sup>th</sup> Annual International Symposium on High Performance Computer Architecture (HPCA-13), Phoenix, Arizona, USA, February 2007. 28 of 174 submissions accepted (16%).
7. Alaa R. Alameldeen and David A. Wood, "Adaptive Cache Compression for High-Performance Processors," 31<sup>st</sup> Annual International Symposium on Computer Architecture (ISCA-31), Munich, Germany, June 2004, pages 212-223. 31 of 217 submissions accepted (14%).
8. Alaa R. Alameldeen and David A. Wood, "Variability in Architectural Simulations of Multi-threaded Workloads," 9<sup>th</sup> Annual International Symposium on High Performance Computer Architecture (HPCA-9), Anaheim, California, USA, February 2003, pages 7-18. 31 of 141 submissions accepted (22%).
9. Ashraf Aboulnaga, Alaa R. Alameldeen and Jeffrey F. Naughton, "Estimating the Selectivity of XML Path Expressions for Internet Scale Applications," 27<sup>th</sup> International Conference on Very Large Data Bases (VLDB), Rome, Italy, September 2001, pages 591-600. 59 of 339 submissions accepted (17%).
10. Milo M. K. Martin, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, and David A. Wood, "Timestamp Snooping: An Approach for Extending SMPs," 9<sup>th</sup> International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-IX), Boston, Massachusetts, USA, November 2000, pages 25-36. 24 of 114 submissions accepted (21%).
11. Alaa R. Alameldeen and M. A. Ismail, "Sequential Methods for Recovering Structure and Motion of a Rigid Object from an Image Sequence," In Proc. CVPRIP'2000, Atlantic City, New Jersey, USA, February-March 2000.

## **REFEREED WORKSHOP PUBLICATIONS**

1. Alaa R. Alameldeen, Carl J. Mauer, Min Xu, Pacia J. Harper, Milo M.K. Martin, Daniel J. Sorin, Mark D. Hill and David A. Wood, "Evaluating Non-deterministic Multi-threaded Commercial Workloads," 5<sup>th</sup> Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW-02), Cambridge, MA, February 2002, pages 30-38.

## NON-REFEREED PUBLICATIONS

1. Alaa R. Alameldeen, "Using Compression to Improve Chip Multiprocessor Performance," Ph.D. dissertation, Computer Sciences Department, University of Wisconsin-Madison, Madison, Wisconsin, USA, March 2006.
2. Alaa R. Alameldeen and David A. Wood, "Frequent Pattern Compression: A Significance-Based Compression Scheme for L2 Caches," Department of Computer Sciences Technical Report CS-TR-2004-1500, April 2004.
3. Alaa R. Alameldeen, "Sequential Methods for Recovering Structure and Motion of a Rigid Object from an Image Sequence," M.Sc. dissertation, Department of Computer Science and Automatic Control, Faculty of Engineering, Alexandria University, Alexandria, Egypt, July 1999.

## PATENTS (Last Updated 2006)

1. "Adaptive Cache Compression for High-Performance Processors," with David A. Wood.

## INVITED AND CONFERENCE TALKS

### *Energy-Efficient Cache Design Using Variable-Strength Error-Correcting Codes*

- 38<sup>th</sup> International Symposium on Computer Architecture (ISCA-38), San Jose, California, USA, June 2011.

### *Improving Cache Lifetime Reliability at Ultra-Low Voltages*

- 42<sup>nd</sup> International Symposium on Microarchitecture (MICRO-42), New York City, New York, USA, December 2009.

### *Interactions between Compression and Prefetching in Chip Multiprocessors*

- 13<sup>th</sup> International Symposium on High Performance Computer Architecture (HPCA-13), Phoenix, Arizona, USA, February 2007.

### *Cores, Caches, and Compression in Chip Multiprocessors*

- Purdue University, West Lafayette, Indiana, USA, April 2005.
- Intel, Hudson, Massachusetts, USA, August 2005.
- Intel, Santa Clara, California, USA, September 2005.
- Intel, Hillsboro, Oregon, USA, September 2005.
- AMD, Sunnyvale, California, USA, September 2005.

### *GEMS: Multifacet's General Execution-Driven Multiprocessor Simulator*

- Tutorial at the 32<sup>nd</sup> International Symposium on Computer Architecture (ISCA-32), June 2006 (with Michael R. Marty, Bradford M. Beckmann, Luke Yen, Min Xu and Kevin E. Moore).

### *Adaptive Cache Compression for High Performance Processors*

- 31<sup>st</sup> International Symposium on Computer Architecture (ISCA-31), Munich, Germany, June 2004.
- 9<sup>th</sup> Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, Wisconsin, USA, October 2004.

### *Using Cache Compression to Improve CMP Performance*

- 8<sup>th</sup> Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, Wisconsin, USA, October 2004.

### *Simulating a \$2M Commercial Server on a \$2K PC*

- Intel Labs, Hillsboro, Oregon, USA, March 2003.

### *Variability in Architectural Simulations of Multi-threaded Workloads*

- Intel Labs, Hillsboro, Oregon, USA, March 2003.
- 9<sup>th</sup> International Symposium on High Performance Computer Architecture (HPCA-9), Anaheim, California, USA, February 2003.
- 7<sup>th</sup> Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, Wisconsin, USA, October 2002.

*Sequential Methods for Recovering Structure and Motion of a Rigid Object from an Image Sequence*

- International Conference on Computer Vision, Pattern Recognition and Image Processing (CVPRIP'2000), Atlantic City, New Jersey, USA, March 2000

## **HONORS AND AWARDS**

- Ranked 1<sup>st</sup> on the Dept. of Computer Science and Automatic Control students during the academic years 1992-1993 to 1995-1996.
- Ranked 1<sup>st</sup> on the faculty of engineering students during the academic year 1991-1992 and upon graduation in the academic year 1995-1996 (B.Sc.).
- Awarded the Prof. Abdelsamie Mustafa prize for the top student of the Faculty of Engineering in 1996.
- Awarded the Prof. Naim Abou Taleb prize for the top student of the Dept. of Computer Science and Automatic Control in 1996.
- Ranked 8<sup>th</sup> on the Mathematics section high school students in Egypt upon graduation.

## **PROFESSIONAL ACTIVITIES AND SERVICE**

- Organizing Committee Chair, JILP Workshop on Data Prefetching: Data Prefetching Championship (with HPCA-2009), February 2009.
- Workshop Chair, 39<sup>th</sup> International Symposium on Computer Architecture (ISCA-39), Portland, OR, June 2012.
- Organizing Committee member, 1<sup>st</sup> JILP Workshop on Computer Architecture Competitions (JWAC-1): Cache Replacement Championship (with ISCA 2010), June 2010.
- Organizing Committee member, 2<sup>nd</sup> JILP Workshop on Computer Architecture Competitions (JWAC-2): Championship Branch Prediction (with ISCA 2011), June 2011.
- Serving on the steering committee for the JILP Workshop on Architecture Competitions.
- Guest editor for the JILP Special Issue on Data Prefetching, August 2010.
- Program Committee Member for the 26<sup>th</sup> International Parallel and Distributed Processing Symposium (IPDPS 2012), 1<sup>st</sup> JILP Workshop on Computer Architecture Competitions (JWAC-1, with ISCA 2010), 2<sup>nd</sup> JILP Workshop on Computer Architecture Competitions (JWAC-2, with ISCA 2011), 2<sup>nd</sup> International Forum on Next-generation MultiCore/ManyCore Technologies (IFMT'10, with ISCA 2010), 5th Annual Workshop on Modeling, Benchmarking and Simulation (MoBS, with ISCA 2009), JILP Workshop on Data Prefetching (DPC-1, with HPCA 2009), and 1<sup>st</sup> International Forum on Next-generation MultiCore/ManyCore Technologies (IFMT'2008).
- Reviewer for the International Symposium on Computer Architecture (ISCA), International Symposium on High-Performance Computer Architecture (HPCA), International Symposium on Microarchitecture (MICRO), International Symposium on Low Power Electronics and Design (ISLPED), International Conference on Parallel and Distributed Systems (ICPADS), IEEE Transactions on Computers, IEEE Transactions on CAD, ACM Transactions on Architecture and Code Optimization, and ACM Transactions on Computer Systems.
- Member of the ACM, the IEEE and the IEEE Computer Society since 2006 (Student Member 2000-2006).
- Member of ACM Special Interest Group on Computer Architecture (SIGARCH), IEEE Technical Committee on Computer Architecture (TCCA), Technical Committee on Microprocessors and Microcomputers (TCMCOMP), Technical Committee on Microprogramming and Microarchitecture (TCUARCH), Technical Committee on Simulation (TCSIM), Technical Committee on Pattern Analysis and Machine Intelligence (TCPAMI).
- Organizer of the Computer Architecture Seminar at the University of Wisconsin-Madison, Spring 2003.

## **REFERENCES**

Available Upon Request