Alaa R. Alameldeen

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Intel Labs
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CONTACT INFORMATION

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RESEARCH INTERESTS

Computer architecture and systems, including (but not limited to):

- Processor microarchitecture, multiprocessor architecture, energy-efficient architectures, and high-performance computing.
- Memory architecture, processing in/near memory, secure cache and memory systems, memory reliability, and cache/memory compression.
- Hardware/software co-design, accelerators for machine learning workloads, performance evaluation of commercial workloads, and architectural support for operating systems and application software.

EDUCATION

Ph.D. in Computer Sciences, March 2006
Department of Computer Sciences, University of Wisconsin-Madison, Madison, WI, USA.
Advisor: Prof. David A. Wood.

M.Sc. in Computer Sciences, December 2000
Department of Computer Sciences, University of Wisconsin-Madison, Madison, WI, USA.
Ph.D. Minor in Business, May 2002.

M.Sc. in Computer Science, July 1999
Faculty of Engineering, Alexandria University, Alexandria, Egypt.

B.Sc. in Computer Science and Automatic Control, June 1996
Faculty of Engineering, Alexandria University, Alexandria, Egypt.

RESEARCH EXPERIENCE

Research Scientist. Intel Labs, Intel Corporation, April 2006-Present
Conducting forward-looking research for future Intel products.

- Memory and Accelerator Architectures Lab, 2019-Present: Research focus on secure, high-performance memory systems, and processing in/near memory.
- Memory Architecture Lab, 2013-2019: Research focus on efficient, secure and high-performance cache and memory architectures.
- Efficient Computing Lab, 2011-2013: Research focus on energy-efficient microarchitectures, caches and memory systems.
- Ubiquitous HPC Microarchitecture Lab, 2010-2011: Research focus on low-power and high-throughput microarchitectures.
- Oregon Microarchitecture Lab, 2006-2010: Research focus on energy-efficient microarchitectures.

Graduate Research Assistant. University of Wisconsin-Madison, Department of Computer Sciences, June 2000-March 2006.

- Member of the Wisconsin Multifacet project (www.cs.wisc.edu/multifacet/) co-directed by Professors Mark D. Hill and David A. Wood.
- Participated in developing Multifacet's commercial workload simulation infrastructure.

- Studied and advocated a statistical methodology for multi-threaded workload evaluation.
- Designed and evaluated compressed cache systems for uniprocessors and chip multiprocessors for Ph.D. dissertation. Advisor: Professor David A. Wood.

Graduate Researcher. Computer Science Department, Alexandria University, Alexandria, Egypt, September 1996-July 1999

- Research Focus: Computer vision.
- Designed and compared sequential methods for recovering structure and motion of a rigid object from an image sequence for my master's dissertation. Advisor: Professor Mohamed A. Ismail.

TEACHING EXPERIENCE

Adjunct Faculty. Portland State University, Department of Electrical and Computer Engineering, September 2008-April 2018.

- Taught two graduate courses: Advanced Computer Architecture I (http://www.cecs.pdx.edu/~alaa/ece587/) and Advanced Computer Architecture II (http://www.cecs.pdx.edu/~alaa/ece588/).

Graduate Teaching Assistant. University of Wisconsin-Madison, Department of Computer Sciences, August 1999-May 2000.

- Leading discussion sections, grading and consulting for two computer science undergraduate classes.

Graduate Teaching Assistant. Alexandria University, Department of Computer Science, Alexandria, Egypt, September 1996-June 1999.

- Instructor, leading discussion sections, consulting, grading and lab supervision for many computer science undergraduate classes.

Graduate Instructor. Alexandria University, Scientific Computation Center, Alexandria, Egypt, July 1996- August 1999.

- Taught introductory computer courses (2-3 weeks per course).

OTHER WORK EXPERIENCE

System Analyst and Programmer. Alexandria University, Scientific Computation Center, Alexandria, Egypt, July 1998-March 1999.

- Designed and implemented the database system for the Spinning Testing Lab in CATGO (General Organization for Cotton Arbitration and Testing), Alexandria, Egypt using MS Access.

Undergraduate Intern. Standardata Egypt, Alexandria, Egypt, July 1995-September 1995.

- Training on Unix, C programming and screen/printer Arabic language interface programs.

Undergraduate Intern. AMAC, Alexandria, Egypt, July 1994-September 1994.

- Training on systems operation and programming in COBOL for an IBM/360-compatible system.

PUBLICATIONS

(To access these documents, please visit http://www.cs.wisc.edu/~alaa/alaa.publications.html or my Google Scholar page: https://scholar.google.com/citations?user=D3voHY0AAAAJ&hl=en&oi=ao)

JOURNAL PUBLICATIONS

1. Berkin Akin and Alaa R. Alameldeen, "A Case for Asymmetric Processing in Memory," Computer Architecture Letters, Volume 18, Issue 1, pages 22-25, January-June 2019.
2. Esha Choukse, Mattan Erez, Alaa R. Alameldeen, "CompressPoints: An Evaluation Methodology for Compressed Memory Systems," Computer Architecture Letters, Volume 17, Issue 2, pages 126-129, July-December 2018.
3. Samira Khan, Chris Wilkerson, Donghyuk Lee, Alaa R. Alameldeen, Onur Mutlu, "A Case for Memory Content-Based Detection and Mitigation of Data-Dependent Failure in DRAM," Computer Architecture Letters, Volume 16, Issue 2, pages 88-93, July-December 2017.
4. Chris Wilkerson, Alaa R. Alameldeen, and Zeshan Chishti, "Scaling the Memory Reliability Wall," Intel Technology Journal, Volume 17, Issue 1, pages 18-35, 2013.
5. Alaa R. Alameldeen, Nam Sung Kim, Samira M. Khan, Hamid Reza Ghasemi, Chris Wilkerson, Jaydeep Kulkarni, and Daniel A. Jiménez, "Improving Memory Reliability, Power, and Performance Using Mixed-Cell Designs," Intel Technology Journal, Volume 17, Issue 1, pages 36-53, 2013.

6. Alaa R. Alameldeen, "Guest Editor's Introduction: The first JILP Data Prefetching Championship," Journal of Instruction Level Parallelism, Volume 13, 2011.
7. Alaa R. Alameldeen, Zeshan Chishti, Chris Wilkerson, Wei Wu, and Shih-Lien Lu, "Adaptive Cache Design to Enable Reliable Low-Voltage Operation," IEEE Transactions on Computers Volume 60, No. 1, pages 50-63, January 2011.
8. Keith A. Bowman, Alaa R. Alameldeen, Srikanth T. Srinivasan, and Chris B. Wilkerson, "Impact of Die-to-Die and Within-Die Parameter Variations on the Clock Frequency and Throughput of Multi-Core Processors," IEEE Transactions on Very Large Scale Integration Systems, Volume 17, No. 12, pages 1679-1690, December 2009.
9. Chris Wilkerson, Hongliang Gao, Alaa R. Alameldeen, Zeshan Chishti, Muhammad Khellah and Shih-Lien Lu, "Trading off Cache Capacity for Low Voltage Operation," IEEE Micro Special Issue: Micro Top Picks from Architecture Conferences 2008, Volume 29, No. 1, pages 96-103, January-February 2009.
10. Alaa R. Alameldeen and David A. Wood, "IPC Considered Harmful for Multiprocessor Workloads," IEEE Micro, Volume 26, No. 4, pages 8-17, June-August 2006.
11. Milo M.K. Martin, Daniel J. Sorin, Bradford M. Beckmann, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood, "Multifacet's General Execution-Driven Multiprocessor Simulation (GEMS) Toolset," Computer Architecture News (CAN), September 2005.
12. Alaa R. Alameldeen and David A. Wood, "Addressing Workload Variability in Architectural Simulations," IEEE Micro Special Issue: Micro's Top Picks from Microarchitecture Conferences, Volume 23, No. 6, pages 94-98, November-December 2003. 15 of 72 submissions accepted (21%).
13. Alaa R. Alameldeen, Milo M.K. Martin, Carl J. Mauer, Kevin E. Moore, Min Xu, Daniel J. Sorin, Mark D. Hill and David A. Wood, "Simulating a $2M Commercial Server on a $2K PC," IEEE Computer, February 2003, pages 50-57.

REFEREED CONFERENCE PUBLICATIONS

14. Berkin Akin, Zeshan A. Chishti, Alaa R. Alameldeen, "ZCOMP: Reducing DNN Cross-Layer Memory Footprint Using Vector Extensions," 52nd International Symposium on Microarchitecture (MICRO-52), pages 126-138, Columbus, OH, USA, October 2019. 79 out of 344 submissions accepted (23%).
15. Jagadish B. Kotra, Haibo Zhang, Alaa R. Alameldeen, Chris Wilkerson, Mahmut T. Kandemir, "Chameleon: A Dynamically Reconfigurable Heterogenous Memory System," 51st International Symposium on Microarchitecture (MICRO-51), pages 533-545, Fukuoka, Japan, October 2018. 74 out of 351 submissions accepted (21%).
16. Esha Choukse, Mattan Erez, Alaa R. Alameldeen, "Compresso: Pragmatic Main Memory Compression," 51st International Symposium on Microarchitecture (MICRO-51), pages 546-558, Fukuoka, Japan, October 2018. 74 out of 351 submissions accepted (21%).
17. Alaa R. Alameldeen and Rajat Agarwal, "Opportunistic Compression for Direct-Mapped DRAM Caches," 4th International Symposium on Memory Systems (MEMSYS-2018), pages 129-136, Washington, D.C., USA, October 2018.
18. Samira Khan, Chris Wilkerson, Zhe Wang, Alaa R. Alameldeen, Donghyuk Lee, and Onur Mutlu, "Detecting and Mitigating Data-Dependent DRAM Failures by Exploiting Current Memory Content," 50th International Symposium on Microarchitecture (MICRO-50), pages 27-40, Boston, MA, USA, October 2017. 61 out of 327 submissions accepted (19%).
19. Elizabeth Reed, Alaa R. Alameldeen, Helia Naeimi, and Patrick Stolt, "Probabilistic Replacement Strategies for Improving the Lifetimes of NVM-Based Caches," 3rd International Symposium on Memory Systems (MEMSYS-2017), pages 166-176, Washington, D.C., USA, October 2017.
20. Jayesh Gaur, Alaa R. Alameldeen, and Sreenivas Subramoney, "Base-Victim Compression: An Opportunistic Cache Compression Architecture," 43rd Annual International Symposium on Computer Architecture (ISCA-43), pages 317-328, Seoul, South Korea, June 2016. 58 of 291 submissions accepted (20%).
21. Jaewoong Sim, Alaa R. Alameldeen, Zeshan Chishti, Chris Wilkerson, and Hyesoon Kim, "Transparent Hardware Management of Stacked DRAM as Part of Memory," 47th International Symposium on Microarchitecture (MICRO-47), pages 13-24, Cambridge, UK, Dec 2014. 53 of 273 submissions accepted (19%).
22. Samira Khan, Donghyuk Lee, Yoongu Kim, Alaa Alameldeen, Chris Wilkerson, and Onur Mutlu, "The Efficacy of Error Mitigation Techniques for DRAM Retention Failures: A Comparative Experimental Study," ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), pages 519-532, Austin, Texas, June 2014. 40 of 238 submissions accepted (17%).

23. Samira M. Khan, Alaa R. Alameldeen, Chris Wilkerson, Onur Mutlu, and Daniel A. Jiménez, "Improving Cache Performance by Exploiting Read-Write Disparity," 20th Annual International Symposium on High Performance Computer Architecture (HPCA-20), pages 452-463, Orlando, FL, USA, February 2014. 55 of 215 submissions accepted (26%).
24. Kevin Kai-Wei Chang, Donghyuk Lee, Zeshan Chishti, Chris Wilkerson, Alaa Alameldeen, Yoongu Kim, Onur Mutlu, "Improving DRAM Performance by Parallelizing Refreshes with Accesses," 20th Annual International Symposium on High Performance Computer Architecture (HPCA-20), pages 356-367, Orlando, FL, USA, February 2014. 55 of 215 submissions accepted (26%).
25. Samira M. Khan, Alaa R. Alameldeen, Chris Wilkerson, Jaydeep Kulkarni, and Daniel A. Jiménez, "Improving Multi-Core Performance Using Mixed-Cell Cache Architecture," 19th Annual International Symposium on High Performance Computer Architecture (HPCA-19), pages 119-130, Shenzhen, China, February 2013. 51 of 249 submissions accepted (20%).
26. Amr Helmy and Alaa R. Alameldeen, "Redundancy and ECC Mechanisms to Improve Energy Efficiency of On-Die Interconnects," 3rd International Conference on Energy-Aware Computing, pages 1-6, METU NCC, Cyprus, December 2012.
27. Alaa R. Alameldeen, Ilya Wagner, Zeshan Chishti, Wei Wu, Chris Wilkerson, and Shih-Lien Lu, "Energy-Efficient Cache Design Using Variable-Strength Error-Correcting Codes," 38th Annual International Symposium on Computer Architecture (ISCA-38), pages 461-471, San Jose, CA, June 2011. 40 of 208 submissions accepted (19%).
28. Shih-Lien Lu, Alaa R. Alameldeen, Keith Bowman, Zeshan Chishti, Chris Wilkerson, and Wei Wu, "Architectural-Level Error-Tolerant Techniques for Low Supply Voltage Cache Operation," 2011 IEEE International Conference on IC Design & Technology (ICICDT 2011), pages 1-5, Kaohsiung, Taiwan, May 2011.
29. Chris Wilkerson, Alaa R. Alameldeen, Zeshan Chishti, Wei Wu, Dinesh Somasekhar, and Shih-Lien Lu, "Reducing Cache Power with Low-Cost, Multi-Bit Error-Correcting Codes," 37th Annual International Symposium on Computer Architecture (ISCA-37), pages 83-93, Saint Malo, France, June 2010. 44 of 245 submissions accepted (18%).
30. Zeshan Chishti, Alaa R. Alameldeen, Chris Wilkerson, Wei Wu, and Shih-Lien Lu, "Improving Cache Lifetime Reliability at Ultra-Low Voltages," 42nd Annual International Symposium on Microarchitecture (MICRO-42), pages 89-99, New York City, NY, USA, December 2009. 52 of 209 submissions accepted (25%).
31. Chris Wilkerson, Hongliang Gao, Alaa R. Alameldeen, Zeshan Chishti, Muhammad Khellah and Shih-Lien Lu, "Trading off Cache Capacity for Reliability to Enable Low Voltage Operation," 35th Annual International Symposium on Computer Architecture (ISCA-35), pages 203-214, Beijing, China, June 2008. 37 of 259 submissions accepted (14%).
32. Keith A. Bowman, Alaa R. Alameldeen, Srikanth T. Srinivasan, and Chris B. Wilkerson, "Impact of Die-to-Die and Within-Die Parameter Variations on Throughput Distribution of Multi-Core Processors," International Symposium on Low Power Electronics and Design (ISLPED), pages 50-55, Portland, Oregon, USA, August 2007.
33. Alaa R. Alameldeen and David A. Wood, "Interactions Between Compression and Prefetching in Chip Multiprocessors," 13th Annual International Symposium on High Performance Computer Architecture (HPCA-13), pages 228-239, Phoenix, Arizona, USA, February 2007. 28 of 174 submissions accepted (16%).
34. Alaa R. Alameldeen and David A. Wood, "Adaptive Cache Compression for High-Performance Processors," 31st Annual International Symposium on Computer Architecture (ISCA-31), Munich, Germany, June 2004, pages 212-223. 31 of 217 submissions accepted (14%).
35. Alaa R. Alameldeen and David A. Wood, "Variability in Architectural Simulations of Multi-threaded Workloads," 9th Annual International Symposium on High Performance Computer Architecture (HPCA-9), Anaheim, California, USA, February 2003, pages 7-18. 31 of 141 submissions accepted (22%).
36. Ashraf Aboulnaga, Alaa R. Alameldeen and Jeffrey F. Naughton, "Estimating the Selectivity of XML Path Expressions for Internet Scale Applications," 27th International Conference on Very Large Data Bases (VLDB), Rome, Italy, September 2001, pages 591-600. 59 of 339 submissions accepted (17%).
37. Milo M. K. Martin, Daniel J. Sorin, Anastassia Ailamaki, Alaa R. Alameldeen, Ross M. Dickson, Carl J. Mauer, Kevin E. Moore, Manoj Plakal, Mark D. Hill, and David A. Wood, "Timestamp Snooping: An Approach for Extending SMPs," 9th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-IX), Boston, Massachusetts, USA, November 2000, pages 25-36. 24 of 114 submissions accepted (21%).

38. Alaa R. Alameldeen and M. A. Ismail, "Sequential Methods for Recovering Structure and Motion of a Rigid Object from an Image Sequence," In Proc. CVPRIP'2000, Atlantic City, New Jersey, USA, February-March 2000.

REFEREED WORKSHOP PUBLICATIONS

39. Alaa R. Alameldeen, Carl J. Mauer, Min Xu, Pacia J. Harper, Milo M.K. Martin, Daniel J. Sorin, Mark D. Hill and David A. Wood, "Evaluating Non-deterministic Multi-threaded Commercial Workloads," 5th Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW-02), Cambridge, MA, February 2002, pages 30-38.

NON-REFEREED PUBLICATIONS

40. Alaa R. Alameldeen, "Using Compression to Improve Chip Multiprocessor Performance," Ph.D. dissertation, Computer Sciences Department, University of Wisconsin-Madison, Madison, Wisconsin, USA, March 2006.
41. Alaa R. Alameldeen and David A. Wood, "Frequent Pattern Compression: A Significance-Based Compression Scheme for L2 Caches," Department of Computer Sciences Technical Report CS-TR-2004-1500, April 2004.
42. Alaa R. Alameldeen, "Sequential Methods for Recovering Structure and Motion of a Rigid Object from an Image Sequence," M.Sc. dissertation, Department of Computer Science and Automatic Control, Faculty of Engineering, Alexandria University, Alexandria, Egypt, July 1999.

PATENTS

1. Zhe Wang, Zeshan A. Chishti, Muthukumar P. Swaminathan, Alaa R. Alameldeen, Kunal A. Khochare, Jason A. Gayman, "Apparatus, system, and method to determine a demarcation voltage to use to read a non-volatile memory," US Patent 10,452,312, October 22, 2019.
2. Zhe Wang, Zeshan A. Chishti, Alaa R. Alameldeen, and Rajat Agarwal, "Near memory miss prediction to reduce memory access latency," US Patent 10,417,135, September 17, 2019.
3. Zhe Wang, Chris Wilkerson, Zeshan A. Chishti, Seth H. Pugsley, Alaa R. Alameldeen, and Shih-Lien Lu, "Method and apparatus for unneeded block prediction in a computing system having a last level cache and a multi-level system memory," US Patent 10,261,901, April 16, 2019.
4. Zhe Wang, Chris Wilkerson, Zeshan A. Chishti, Seth H. Pugsley, Alaa R. Alameldeen, and Shih-Lien Lu, "Method and apparatus for pre-fetching data in a system having a multi-level system memory," US Patent 10,108,549, October 23, 2018.
5. Alaa R. Alameldeen, Glenn J. Hinton, Blaise Fanning, and James J. Greensky, "Replacement of a Block with a Compressed Block to Increase Capacity of a Memory-Side Cache," US Patent 10,048,868, August 14, 2018.
6. Chris Wilkerson, Alaa R. Alameldeen, Zeshan Chishti, and Jaewoong Sim, "Method and Apparatus for Implementing a Heterogeneous Memory Subsystem," US Patent 9,921,972, March 20, 2018.
7. Alaa R. Alameldeen, Chris Wilkerson, Eugene Gorbatov, and Zeshan Chishti, "System and Method for Thread Scheduling on Reconfigurable Processor Cores," US Patent 9,703,708, July 11, 2017.
8. Chris Wilkerson, Alaa R. Alameldeen, Zhe Wang, and Zeshan Chishti, "Multi-Level Memory Management," US Patent 9,583,182, February 28, 2017.
9. Chris Wilkerson, Alaa R. Alameldeen, Zeshan A. Chishti, and Jaewoong Sim, "Method and Apparatus for Implementing a Heterogeneous Memory Subsystem," US Patent 9,472,248, October 18, 2016.
10. Chris Wilkerson, Alaa R. Alameldeen, Eugene Gorbatov, and Zeshan A. Chishti, "Systems and Methods for Managing Reconfigurable Processor Cores," US Patent 9,417,879, August 16, 2016.
11. Tingting Sha, Chris Wilkerson, Herbert Hum, and Alaa R. Alameldeen, "Compiler Assisted Low Power and High Performance Load Handling Based on Load Types," US Patent 9,311,085, April 12, 2016.
12. Alaa R. Alameldeen, Niranjan L. Cooray, Jayesh Gaur, Steven D. Pudar, Manuel A. Aguilar Arreola, Margareth E. Marrugo, and Chinnakrishnan Ballapuram, "Cache Memory Data Compression and Decompression," US Patent 9,292,449, March 22, 2016.
13. Sreenivas Subramoney, Jayesh Gaur, and Alaa R. Alameldeen, "Data Compression in Processor Caches," US Patent 9,251,096, February 2, 2016.
14. Alaa R. Alameldeen, Chris Wilkerson, and Samira M. Khan, "Read-Write Partitioning of Cache Memory," US Patent 9,233,710, December 29, 2015.
15. Chris Wilkerson, Alaa R. Alameldeen, and Shih-Lien Lu, "Selective Error Correction in Memory to Reduce Power Consumption," US Patent 8,966,345, February 25, 2015.

16. Muhammad M. Khellah, Chris Wilkerson, Alaa R. Alameldeen, Bibiche M. Geuskens, Tanay Karnik, Vivek De, and Gunjan H. Pandya, "Reducing Minimum Operating Voltage through Hybrid Cache Design," US Patent 8,868,836, October 21, 2014.
17. Alaa R. Alameldeen, Ilya Wagner, Zeshan A. Chishti, Wei Wu, and Chris Wilkerson, "Dynamically Allocatable Memory Error Mitigation," US Patent 8,806,285, August 12, 2014.
18. Chris Wilkerson, Alaa R. Alameldeen, and Jaydeep P. Kulkarni, "Adaptive Self-Repairing Cache," US Patent 8,719,502, May 6, 2014.
19. Chris Wilkerson, Alaa R. Alameldeen, Zeshan A. Chishti, Dinesh Somasekhar, Wei Wu, and Shih-Lien Lu, "Method and Apparatus for Using Cache Memory in a System that Supports a Low Power State," US Patent 8,640,005, January 28, 2014.
20. Alaa R. Alameldeen and Zeshan A. Chishti, "Hardware Support for Thread Scheduling on Multi-Core Processors," US Patent 8.276,142, September 25, 2012.
21. Zeshan A. Chishti, Alaa R. Alameldeen, Chris Wilkerson, Wei Wu, Dinesh Somasekhar, Muhammad Khellah, and Shih-Lien Lu, "Performing Multi-Bit Error Correction on a Cache Line," US Patent 8,245,111, August 14, 2012.
22. David A. Wood and Alaa R. Alameldeen, "Adaptive Cache Compression System," US Patent 7,412,564, August 12, 2008.

INVITED AND CONFERENCE TALKS

Moderator Introduction: Is Processing In/Near Memory Worth the Effort?
- 5th Workshop on Computer Architecture Research Directions (CARD-5) with ISCA-2019, Phoenix, Arizona, June 2019.

Chameleon: A Dynamically Reconfigurable Heterogenous Memory System
- 51st International Symposium on Microarchitecture (MICRO-51), Fukuoka, Japan, October 2018.

Opportunistic Compression for Direct-Mapped DRAM Caches
- 4th International Symposium on Memory Systems, Washington, D.C., USA, October 2018.

Probabilistic Replacement Strategies for Improving the Lifetimes of NVM-Based Caches
- 3rd International Symposium on Memory Systems, Washington, D.C., USA, October 2017.

Keynote Address: Near-Threshold Computing: How Close Should We Get?
- 2nd Workshop on Near-Threshold Computing (with ISCA-41), Minneapolis, Minnesota, USA, June 2014.

Energy-Efficient Cache Design Using Variable-Strength Error-Correcting Codes
- 38th International Symposium on Computer Architecture (ISCA-38), San Jose, California, USA, June 2011.

Improving Cache Lifetime Reliability at Ultra-Low Voltages
- 42nd International Symposium on Microarchitecture (MICRO-42), New York City, New York, USA, December 2009.

Interactions between Compression and Prefetching in Chip Multiprocessors
- 13th International Symposium on High Performance Computer Architecture (HPCA-13), Phoenix, Arizona, USA, February 2007.

Cores, Caches, and Compression in Chip Multiprocessors
- Purdue University, West Lafayette, Indiana, USA, April 2005.
- Intel, Hudson, Massachusetts, USA, August 2005.
- Intel, Santa Clara, California, USA, September 2005.
- Intel, Hillsboro, Oregon, USA, September 2005.
- AMD, Sunnyvale, California, USA, September 2005.

GEMS: Multifacet's General Execution-Driven Multiprocessor Simulator
- Tutorial at the 32nd International Symposium on Computer Architecture (ISCA-32), June 2006 (with Michael R. Marty, Bradford M. Beckmann, Luke Yen, Min Xu and Kevin E. Moore).

Adaptive Cache Compression for High Performance Processors
- 31st International Symposium on Computer Architecture (ISCA-31), Munich, Germany, June 2004.
- 9th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, Wisconsin, USA, October 2004.

Using Cache Compression to Improve CMP Performance
- 8th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, Wisconsin, USA, October 2004.

Simulating a $2M Commercial Server on a $2K PC

- Intel Labs, Hillsboro, Oregon, USA, March 2003.

Variability in Architectural Simulations of Multi-threaded Workloads

- Intel Labs, Hillsboro, Oregon, USA, March 2003.
- 9th International Symposium on High Performance Computer Architecture (HPCA-9), Anaheim, California, USA, February 2003.
- 7th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, Wisconsin, USA, October 2002.

Sequential Methods for Recovering Structure and Motion of a Rigid Object from an Image Sequence

- International Conference on Computer Vision, Pattern Recognition and Image Processing (CVPRIP'2000), Atlantic City, New Jersey, USA, March 2000.

HONORS AND AWARDS

- Divisional Recognition Award, Architecture and Design Research, Intel Labs, 2019.
- Divisional Recognition Award, Architecture and Design Research, Intel Labs, 2018.
- Divisional Recognition Award, Product Architecture Group, Platform Engineering Group, Intel Corporation, 2017.
- Divisional Recognition Award, Architecture and Design Research, Intel Labs, 2015.
- Ranked 1st on the Dept. of Computer Science and Automatic Control students during the academic years 1992-1993 to 1995-1996.
- Ranked 1st on the faculty of engineering students during the academic year 1991-1992 and upon graduation in the academic year 1995-1996 (B.Sc.).
- Awarded the Prof. Abdelsamie Mustafa prize for the top student of the Faculty of Engineering in 1996.
- Awarded the Prof. Naim Abou Taleb prize for the top student of the Dept. of Computer Science and Automatic Control in 1996.
- Ranked 8th on the Mathematics section high school students in Egypt upon graduation.

PROFESSIONAL ACTIVITIES AND SERVICE

- Organizing Committee Chair, JILP Workshop on Data Prefetching: Data Prefetching Championship (with HPCA-2009), February 2009.
- Program Committee Chair, Industry Track at the 26th International Symposium on High-Performance Computer Architecture (HPCA-2020), February 2020.
- Workshop Chair, 39th International Symposium on Computer Architecture (ISCA-39), Portland, OR, June 2012.
- Organizing Committee member, 1st JILP Workshop on Computer Architecture Competitions (JWAC-1): Cache Replacement Championship (with ISCA 2010), June 2010.
- Organizing Committee member, 2nd JILP Workshop on Computer Architecture Competitions (JWAC-2): Championship Branch Prediction (with ISCA 2011), June 2011.
- Organizing Committee member, 4th JILP Workshop on Computer Architecture Competitions (JWAC-4): Championship Branch Prediction (with ISCA 2014), June 2014.
- Organizing Committee member, 5th JILP Workshop on Computer Architecture Competitions (JWAC-5): Data Prefetching Championship (with ISCA 2015), June 2015.
- Organizing Committee member, 7th JILP Workshop on Computer Architecture Competitions: Second Cache Replacement Championship (with ISCA 2017), June 2017.
- Serving on the steering committee for the JILP Workshop on Architecture Competitions.
- Served on NSF review panels.
- Guest editor for the JILP Special Issue on Data Prefetching, 2011.
- Program Committee Member for the 2020 International Symposium on High-Performance Computer Architecture (HPCA-2020), 2019 International Symposium on Computer Architecture (ISCA-2019), 2019 International Symposium on High-Performance Computer Architecture (HPCA-2019), 2019 International Parallel and Distributed Processing Symposium (IPDPS-2019), 2018 International Symposium on High-Performance Computer Architecture (HPCA-2018), 2017 International Symposium on Microarchitecture (MICRO-2017), 2017 IEEE Micro Special Issue on "Micro's Top Picks from 2016 Computer Architecture Conferences," 2015 International Symposium on Microarchitecture (MICRO-2015), IEEE International

Symposium on Workload Characterization (IISWC-2015), 2015 International Symposium on Performance Analysis of Systems and Software (ISPASS-2015), Workshop on Near-Threshold Computing (with ISCA-2014), 2014 Workshop on Computer Architecture Competitions (CPB-4, with ISCA 2014), 2014 International Symposium on Performance Analysis of Systems and Software (ISPASS-2014), 26th International Parallel and Distributed Processing Symposium (IPDPS 2012), 1st JILP Workshop on Computer Architecture Competitions (JWAC-1, with ISCA 2010), 2nd JILP Workshop on Computer Architecture Competitions (JWAC-2, with ISCA 2011), 2nd International Forum on Next-generation MultiCore/ManyCore Technologies (IFMT'10, with ISCA 2010), 5th Annual Workshop on Modeling, Benchmarking and Simulation (MoBS, with ISCA 2009), JILP Workshop on Data Prefetching (DPC-1, with HPCA 2009), and 1st International Forum on Next-generation MultiCore/ManyCore Technologies (IFMT'2008).

- Reviewer for the International Symposium on Computer Architecture (ISCA), International Symposium on High-Performance Computer Architecture (HPCA), International Symposium on Microarchitecture (MICRO), ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), International Symposium on Low Power Electronics and Design (ISLPED), International Conference on Parallel and Distributed Systems (ICPADS), VLSI Design Conference, IEEE Micro, IEEE Transactions on Computers, IEEE Transactions on CAD, IEEE Transactions on VLSI Systems, IEEE Transactions on Dependable and Secure Computing, IEEE Computer Architecture Letters (CAL), ACM Transactions on Architecture and Code Optimization, and ACM Transactions on Computer Systems.
- Member of the ACM, the IEEE and the IEEE Computer Society since 2006 (Student Member 2000-2006).
- Member of ACM Special Interest Group on Computer Architecture (SIGARCH), ACM Special Interest Group on Microarchitecture (SIGMICRO), IEEE Technical Committee on Computer Architecture (TCCA), Technical Committee on Microprocessors and Microcomputers (TCMCOMP), Technical Committee on Microprogramming and Microarchitecture (TCUARCH), Technical Committee on Simulation (TCSIM), Technical Committee on Pattern Analysis and Machine Intelligence (TCPAMI).
- Organizer of the Computer Architecture Seminar at the University of Wisconsin-Madison, Spring 2003.

REFERENCES

Available upon request.