

Guoliang Jin

Department of Computer Sciences
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Research Interest

Software reliability. Especially in concurrent software.

Education

University of Wisconsin-Madison (2007.9-present)

Ph.D. Student at Department of Computer Sciences

University of Science and Technology of China (2003.9-2007.7)

B.Eng. in Computer Science and Technology, Departmental Ranking: 1/128

Publications

Automated Atomicity-Violation Fixing

Guoliang Jin, Linhai Song, Wei Zhang, Shan Lu, Ben Liblit.

32nd ACM SIGPLAN conference on Programming Language Design and Implementation (PLDI'10).

ConSeq: Detecting Concurrency Bugs through Sequential Errors

Wei Zhang, Junghee Lim, Ramya Olichandran, Joel Scherpelz, Guoliang Jin, Shan Lu, Thomas Reps.

16th International Conference on Architecture Support for Programming Languages and Operating Systems 2011 (ASPLOS'11).

Instrumentation and Sampling Strategies for Cooperative Concurrency Bug Isolation

Guoliang Jin, Aditya Thakur, Ben Liblit, and Shan Lu.

International Conference on Object-Oriented Programming, Systems, Languages & Applications 2010 (OOPSLA'10).

Experience

RA for Professor Shan Lu, UW-Madison (2009.1-present)

Working on concurrent program reliability issue. Developing tools to handle atomicity violations. Developing low-overhead monitoring and failure diagnosis techniques suitable for multi-threaded applications in production environment. Surveying real concurrent bugs and corresponding fixes.

TA for CS 537 Introduction to Operating Systems, UW-Madison (2008.9-2009.5)

TA for CS 302 Introduction to Programming, UW-Madison (2008.1-2008.5)

RA for MRNet project, UW-Madison (2007.9-2008.5)

MRNet is a Tree Base Overlay Network for parallel computing.

Implemented a GUI called A1 for MRNet using gtkmm to show the node structure in the network.

Added performance measurement functionality to MRNet and the GUI.

TA for CS/ECE 252 Introduction to Computer Engineering, UW-Madison (2007.9-2007.12)

RA for Computer Principles and Interface Lab, USTC (2006.7-2007.6)

Implemented a LCD controller for the Computer Architecture Experiment Platform.

Implemented the ADC and DAC modules for the Logical Simulation System of Computer Principles Experiment Platform.

Skill Set

C/C++, LLVM, OCaml/CIL, Shell script, Python, Java, Erlang.