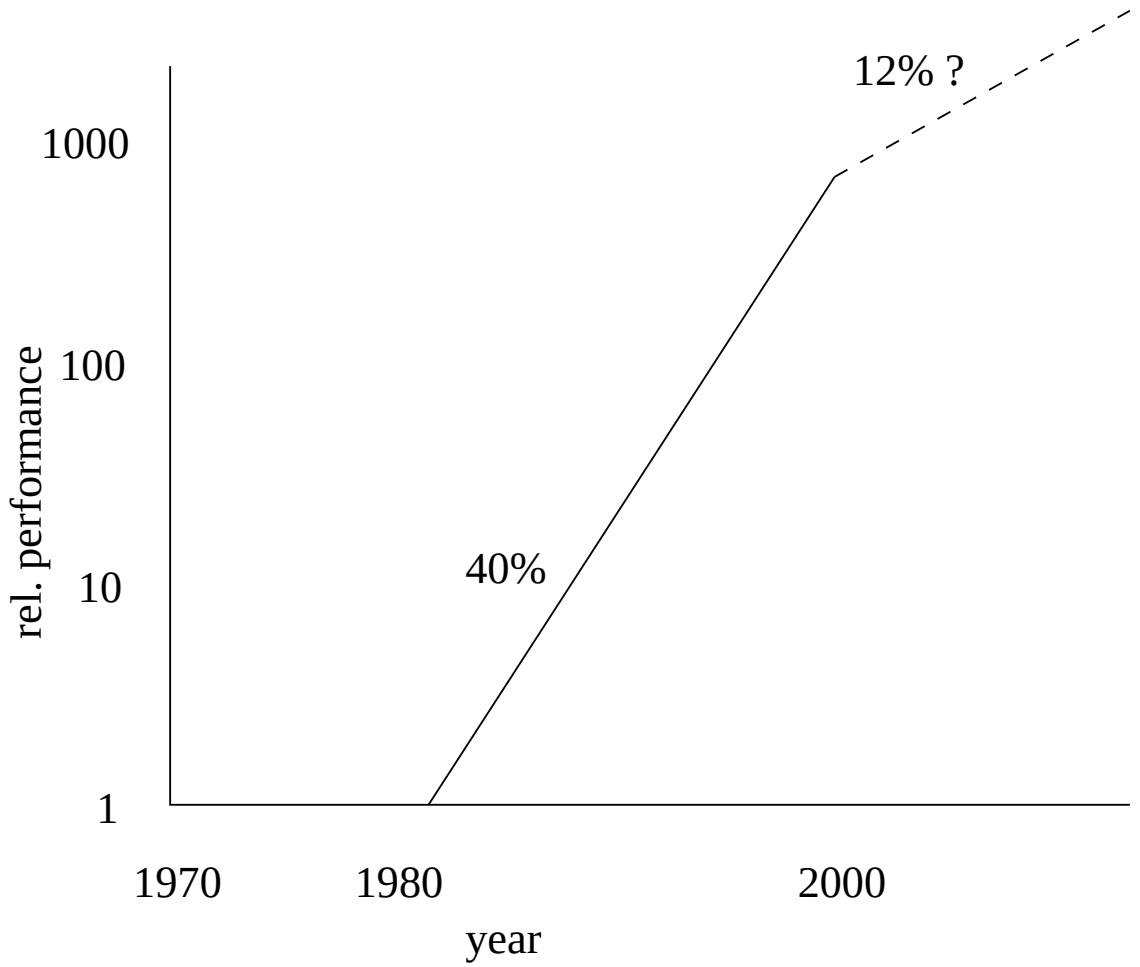
Uniprocessor Performance Improvement

Consider Microprocessors



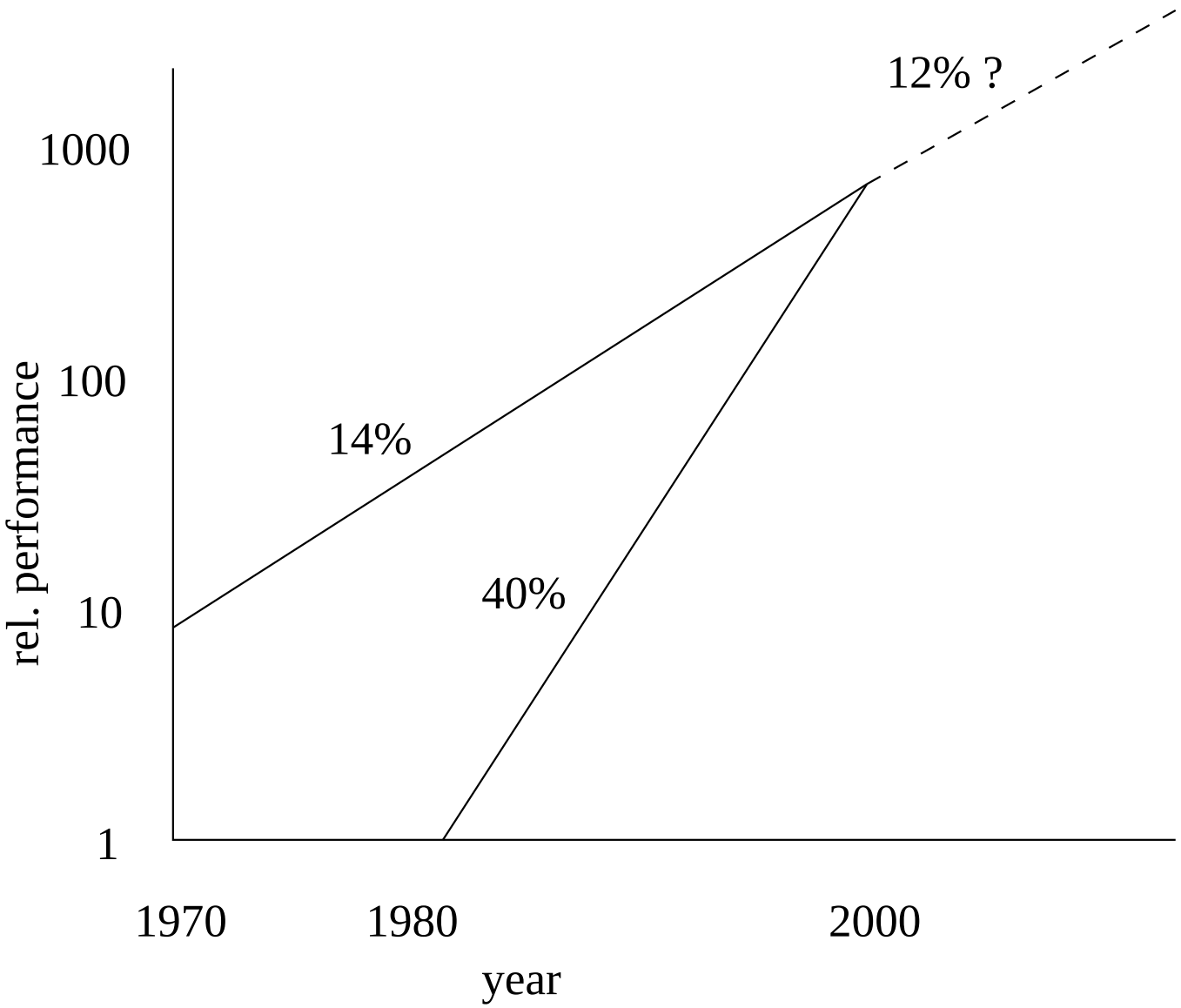
But

-- micro technology has not always been dominant

-- ILP was known long before microprocessors

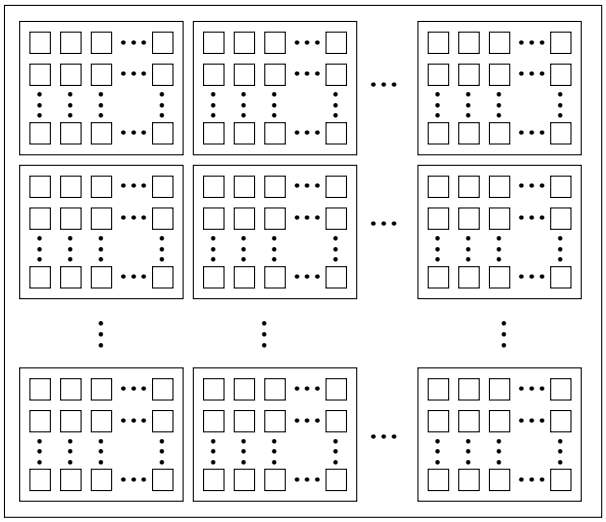
Uniprocessor Performance Improvement

Best Uniprocessor Performance

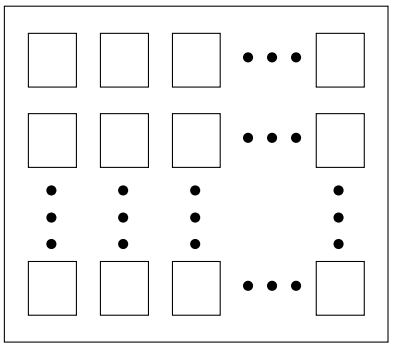


Computer Evolution

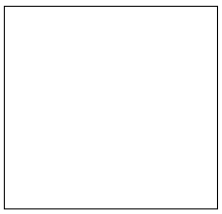
from a packaging perspective



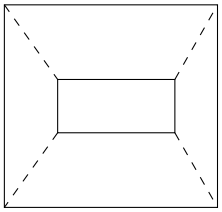
Mainframe



Minicomputer



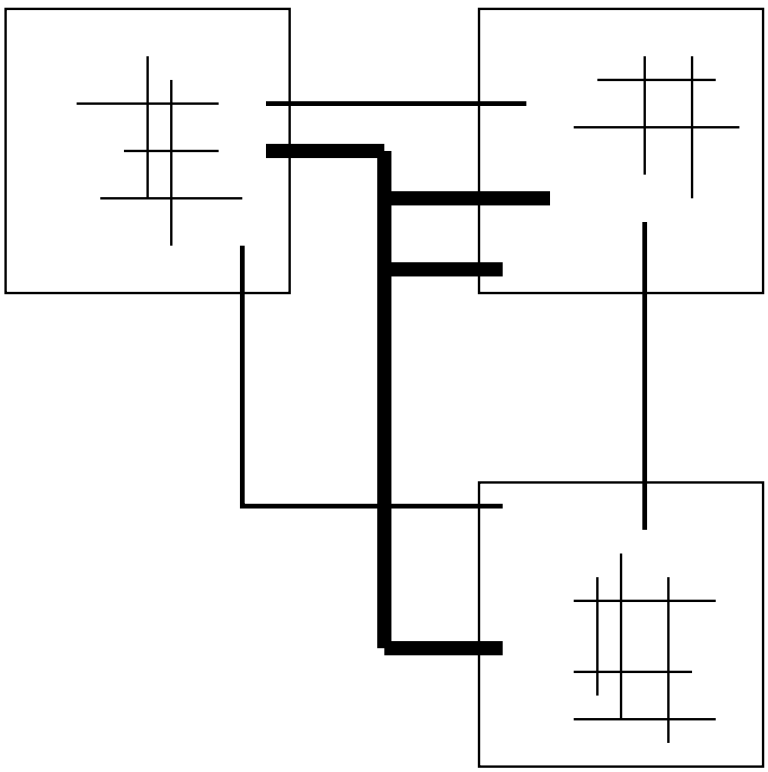
Microprocessor



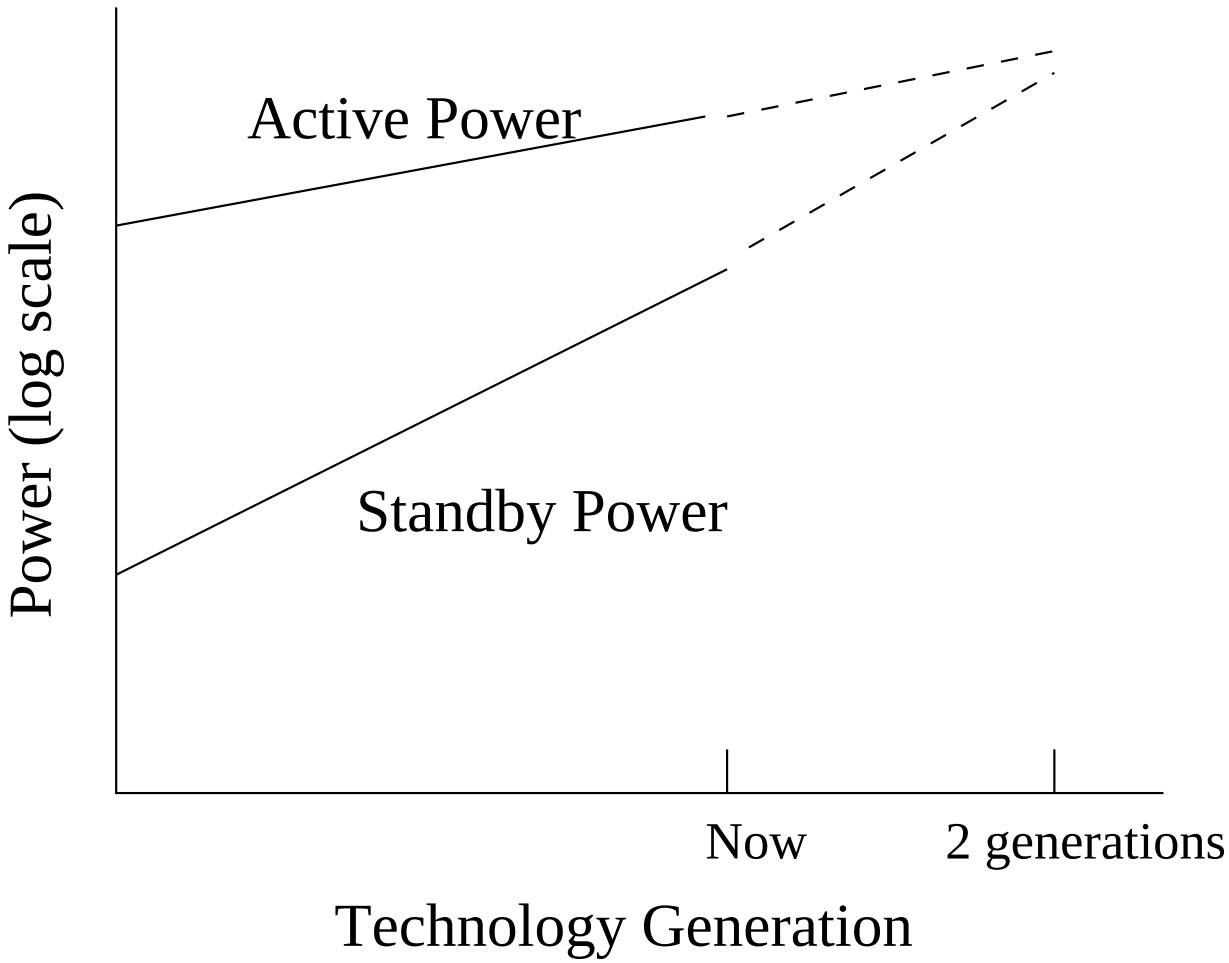
Core processor

Future Processors: Wires

- Local wires: congestion
- Global wires: delay
- Global multi-buses: very bad delay



Future Processors: Power



adapted from Intel data

Future Processors: Clocks

-- *we may have seen the high water mark in IPC*

- Fast clocks
  - -- one sure way of improving overall perf.
  - -- one key to S. Cray's success
  - -- evident in Pentium evolution

P5 5 stages

Pref	Dec 1	Dec 2	Exec	Wrt Bck

P6 12 stages

F1	F2	D1	D2	D3	Rn	ROB	Rdy/Sch	Disp	Ex	Ret1	Ret2

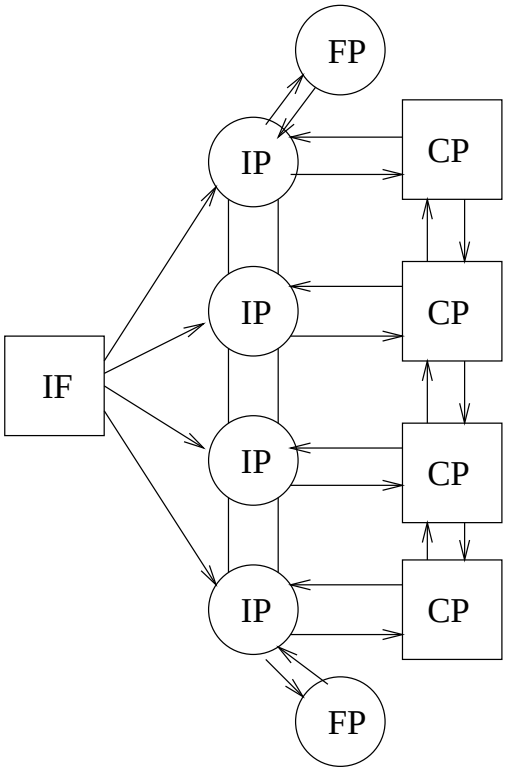
Willamette 20 stages

IP1	IP2	TC1	TC2	Dr	Al	Rn	Q	S1	S2	S3	Dp1	Dp2	R1	R2	Ex	Flgs	Br

Implications: Microarchitecture

--Instruction Level Distributed Processing (ILDP) will replace Instruction Level Parallelism

- Point-to-point global interconnects
- Units with few transistors running very fast
- Amenable to multiple clock domains
- Little speculation (only br. predict and caches)
- Determinism is better than arbitration



Implications: ISA

--*We need new ISAs*

- Focus on *communication* and *dependence*
  NOT computation and *independence*
  accumulator or stack-based
- Small instruction footprint
  variable length instructions?

Example ISA

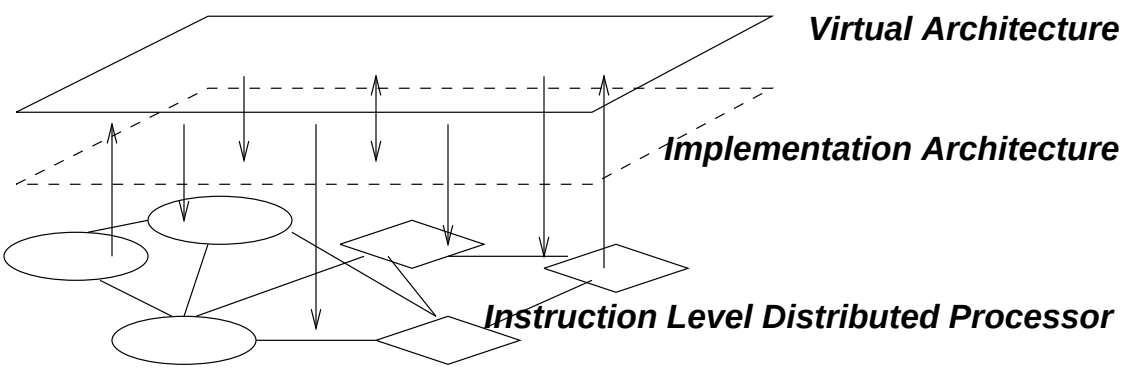
- Consider an accumulator-based ISA
- Perhaps 64 GPRs
- Implementation in clusters each w/ Accumulator
- Intra-cluster communication via Accumulator
- Inter-cluster communication via GPRs

```
R <- A                1 byte
A <- R                1 byte
A <- A op R           2 bytes
A <- A op imm         4 bytes
A <- M(R op imm)      4 bytes
M(R op imm) <- A      4 bytes
R <- M(A op imm)      4 bytes
```

etc.

Enabler: Co-Designed Virtual Machines

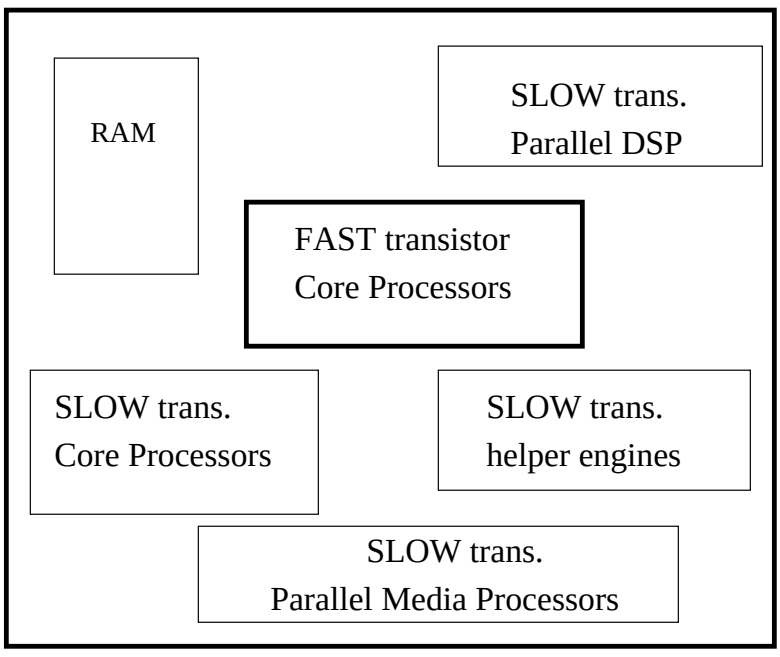
-- *Give hardware implementors a layer of software*



- Gives designers more flexibility for managing distributed processor resources
- Allows new implementation ISAs
- Allows higher level dynamic optimization

  examples: IBM System 38, AS/400; Daisy; Transmeta

Chip Architecture

--*Cores may become a solved problem*

- Few fast transistors/emphasis on fast clock
  => fewer opportunities for complications
- Emphasis will shift to chip architecture
- Remove high ILP media/DSP functions from core
  (into slow parallel transistors?)
- Perf optimization with slow helper threads
- VM optimization threads timeshare fast transistors
  or space share on slower core processors