

BRADFORD M. BECKMANN

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Objective

To obtain a challenging job designing or researching digital systems such as chip multiprocessors or media processors.

Education

Ph. D. Computer Science, July 2006 (expected).

University of Wisconsin-Madison, Madison, Wisconsin.

Advisor: Prof. David A. Wood

Dissertation Title: Utilizing Transmission Lines in CMP Caches

M.S. Computer Science, May 2002.

University of Wisconsin-Madison, Madison, Wisconsin.

G.P.A.: 3.89/4.0.

B.S. Electrical Engineering, June 2000.

University of Cincinnati, Cincinnati, Ohio.

G.P.A.: 3.96/4.0 (summa cum laude).

Research Experience

Research Assistant, May 2001 – current

Department of Computer Science, University of Wisconsin-Madison. Madison, Wisconsin

- Member of the Wisconsin Multifacet project (www.cs.wisc.edu/multifacet/) co-directed by Professors Mark D. Hill and David A. Wood.
- Co-developing Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) and providing support for its 380 registered users.
- Researching micro-architecture mechanisms to exploit novel low-latency interconnection networks to create high performance, energy efficient CMP caches.

Work Experience

Teaching Assistant, Sept. 2000 – May 2001

Department of Computer Science, University of Wisconsin-Madison. Madison, Wisconsin

- Assisted with the VLSI System Design graduate course, and created tutorials and class presentations to assist student learning of the Mentor Graphic tool package. Also graded homework assignments and answered student questions.
- Taught four half-semester sections of the Elementary Programming undergraduate course. Created notes and lesson plans to teach students the fundamentals of C++ programming and evaluated their performance by constructing original quizzes and assignments.

VLSI Design Intern, March – Sept., 1998 and 1999

Digital/Compaq Computer Corporation. Shrewsbury, Massachusetts

- Worked for the Alpha Advanced Development Group designing the 21464 microprocessor.
- Designed five unique schematics and verified them utilizing various CAD analysis tools. Created SPICE critical-path simulations, defined micro-architecture pipeline, and gave a presentation on the negative effects of back-gate coupling and charge-pumping.

Product and Test Intern, April – Sept. 1997

Digital Semiconductor. Hudson, Massachusetts

- Worked for the Alpha Product and Test Group testing the 21264 microprocessor.
- Dissected and documented the processor's cache repair system. Also designed and debugged hardware used to test Alpha processors.

Publications

(To access these documents, visit <http://www.cs.wisc.edu/~beckmann/>)

Balancing Capacity and Latency in CMP Caches. **Bradford M. Beckmann**, Michael R. Marty, and David A. Wood. University of Wisconsin-Madison Computer Sciences Technical Report CS-TR-2006-1554, February 2006.

Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) Toolset. Milo M. K. Martin, Daniel J. Sorin, **Bradford M. Beckmann**, Michael R. Marty, Min Xu, Alaa R. Alameldeen, Kevin E. Moore, Mark D. Hill, and David A. Wood. SIGARCH Computer Architecture News (**CAN**), Volume 22, Number 4, September 2005.

Managing Wire Delay in Large Chip-Multiprocessor Caches. **Bradford M. Beckmann** and David A. Wood, Proceedings of the 37th International Symposium on Microarchitecture (**MICRO**), December 2004. 29 of 158 submissions accepted (18%).

TLC: Transmission Line Caches. **Bradford M. Beckmann** and David A. Wood, Proceedings of the 36th International Symposium on Microarchitecture (**MICRO**), December 2003. 34 of 134 submissions accepted (25%).

Tutorials

GEMS: Multifacet's General Execution-driven Multiprocessor Simulator, Michael R. Marty, **Bradford M. Beckmann**, Luke Yen, Alaa R. Alameldeen, Min Xu, and Kevin Moore Tutorial at the 32nd International Symposium on Computer Architecture (**ISCA**), June 2005.

Talks

Balancing Capacity and Latency in CMP Caches

- 10th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, Oct. 2005

Managing Wire Delay in CMP Caches

- 37th International Symposium on Microarchitecture, Portland, OR, Dec. 2004
- 9th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, Oct. 2004

TLC: Transmission Line Caches

- 36th International Symposium on Microarchitecture, San Diego, CA, Dec. 2003
- 8th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, Oct. 2003

The Cost and Benefits of On-chip Transmission Lines

- 7th Annual Wisconsin Architecture Industrial Affiliates Meeting, Madison, WI, Oct. 2002

The Negative Effects of Back-gate Coupling and Charge Pumping on Dynamic Circuits

- Compaq Technical Presentation, Shrewsbury, MA, Sept. 1998.

Skills

- Engineering: microarchitecture, static and dynamic CMOS circuit design and simulation, logic design and simulation, device physics and modeling, electromagnetic wave transmission
- Computer Science: compilers, operating systems, analytic modeling
- Programming: C/C++, Pascal, assembly (x86, SPARC), Python, VHDL, shell scripting
- Tools: Simics, SimpleScalar, Mentor Graphics, SPICE

References

Available Upon Request.