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RESEARCH INTERESTS

(Interests: Program analysis and verification, abstract interpretation, static analysis of executables.)
My research interests broadly span programming languages and compilers. Specifically, I am interested in program analysis and verification problems based on abstract interpretation and static analysis. For my Ph.D. dissertation, I developed static-analysis algorithms to address the problem of analyzing executables without debugging information.

EDUCATION

- Aug 2007 **Ph.D. (Computer Science)**
University of Wisconsin, Madison, USA
Advisor: Prof. Thomas. W. Reps
Thesis: "WYSINWYX: **W**hat **Y**ou **S**ee **I**s **N**ot **W**hat **Y**ou **eX**ecute"
(Static Analysis of Executables)
- May 2003 **M.S. (Computer Science)**
University of Wisconsin, Madison, USA
- May 2001 **B.E. (Computer Science and Engineering)**
College of Engineering Guindy
Anna University, Chennai, India

RESEARCH AND WORK EXPERIENCE

- Oct 2007 - Present **Research Staff Member** NEC Laboratories Inc., Princeton, NJ, USA
Aug 2001 - Aug 2007 **Research Assistant** University of Wisconsin, Madison, WI, USA

AWARDS AND DISTINCTIONS

- 2008 Outstanding Graduate Research Award (UW Computer Sciences Department)
2004 EAPLS Best Paper Award at ETAPS 2004 (with T. Reps)

PUBLICATIONS

Thesis

- Balakrishnan, G., **WYSINWYX: What You See Is Not What You eXecute**, Ph.D. dissertation (TR-1603), Computer Sciences Department, University of Wisconsin, Madison, WI, August 2007.

Conference Publications

- Balakrishnan, G., Sankaranarayanan, S., Ivancic, F., and Gupta, A., Refining the Control Structure of Loops using Static Analysis, In *Proc. Conf. on Embedded Software (EMSOFT)*, Oct 2009.
- Balakrishnan, G., Ganai, Malay., **PED: Proof-guided Error Diagnosis by Triangulation of Program Error Causes**, In *Proc. Software Engineering and Formal Methods (SEFM)*, Nov 2008.
- Balakrishnan, G., Sankaranarayanan, S., Ivancic, F., Wei, O., and Gupta, A., **SLR: Path-Sensitive Analysis Through Infeasible-Path Detection and Syntactic-Language Refinement**. In *Proc. Static Analysis Symposium (SAS)*, Jul 2008 .
- Balakrishnan, G. and Reps, T., **Analyzing Stripped Device-Driver Executables**, In *Proc. 14th Int Conf. on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, Mar. 2008.
- Balakrishnan, G. and Reps, T., **Recency-Abstraction for Heap-Allocated Storage**. In *Proc. 13th Static Analysis Symposium (SAS)*, pages 221-239, Aug. 2006.
- Balakrishnan, G., Reps, T., Melski, D., and Teitelbaum, T., **WYSINWYX: What You See Is Not What You eXecute**. In *Proc. IFIP Working Conference on Verified Software: Theories, Tools, Experiments (VSTTE)*, Oct. 2005.
- Balakrishnan, G., Reps, T., Kidd, N., Lal, A., Lim, J., Melski, D., Gruian, R., Yong, S., Chen, C.-H., and Teitelbaum, T., **Model checking x86 executables with CodeSurfer/x86 and WPDS++**, (Tool Demonstration Paper). In *Proc. 17th Int. Conf. on Computer Aided Verification (CAV)*, pages 158-163, Jul. 2005.
- Lal, A., Reps, T., and Balakrishnan, G., **Extended Weighted Pushdown Systems**. In *Proc. 17th Int. Conf. on Computer Aided Verification (CAV)*, pages 434-448, Jul. 2005.
- Balakrishnan, G., Gruian, R., Reps, T. and Teitelbaum, T., **CodeSurfer/x86 - A Platform for Analyzing x86 Executables**, (Tool Demonstration Paper). In *Proc. 14th Int. Conf. on Compiler Construction (CC)*, pages 250-254, Apr. 2005.
- Balakrishnan, G. and Reps, T., **Analyzing Memory Accesses in x86 Executables**. In *Proc. 13th Int. Conf. on Compiler Construction (CC)*, pages 5 - 23, Apr. 2004.
(Won the EAPLS best paper award at ETAPS 2004.)

Invited Papers

- Reps, T. and Balakrishnan, G., **Improved Memory-Access Analysis for x86 Executables**, In *Proc. Conf. on Compiler Construction (CC)*, Budapest, Hungary, Mar 29-Apr 6, 2008. **(Paper accompanying a unifying invited talk at ETAPS08.)**
- Balakrishnan, G. and Reps, T., **DIVINE: Discovering Variables IN eXecutables**. In *Proc. Conf. on Verification Model Checking and Abstract Interpretation (VMCAI)*, Nice, France, Jan 14-17, 2007.
- Reps, T., Balakrishnan, G., and Lim, J., **Intermediate-representation recovery from low-level code**. In *Proc. Workshop on Partial Evaluation and Program Manipulation (PEPM)*, Charleston, SC, Jan. 9-10, 2006.

- Reps, T., Balakrishnan, G., Lim, J., and Teitelbaum, T., **A Next-Generation Platform for Analyzing Executables**. In *Proc. 3rd Asian Symposium on Programming Languages and Systems*, Tsukuba, Japan, Nov. 3-5, 2005.

Book Chapters

- **Malware Detection**, volume 27 of *Advances in Information Security*. Springer-Verlag, Oct. 2006. [Editors: M. Christodorescu, S. Jha, D. Maughan, D. Song, and C. Wang]
- **Analysis of COTS for Security Vulnerability Remediation**, G. Balakrishnan, M. Christodorescu, V. Ganapathy, J. T. Giffin, S. Rubin, H. Wang, S. Jha, B. P. Miller, and T. Reps. In *Information Security Research: New Methods for Protecting against Cyber Threats*, C. Wang, S. King, R. Wachter, R. Herklotz, C. Arney, G. Toth, D. Hislop, S. Heise, and T. Combs, editors, Wiley Publishing Inc., July 2007.

Reprinted in Collections

- Reps, T., Balakrishnan, G., Lim, J., and Teitelbaum, T., **A Next-Generation Platform for Analyzing Executables**. In *Proc. of the ARO-DHS Malware Detection Workshop*, (Arlington, VA, Aug 10-11, 2005), *Advances in Information Security* series, Springer-Verlag.

(Reprinted from *Proc. 3rd Asian Symposium on Programming Languages and Systems*, Tsukuba, Japan, Nov. 3-5, 2005.)

Other Publications and Reports

- Balakrishnan, G., Reps, T., Kidd, N., Lal, A., Lim, J., Melski, D., Gruian, R., Yong, S., Chen, C.-H., and Teitelbaum, T., **Model Checking x86 Executables with CodeSurfer/x86 and WPDS++**. In *Proc. Workshop on the Evaluation of Software Defect Detection Tools*, June 2005. [Co-located with PLDI05.]

TECHNICAL PRESENTATIONS

Conference and External Seminar Presentations

- “SLR: Path-Sensitive Analysis Through Infeasible-Path Detection and Syntactic-Language Refinement”, *Static Analysis Symposium (SAS)*, Valencia, Spain, June 2008.
- “Analyzing Stripped Device Driver Executables,” *Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, Budapest, Hungary, March 2008.
- “WYSINWYX: What You See Is Not What You eXecute,”
 - ROSAEC Center, Seoul National University, June 02, 2009.
 - IMDEA, Madrid, Spain, June 2008.
 - North East Verification (NEVER) Seminar, U Penn, Philadelphia, PA, Nov 2007.
 - Ph.D Defense at UW Madison, Aug 2, 2007.
 - IBM Research, Hawthorne, NY, May 2007.

- GrammaTech, Inc., Ithaca, NY, April 2007.
- NEC labs, Princeton, NJ, March 2007.
- Microsoft Research, Bangalore, India, August 2006.
- IBM India Research Lab, New Delhi, India, August 2006.
- “Recency-Abstraction for Heap-Allocated Storage,”
Static Analysis Symposium (SAS), Seoul, South Korea, August 2006.
- “Model Checking x86 Executables with CodeSurfer/x86 and WPDS++,”
Conference on Computer Aided Verification (CAV), Scotland, UK, July 2005.
- “CodeSurfer/x86 - A Platform for Analyzing x86 Executables”
Conference on Compiler Construction (CC), Scotland, UK, April 2005.
- “Analyzing Memory Accesses in x86 Executables,”
 - CSA Dept., Indian Institute of Science (IISc), Bangalore, India, August 2004.
 - CSE Dept., Anna University, Chennai, India, August 2004.
 - CS Dept., Indian Institute of Technology (IIT), Chennai, India, August 2004.
 - Conference on Compiler Construction (CC), Barcelona, Spain, April 2004.
 - IBM Watson Research Center, Hawthorne, NY, USA, December 2003.
 - Dagstuhl Seminar on Language-based Security, Germany, October 2003.

Presentations to Funding Agencies

- “Identifying Variables in x86 Executables,”
ONR MURI Workshop, Arlington, Virginia, February 14, 2005.
- “Analyzing Memory Accesses in x86 Executables,”
 - ONR MURI Workshop, Pittsburgh, Pennsylvania, July 23, 2003.
 - ONR MURI Workshop, Williamsburg, Virginia, January 28, 2003.
 - ONR MURI Workshop, Harpers Ferry, West Virginia, July 12, 2002.
 - ONR MURI Workshop, Washington, DC, January 15, 2002.

PROFESSIONAL ACTIVITIES

- Reviewer (as an external referee) for POPL 10, SAS 09, VMCAI 09, TACAS 09, ATVA 08, Computer Aided Verification (CAV) 2008, Programming Language Design and Implementation (PLDI) 2008, Tools and Algorithms for the Construction and Analysis of Systems (TACAS) 2007, CAV 2006.
- Technology transfer to GrammaTech, Inc., Ithaca, NY, USA. Led the design, implementation, and transfer of the core analysis component of CodeSurfer/x86.

PERSONAL INFORMATION

Visa Status: F1

Country of Citizenship: India

REFERENCES

Available on request.