Jayaram Bobba

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Research Interests

Multi-core architectures, Memory System Design, Novel Hardware/Software Interfaces like Transactional Memory

Education

Doctor of Philosophy, Computer Sciences — Jan 2010 (Expected)
University of Wisconsin–Madison
Thesis: "Hardware Support for Efficient Transactional and Supervised Memory Systems"
Advisor: Dr. Mark D. Hill
Minor: Science and Technology Studies
GPA: 4.0/4.0

Master of Science, Computer Sciences — May 2006
University of Wisconsin–Madison
GPA: 3.94/4.0

Bachelor of Technology, Computer Science — May 2004
IIT Madras, India
GPA: 3.78/4.0

Work Experience

Research Assistant, Multifacet Group — Summer 2005–Present
Department of Computer Sciences
University of Wisconsin–Madison

Research Focus: Transactional Memory (TM)—hardware design and software applications. Architectural support for program supervision

Technical:

- Co-developed an implementation of the LogTM-SE hardware TM system in a full-system hardware simulator
  - Defined high-level simulator architecture
  - Defined and implemented the hardware-software interface for the TM system (e.g., user-level exception handlers, software abort handlers)
  - Developed TM workloads (SPLASH2, BerkeleyDB etc.)
- Developed the TokenTM hardware TM system in a full-system simulator
- Modified an RTL-level implementation of the OpenSPARC memory controller.

Changed ECC codes in order to 'steal' some bits for TM implementations, similar to the S3.mp architecture
- Added store buffer handlers to OpenSPARC hypervisor code
- Developed a framework to run unit tests and patch tests on commercial software using proposed software and hardware TM systems

Service:
- One of a 3 member student-team that open-sourced the LogTM-SE implementation (www.cs.wisc.edu/gems) leading to many non-Wisconsin publications
- Organized architecture seminar series and reading groups (Fall 2008 and Spring2009)
- Reviewed articles for multiple IEEE journals and conferences

Coop Intern — Jan 2007–May 2007
Manager: Pat Conway, Northbridge performance team
Advanced Micro Devices (AMD)

- Developed stochastic processor models for current and future AMD processors
- Developed a python-based scripting framework for end-to-end automation of simulation studies-from specifying configuration to displaying results graphically

Teaching Assistant — Fall 2004, Spring 2005, Spring 2008
Department of Computer Sciences
University of Wisconsin–Madison

Undergraduate: Introduction to Computing; Machine organization and programming
Graduate: Advanced Computer Architecture II

Refereed Publications
(Available at http://pages.cs.wisc.edu/~bobba/publications.htm)

- **Jayaram Bobba**, Mark D. Hill and David A. Wood, "Safe and Efficient Supervised Memory" (***Under Submission***)
- **Jayaram Bobba**, Weiwei Xiong, Luke Yen, Mark D. Hill, and David A. Wood, "StealthTest: Low Overhead Online Software Testing using Transactional Memory," *Proc. of the Conference on Parallel Architectures and Compilation Techniques (PACT)*, Sep 2009
- **Jayaram Bobba**, Neelam Goyal, Mark D. Hill, Michael M. Swift and David A. Wood, "TokenTM: Efficient Execution of Large Transactions with Hardware Transactional Memory," *Proc. of the 35th Annual International Symposium on Computer Architecture (ISCA)*, June 2008
- **Jayaram Bobba**, Kevin E. Moore, Luke Yen, Haris Volos, Mark D. Hill, Michael M. Swift and David A. Wood, "Performance Pathologies in Hardware Transactional Memory," *IEEE Micro Special Issue: Micro's Top Picks from Microarchitecture Conferences*, January-February 2008. (Shorter, award version of ISCA 2007 paper)
- **Jayaram Bobba**, Kevin E. Moore, Luke Yen, Haris Volos, Mark D. Hill, Michael M. Swift and David A. Wood, "Performance Pathologies in Hardware Transactional Memory," *Proc. of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007

- Luke Yen, **Jayaram Bobba,** Michael M. Marty, Kevin E. Moore, Haris Volos, Mark D. Hill, Michael M. Swift and David A. Wood, "LogTM-SE: Decoupling Hardware Transactional Memory from Caches," *Proc. of the 13th International Symposium on High-Performance Computer Architecture (HPCA),* Feb 2007
- Michelle J. Moravan, **Jayaram Bobba**, Kevin E. Moore, Luke Yen, Mark D. Hill, Ben Liblit, Michael M. Swift and David A. Wood, "Supporting Nested Transactional Memory in LogTM," *Prof. of the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Oct 2006
- Kevin E. Moore, **Jayaram Bobba**, Michelle J. Moravan, Mark D. Hill and David A.Wood, "LogTM: Log-Based Transactional Memory," *Twelfth International Symposium on High Performance Computer Architecture (HPCA)*, February 2006
- Manoj Kumar A., **Jayaram Bobba**, Kamakoti V., "MemMap: Technology Mapping Algorithm for Area Reduction in FPGAs with Embedded Memory Arrays using Reconvergence Analysis," *Proc. of Design and Test Automation in Europe (DATE)* 2004
- Manimegalai R., **Jayaram Bobba**, Manoj Kumar A., , Kamakoti V., "SHAPER: Synthesis for Hybrid FPGAs containing PLAs using Reconvergence Analysis, " *International Conference on Field-Programmable Technology (FPT)*, Dec 2004
- Manoj Kumar A., **Jayaram Bobba**, Manimegalai R., Kamakoti V., "MemMap-pd: Performance Driven Technology Mapping Algorithm for FPGAs with Embedded Memory Arrays," *11th Reconfigurable Architectures Workshop (RAW2004)*, Santa Fe, New Mexico
- **Jayaram Bobba**, Manoj Kumar A. and Kamakoti V., "Parallel Partitioning Techniques for Logic Minimization using Redundancy Identification," *International Conference on High Performance Computing (HiPC)*, Dec 2003

Selected Talks and Posters

- StealthTest: Low Overhead Online Software Testing using Transactional Memory, Invited Talk, Microsoft Research India, Oct 2009
- Designing Efficient Safe Supervised Memory Systems, Poster, PACT, Sep 2009
  (Awarded second place in ACM SRC competition)
- LogTM-SE: Log-Based Transactional Memory Signature Edition, Invited Talk, Microsoft Research Silicon Valley, Mar 2007
- LogTM-SE: Log-Based Transactional Memory Signature Edition, Invited Talk, Advanced Micro Devices, Mar 2007
- Virtualizing Log-Based Transactional Memory, Invited Talk, Intel PhD Fellowship Forum, Oct 2006

Technical Skills

- Languages
  Working knowledge of C/C++, Python, Verilog and SPARC assembly.
  Familiar with Java, Perl and x86 assembly
- Tools
  SVN (software versioning), Virtutech Simics (full-system simulation), Synopsys VCS (RTL compilation and simulation), Intel Pin (Dynamic Binary Instrumentation)
- Platforms: Linux, Solaris

Selected Awards

- **2nd place ACM Student Research Competition (SRC)**, PACT 2009
- **Intel Foundation PhD Fellowship** 2006-2007
- **Summer Research Fellowship** 2005 by the Dept. of CS, Univ. of Wisconsin–Madison
- TCS Award for **Best Outgoing Student** by the Dept. of CS, IIT Madras
- **Prathibha Scholarship** by the Govt. of Andhra Pradesh
- **All India Rank 7** in GATE examinations for entrance into graduate studies among premier institutes in India