QUALCOMM AIMS HEXAGON AT FEMTOCELLS

Hexagon DSP, Scorpion CPU Power New FSM Processors

By Linley Gwennap {10/31/11-02}

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Qualcomm is best known for its cell-phone processors, but the company has been producing base-station chipsets for decades. For most of this time, Qualcomm has focused on CDMA base stations, but more recently, it has seized an opportunity to expand into the femtocell market. The company's FSM products support either CDMA or UMTS (also known as WCDMA), the two most common 3G protocols, and target residential and enterprise femtocell systems.

The FSM products use function blocks developed for Qualcomm's cell-phone processors, including its Scorpion CPU, Hexagon DSP, and cellular-protocol hardware accelerators. This leverage, as well as Qualcomm's huge engineering resources, enabled the company to quickly develop these products to target the growing demand for small base stations. Qualcomm joins Freescale, Picochip, Texas Instruments (TI), and several other competitors in this burgeoning market.

Hexagon is a new name for Qualcomm's in-house DSP design. Until recently, Qualcomm wrote all the code for its DSPs, giving customers access only through APIs. Now, however, the company is opening its DSP architecture to outside programmers, expanding their ability to create innovative applications for Qualcomm's processors.

The FSM9832 is Qualcomm's newest femtocell processor. This chip is designed for enterprise femtocells supporting up to 32 users—an upgrade from earlier 8-user chips intended for residential models. The new processor supports CDMA 1x and EV-DO connections at up to 9.8Mbps. It is also available in a 16-user UMTS version that supports HSPA+ at up to 28Mbps in two-antenna (2×2) configurations, as Table 1 shows. None of these processors supports LTE, although the company is developing future products for 4G femtocells.

Hexagon Replaces CPU, DSP

Hexagon, the sixth-generation Qualcomm DSP (QDSP6), is based on work that goes back more than a decade. Earlier QDSP versions used a traditional DSP architecture designed to maximize MAC performance and minimize area. At first, the company used these DSPs only in its cellular-baseband units, where they handled the heavy signal processing that CDMA requires. These baseband units also included an ARM CPU, which was easier to program for the complicated upper levels of the cellular protocol. Qualcomm's Snapdragon smartphone processors include an additional DSP that offloads some multimedia functions from the application CPU.

For Hexagon, the company took a different approach. Although still designed for high performance, this version provides a simpler, more RISC-like programming model. Hexagon has a unified memory space for both instructions and data and includes an MMU for virtual addressing. It uses a single orthogonal register file for all data and a load/store model to simplify arithmetic execution. The instruction set includes a variety of jumps and subroutine

	FSM9216	FSM9816	FSM9832
CPU Speed	1.0GHz	1.0GHz	1.0GHz
DSP Speed	600MHz	600MHz	600MHz
Max Active Users	16 users	16 users	32 users
Cellular Protocols	UMTS	CDMA	CDMA
Max Download	28Mbps	9.8Mbps	9.8Mbps
IC Process	45nm G	45nm G	45nm G
Power (max)	3.5W	3.5W	4W
Production	3Q11	3Q11	4Q11 (est)

Table 1. Qualcomm FSM9xxx product configurations. In addition to these newer products, the company also offers four- and eight-user models that entered production in 1Q11. (Source: Qualcomm)

calls along with traditional DSP zero-overhead looping. Caches, address translation, and pipeline hazards are all handled in hardware, transparent to most software.

This simpler programming model enables Hexagon to support a standard CPU software-development tool chain (GCC). With its MMU, it can support real-time operating systems and even Linux. These capabilities allowed Qualcomm to open the architecture to third-party software development, expanding the capabilities of its processors. In some of its new baseband units, the Hexagon DSP even runs the cellular protocol stack.

A Four-Slot VLIW DSP

Hexagon is a 32-bit fixed-point DSP. It includes a 32-entry general-register file; each register contains 32 bits, but they can be addressed in pairs to enable 64-bit operations. The architecture defines additional special registers: for example, four special predicate registers that hold 8 bits each, enabling vector compare operations. Conditional branch instructions use the values of these predicate registers to determine whether to branch. Some math and load/store instructions can also be predicated, enabling them to execute conditionally on the basis of a predicate value. Predicated execution eliminates branches in some short code sequences.

Like TI's C64x and other modern DSP architectures, Hexagon uses a VLIW model for parallel instruction execution. This method reduces the hardware complexity associated with superscalar issue while putting the burden on the compiler and the programmer to build parallel-instruction groups. Hexagon supports groups of up to four instructions, corresponding to the four function units in the DSP itself, shown in Figure 1. No instruction group can include two instructions for the same function unit, and the instructions in a group cannot write to the same register or read the results of another instruction in the same group. One exception is that predicates can be written and read in the same group, enabling a compare and branch in the same cycle.
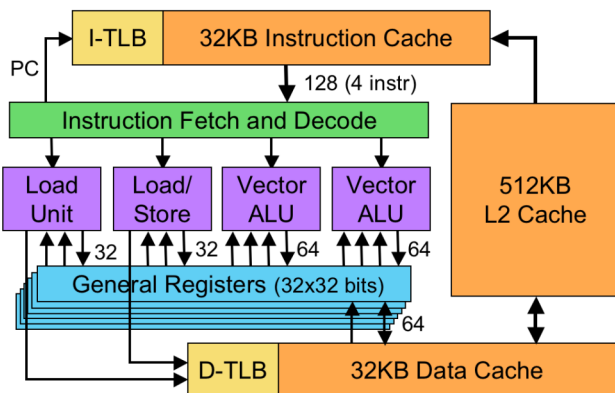
Figure 1. Hexagon DSP block diagram. The VLIW-style design can issue four instructions per cycle. It supports multithreading using six copies of the register file.

The architecture contains two memory units and two vector units. The vector units perform SIMD operations on byte, half-word, and word data stored in pairs of 32-bit registers. They also handle standard 32-bit math as well as branch instructions. Floating-point operations are not supported. Each memory unit can load data; one can also store data. When not performing memory operations, both memory units can instead execute 32-bit ALU operations, increasing the flexibility of instruction grouping.

The architecture defines both scalar and vector instructions. Typical math operations include add, compare, average, multiply, multiply-accumulate with optional scaling, rounding, and saturation. The architecture also supports complex ($a+bi$) operations. Other data manipulations include sum of absolute differences (SAD), logical operations, shifts, permutations, and format conversions. SAD is useful in video compression and other signal-processing algorithms.

Load and store instructions can access from 8 to 64 bits each. The architecture supports a variety of memory-addressing modes, such as relative, indirect, circular, and bit-reversed. The latter two modes are common in DSP algorithms. Loads and stores can specify auto-increment, eliminating the need for a separate instruction to increment the address pointer. Atomic load/stores support semaphores and mutexes.

Two special loop registers support zero-overhead looping with one level of nesting. Using this approach, the operations of decrementing and testing the loop count do not consume any instruction slots or execution cycles.

Hardware Multithreading Adds Efficiency

The DSP in the FSM processor is known internally as QDSP6v3, a third-generation design developed mainly in Austin, Texas. This implementation of the Hexagon architecture operates at up to 600MHz in 45nm. It includes a 32KB instruction cache and a 32KB data cache as well as a 512KB level-two (L2) cache.

The DSP fetches 128 bits (four instructions) per cycle from the instruction cache and examines the grouping bits to determine if it can issue all four instructions in a single cycle or if it requires multiple cycles. Because the compiler/assembler adds the grouping bits and also orders the instructions according to which function unit should execute it, the instruction-issue hardware is relatively simple.

The QDSP6v3 implements hardware multithreading for up to six threads. The design uses a round-robin approach to multithreading, switching from one thread to the next on every cycle. This approach hides many delays caused by data dependencies, L1 cache misses, and pipeline stalls; if all threads are active, any pipeline stall has six cycles to resolve before the next instruction group in that thread is executed. If the stall takes more cycles to resolve, that thread does nothing on its next execution cycle, and then the DSP continues cycling through the other threads.

This multithreading approach reduces the number of unused pipeline cycles. Since the thread-switching logic is so simple, the only significant die-area penalty is the six complete register files, one for each thread. The downside is that programs must have at least six active threads to take full advantage of the Hexagon DSP; a single thread operates at just 100MHz, effectively. In addition, the caches must be shared among the active threads, which can reduce the cache-hit rate compared with running a single thread only.

Multithreaded Benchmarking Is Tricky

Using both vector units and the multiply-accumulate instructions, a Hexagon DSP can perform eight 16-bit integer MACs per cycle or four 32-bit MACs. While performing these operations, the processor can use the two memory units to load a total of 128 bits per cycle—enough to feed one new operand into the vector units. Using zero-overhead looping and auto-increment addressing, all of these operations can execute at their peak rate without any overhead for updating address registers and loop counters. Thus, the processor should be able to sustain its peak MAC performance on most common algorithms.

Hexagon is similar to TI's C64x+ DSP, an integer-only design that can also execute eight 16-bit MACs per cycle using a pair of 64-bit-wide MAC units. It has four other function units that can perform additional computations, and the VLIW design can issue up to eight instructions per cycle. But it has less load bandwidth (64 bits per cycle) than the Hexagon design. Thus, the TI design will excel on algorithms that perform multiple computations on each operand, but Hexagon will be more efficient on algorithms that are memory bound, such as simple dot products.

For its newer processors, TI is shifting to the C66x, which doubles the per-cycle performance of the C64x+ and combines both fixed- and floating-point support in a single design (see *MPR 6/27/11,* "TI Tackles Small Base Stations"). Originally intended for mobile processors, Hexagon targets low cost and low power. Qualcomm is developing more-powerful DSP designs for future processors.

We prefer to compare DSP performance using the BDTImark2000, which provides a summary measure of signal-processing speed using 16-bit data. BDTI has measured the QDSPv2 but not the QDSPv3, although the differences between these two versions are minor. On BDTImark2000, the 600MHz QDSPv2 achieves a score of just 1,550. By comparison, the C64x+ scores 6,585 at the same clock speed.

The BDTImark2000, however, is based on a set of single-threaded DSP kernels that do not exploit Hexagon's multithreading. We believe the design would achieve near-linear scaling when running six copies of BDTImark2000, since these small kernels would not overflow the caches. If so, Hexagon would outperform the C64x+ by about 40%

on a clock-for-clock basis and would even outperform the C66x by a small margin. The TI DSPs, however, are capable of operating at up to twice the clock speed of the current Hexagon DSP, giving TI an overall performance advantage.

Furthermore, real signal-processing applications are unlikely to achieve perfect scaling on the Hexagon design. Because of its round-robin scheduling, if the performance of the threads is not precisely balanced, some threads will waste cycles waiting for the others to complete. In addition, the L1 caches can quickly fill when six threads are running, wasting cycles while the DSP fetches instructions and data from the L2 cache. To better characterize these effects, additional benchmarking of the Hexagon design is needed.

Qualcomm Delivers Complete Chipset

The FSM9832 includes a single Scorpion CPU running at 1.0GHz. Scorpion is the company's in-house microarchitecture and is ARMv7 compatible (see *MPR 7/19/10,* "Two-Headed Snapdragon Takes Flight"). This CPU handles Layers 2 and 3 of the cellular protocol as well as OEM-specific code and applications, while the Hexagon DSP handles Layer 1. The DSP is assisted by a hard-wired modem engine similar to the one Qualcomm uses in its handset chips. This modem supports two-antenna techniques, such as 2×2 MIMO and T/R (transmit/receive) diversity, that improve throughput and reduce interference.

The processor includes a separate "network listen" (NL) subsystem with an ARM11 CPU and its own cellular modem. This subsystem continually monitors the RF environment; if it detects RF interference, it notifies the main CPU, which can adjust the power or frequency of the cellular transmission to overcome or avoid the interference. Most competing processors have a single cellular sub-
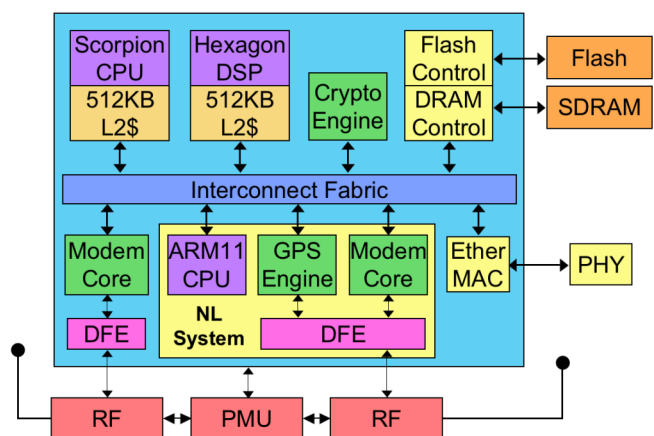
Figure 2. FSM9832 block diagram. Qualcomm's femtocell processor combines an ARM-compatible Scorpion CPU, a Hexagon DSP, hardware accelerators, and other system components. The company provides power-management (PMU) and RF chips to complete the design.

system and can check for interference only when they are not sending or receiving data. The dedicated NL subsystem makes Qualcomm's design more robust and less likely to drop calls.

Taking advantage of this capability, Qualcomm has developed software called UltraSON that helps coordinate multiple femtocells operating in the same area, such as a single building. This software supports handoffs between cells and uses the NL input to minimize interference between nearby femtocells. UltraSON should be particularly useful in enterprise deployments.

The NL subsystem also includes a GPS engine. GPS provides not only precise location but precise time, which is required to support synchronous cellular networks such as CDMA and LTE.

The FSM9832 is a complete system-on-a-chip design with a memory controller and a Gigabit Ethernet controller. The system can use Ethernet for the uplink, or this port can connect to an external DSL or cable-modem chip for broadband access. As Figure 2 shows, the chip also integrates the digital front end (DFE), providing a glueless interface to the external radio chips.

The FSM9xxx requires two external cellular RF chips: one for the main modem (FTR8700) and a second for the NL modem (RTR8605). The RTR chip also includes the RF circuitry for the GPS controller. A single FTR chip implements two receive chains for MIMO and T/R diversity, but systems that support multiple bands require a second FTR8700 chip. Qualcomm provides a complete chipset including the processor, RF chips, and a power-management chip (PM8058).

The company also supplies a complete Layer 1 software stack that has passed IOT in the lab. OEMs can develop their own software for Layer 2 and above. Qualcomm also supports third-party software stacks, including one from Radisys (which acquired Continuous Computing earlier this year).

	Qualcomm FSM9216	Freescale PSC9131
CPU Type	1.0GHz Scorpion	1.0GHz PPC e500
DSP Type	600MHz Hexagon	1.0GHz SC3850
Peak DSP MACs*	4.8GMAC/s	8.0GMAC/s
BDTImark2000	1,550×6†	15,420
Max UMTS Rate	28Mbps	42Mbps
Max LTE Rate	Not supported	100Mbps
System I/O	1×GbE	2×GbE, USB
# of Active Users	16 users	16 users
Power (max)	3.5W	3W
IC Process	45nm G	45nm SOI
Availability	Production 3Q11	Production 2Q12‡

Table 2. Qualcomm FSM versus Freescale Qonverge. Both products target 16-user femtocells. The PSC9131 offers faster downloads, LTE support, and lower power, but it is a year later than the FSM9216. *Real fixed-point 16-bit MACs; †1,550 per thread, six threads. (Source: vendors, except ‡The Linley Group estimate)

Competitors Lead With LTE

By extending its product line to support 16 and 32 users, Qualcomm has exceeded the performance of residential femtocells, but it cannot match vendors such as Cavium and TI that are aiming at pico and metro base stations with 64 to 128 or more users. The closest competitor to the new FSM processor is Freescale's Qonverge, which currently supports 8 to 64 users (see *MPR 2/21/11,* "Freescale Cues CPU/DSP Hybrid"). Table 2 compares the FSM9216 with Freescale's PSC9131, which is also rated for 16 users.

Both products include a 1.0GHz dual-issue CPU, but Freescale's Power e500 core should deliver slightly better application performance because of its instruction reordering. Both DSPs can execute eight real fixed-point 16-bit MACs per cycle, but Freescale's StarCore DSP operates at 1.0GHz, 67% faster than the Hexagon DSP. On BDTI-mark2000, the Freescale design has a similar 66% advantage, even assuming perfect scaling from Hexagon's six threads. This greater DSP performance helps the PSC9131 reach a maximum downlink speed of 42Mbps for HSPA, whereas the FSM9216 tops out at 28Mbps.

Both companies provide production-ready Layer 1 code while relying on OEMs to develop their own code for higher layers. Freescale relies on third-party components for the radio and power management, but Qualcomm supplies a complete chipset, simplifying system design. Both companies also offer CDMA versions of their processors. The FSM9216 integrates GPS, whereas the PSC9131 requires an external GPS chip (although not in UMTS-only designs).

The biggest difference between the two is that Freescale supports LTE, whereas Qualcomm does not. On the other hand, the FSM9216 is already in production; the Qonverge products only recently sampled. Qualcomm plans to have an LTE femtocell processor in production in 2012, possibly around the same time or only slightly behind Freescale's LTE product. Another difference is that Qonverge scales to 64 users, but Qualcomm supports only 4 to 16 users (or 32 users for CDMA).

Qualcomm Targets Enterprise

Most carriers have acknowledged the need for smaller base stations, but they disagree on whether these systems will be residential femtocells, enterprise femtocells, or larger pico and metro cells. As a result, different processor vendors are targeting different portions of this spectrum, with no agreement on a standard set of features.

Qualcomm has chosen to start at the low end of the market, the better to make use of its handset-processor technology. So far, carriers have deployed a few million residential femtocells, mainly to retain customers with poor voice coverage at home. Most consumers use Wi-Fi at home for data traffic, limiting the number of residential femtos needed. Thus, we see this market having modest but steady volume.

The enterprise is the new femto battleground. Designed for areas with poor macro coverage, most residential femtocells do not work in an enterprise with multiple base stations, nor do they support the higher numbers of users that an enterprise requires. Qualcomm believes it has solved the former problem with its UltraSON technology, and it has beefed up its DSP performance to address the latter problem. Although business employees also use Wi-Fi for data, the limited frequencies of an enterprise Wi-Fi network can become overwhelmed at times; cellular provides a useful alternative in these situations. With its recent acquisition of Atheros, Qualcomm offers complete chipsets for combined 3G/Wi-Fi access points.

In the longer term, we foresee sizable demand for small cells to fill out carrier's LTE networks. Qualcomm's lack of LTE support is surprising, given that the company is a leader in delivering LTE handset processors. The company's roadmap includes LTE femtocell chips, but Cavium, Freescale, and TI have already rolled out their LTE offerings, putting Qualcomm behind in this race. Those three competitors are also rolling out processors that target pico and metro base stations with higher user requirements.

Price and Availability

Qualcomm's FSM9216 (UMTS) and FSM9816 (CDMA) processors are in production; the FSM9832 (CDMA) processor is sampling and expected to enter production by the end of this year. The company has not disclosed pricing. For more information on these products, access *www.qualcomm.com/femtocell.* For more information on BDTImark2000, access *www.bdti.com/ Resources/BenchmarkResults/BDTImark2000.*

In the meantime, the new FSM9xxx products are a good solution for residential and enterprise femtocells, offering a range of price points and supporting both UMTS and CDMA networks. Qualcomm offers a complete chipset, simplifying system design, and is working with third parties to provide a complete software stack. Thus, its solution is well suited to new entrants to the base-station market that are focusing on femtocells. Qualcomm's FSM processors are already in production, and the company is working on higher-end products for next-generation base stations. ♦