

## Dana M. Vantrease

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danav@cs.wisc.edu  
<http://www.cs.wisc.edu/~danav/>

### Education

Ph.D., Computer Sciences August, 2010  
Advisor: Mikko Lipasti University of Wisconsin - Madison  
Dissertation Title: "Optical Tokens in Many-Core Processors."

M.S., Computer Sciences May, 2004  
Advisor: Mikko Lipasti University of Wisconsin - Madison

B.S.E, Computer Science Engineering June, 2002  
Magna Cum Laude Ohio State University

### Publications

"Atomic Coherence: Leveraging Nanophotonics to Build Race-Free Cache Coherence Protocols," Dana Vantrease, Mikko H. Lipasti, Nathan Binkert. In Proceedings of the 17th Annual IEEE International Symposium on High Performance Computer Architecture (HPCA-17), San Antonio, February 2011.

"Light Speed Arbitration and Flow Control for Nanophotonic Interconnects," Dana Vantrease, Nathan Binkert, Robert Schreiber, Mikko H. Lipasti. In Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-42), New York City, December 2009.

"Nanophotonic Barriers," Nathan Binkert, Al Davis, Mikko H. Lipasti, Robert Schreiber, Dana Vantrease. Workshop on Photonic Interconnects And Computer Architecture. Held in Conjunction with 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-42), New York City, December 2009.

"Corona: System Implications of Emerging Nanophotonic Technology," Dana Vantrease, Robert Schreiber, Matteo Monchiero, Moray McLaren, Norman P. Jouppi, Marco Fiorentino, Al Davis, Nathan Binkert, Raymond G. Beausoleil, and Jung Ho Ahn. In Proceedings of the 35th International Symposium on Computer Architecture (ISCA-35), Beijing, China, June 2008.

"An Evaluation of Server Consolidation Workloads for Multi-core Designs," Natalie Enright Jerger, Dana Vantrease, and Mikko H. Lipasti. In Proceedings of the IEEE International Symposium on Workload Characterization (IISWC), Boston, MA, September 2007.

"Commods on the Rez: The Impact of US Government Supplied Foodstuffs on the Identity of American Indians," Dana Vantrease. In American Folklore Society's Annual Meeting, Milwaukee, WI, October 2007.

### Talks

"Light Speed Arbitration and Flow Control for Nanophotonic Interconnects"  
*IEEE/ACM International Symposium on Microarchitecture (MICRO-42)*  
December 2009

"Atomic Coherence: Leveraging Nanophotonics to Build Race-Free Cache Coherence Protocols"  
*IEEE International Symposium on High Performance Computer Architecture (HPCA-17)*  
February 2011

## Invited Talks

“From Rosie The Riveter to Rosie The Researcher”

*University of Wisconsin - Madison's Women in Science and Engineering Seminar*

October 2009

“Under Pressure: Register Files in Multithreaded Processors.”

*Ohio State University's BACK Colloquium*

April 2005

## Experience

Mikko H. Lipasti  
Research Assistant

University of Wisconsin - Madison  
June 2003 – 2010

Researched several aspects of high performance architectures including photonic arbitration, photonic cache coherence techniques, lock arbitration, variations of runahead execution, simultaneous multithreading scheduling policies, soft-error vulnerability in DRAM, and effects of misguided prefetching.

Nathan Binkert and Norm Jouppi  
Intern

Hewlett-Packard Laboratories, Palo Alto, CA  
Summer 2007 and Summer 2008

Investigated exploiting the novel properties of photonic interconnects for data communication and interconnect control in many-core processors.

Developed detailed timing simulator for modeling photonic switches, as well as a PIN-based system-level simulator.

Chris Francois and Jim Effle  
Intern

IBM, Rochester, MN  
Summer 2004

Redesigned tasking, scheduling, and queuing techniques for next generation hardware in iSeries System Licensed Internal Code (SLIC). Also, contributed to compiler debugging efforts of the Blue-Gene/L supercomputer project prior to its deployment.

Jason Reasor and Donald Mullins  
Co-op

Hewlett-Packard, Richardson, TX  
Spring, Summer 2001

Contributing member of the firmware design team for a new generation of high-end Itanium servers. Responsibilities included implementing formal specifications in IA-64 assembly, debugging system bring-up, and designing a nightly regression tester.

## Teaching Experience

Mathematics Volunteer Tutor, Madison Public Schools, 2004–2009

Teaching Assistant, Advanced Computer Architecture I, University of Wisconsin - Madison, 2003

Teaching Assistant, Computer Vision, University of Wisconsin - Madison, Fall 2002

Teaching Assistant, Freshman Engineering Honors Program, Ohio State University, 2000 – 2001

Teaching Assistant, Engineering Honors Summer Institute, Ohio State University, 1999, 2002

## Patents

Two patent applications pending (Qualcomm).

Three photonic patent applications pending (HP Labs).

## University Service

Organizer of Computer Architecture Reading Group, 2009.

Founder of the UW-CS Graduates Anonymous group, a graduate student mentoring group, Fall 2006–2009.

Presenter and organizer of “What’s Hot in CS” luncheon, 2009.

Co-organizer of UW-CS panels on “How to (Successfully) Interview for Academic and Research Lab Positions” and “Preparing for The Preliminary Examination,” 2008.

Co-coordinator of Wisconsin Indigenous Graduate Women And Men (WIGWAM), 2008–2009.

Coordinator of The American Indian High School Retreat Weekend for the UW-Madison AISES chapter, 2005.

New Graduate Student Orientation Chair for the Computer Sciences department of UW-Madison 2003.

### **Professional Service**

External Reviewer for IEEE Computer Architecture Letters, HPCA-15, MICRO-40, MICRO-41, ISCA-35, and ISCA-36.

### **Honors and Awards**

Best Student Presentation, IEEE MICRO-42, 2009

Wisconsin Entrepreneurial Bootcamp Participant, 2009

National Summer Institute Fellow, University of Denver, 2009

National Science Foundation Graduate Research Fellowship, 2004

Wisconsin Capital Times “Volunteers Get Recognition,” 2003

Advanced Opportunity Fellowship, 2002

Undergraduate University Research Grant, 2001