Dana Vantrease

Contact Information

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Summary

PhD with 11 years of industry experience in computer architecture modeling and performance.

Strong in solving hard technical problems in new problem spaces, communicating across disciplines, and critical analysis.

Specialities

machine learning, computer architecture, code-optimization, workload analysis, cache coherence, memory consistency, interconnects, silicon photonics, hw/sw codesign, debug, performance, modeling, low level sw, compilers, synchronization, dma, accelerators.

Education

University of Wisconsin, Madison, WI
Ph.D., Computer Sciences (Computer Architecture), August 2010

Ohio State University, Columbus, OH
B.S. Magna Cum Laude, Computer Science Engineering, May 2002

Experience

Amazon Web Services, Austin, TX

Senior Hardware Engineer **2016-present**

Tech Lead for AWS' ML-Inference chip modeling team. Responsible for design and development of the cycle-approximate bit-accurate model that is used for SW development, HW verification/validation, and performance/power prediction.

Research & Development Experience:

- Created the instruction set and micro-architecture for an ML accelerator engine.
- Invented a testing methodology that generated random race-free multi-threaded programs, unveiling critical RTL bugs.
- Wrote an analytic tool, based in genetic algorithms, that guided network topology decisions.
- 19th top patent-filter in Amazon for 2018.

Leadership Experience:

- Delivered ML education talks that have been recorded as a part of new-hire training.
- Led the technical evaluation of an IP purchase.
- Performed duties as people manager, project manager, and AWS mentor.

Qualcomm, Austin, TX

Staff Engineer **2010-2016**

- Responsible for DSP performance modeling/correlation of: fetch unit, I/D/L2 caches, and memory buses.
- ImpaQt innovation competition finalist, studying database performance/power tradeoffs of Arm vs DSP cores.

University of Wisconsin - Madison, Madison, WI

Graduate Student (advisor Mikko Lipasti) **2002-2010**

- Studied applications of silicon photonics to on-chip interconnect arbitration and cache coherency.
- Publications cited 1300+ times, 5 patents
- Repeat intern at HP Labs' ExaScale group, led by Norm Jouppi.
- Teaching Assisant for graduate level computer architecture and computer vision courses.
- National Science Foundation Graduate Research Fellowship recipient.

Service

Ohio State CSE Industrial Advisory Board Member, 2016-present
MICRO Best Paper Committee, 2020
ISCA External Review Committee, 2019
HPCA Program Committee - Industry Session, 2018
Conducted LED wearable workshops for GirlStart, 2015

Selected Publications

- Dana Vantrease, Mikko Lipasti, and Nathan Binkert. Atomic Coherence: Leveraging Nanophotonics to Build Race-Free Cache Coherence Protocols *HPCA-17*. Feb 2011.
- Dana Vantrease, Nathan Binkert, Robert Schreiber, and Mikko Lipasti. Light Speed Arbitration and Flow Control for Nanophotonic Interconnects. *MICRO-42*. Dec 2009.
- Dana Vantrease, Robert Schreiber, Matteo Monchiero, Moray McLaren, Norman P. Jouppi, Marco Fiorentino, Al Davis, Nathan Binkert, Raymond G. Beausoleil, and Jung Ho Ahn. Corona: System Implications of Emerging Nanophotonic Technology. *ISCA-35*. June 2008.