

Dana M. Vantrease

CONTACT INFORMATION	4613 Ramsey Ave Austin, TX 78756 USA	Voice: (608) 320-1413 E-mail: dana.vantrease@gmail.com Website: http://www.cs.wisc.edu/~danav/
RESEARCH INTERESTS	Computer architecture, memory systems, many-core interconnects, hardware/software interaction, and synchronization.	
EDUCATION	University of Wisconsin , Madison, Wisconsin USA Ph.D., Computer Sciences w/ Folklore Minor, August 2010 M.S., Computer Sciences, May 2004 Advisor Mikko Lipasti Ohio State University , Columbus, Ohio USA B.S. Magna Cum Laude, Computer Science Engineering, May 2002	
HONORS AND AWARDS	Best Student Presentation, MICRO-42, 2009 National Science Foundation Graduate Research Fellowship, 2004 Advanced Opportunity Fellowship, University of Wisconsin, 2002	
SELECTED PUBLICATIONS	<ul style="list-style-type: none">• Dana Vantrease, Mikko Lipasti, and Nathan Binkert. Atomic Coherence: Leveraging Nanophotonics to Build Race-Free Cache Coherence Protocols <i>HPCA-17</i>. Feb 2011.• Dana Vantrease, Nathan Binkert, Robert Schreiber, and Mikko Lipasti. Light Speed Arbitration and Flow Control for Nanophotonic Interconnects. <i>MICRO-42</i>. Dec 2009.• Dana Vantrease, Robert Schreiber, Matteo Monchiero, Moray McLaren, Norman P. Jouppi, Marco Fiorentino, Al Davis, Nathan Binkert, Raymond G. Beausoleil, and Jung Ho Ahn. Corona: System Implications of Emerging Nanophotonic Technology. <i>ISCA-35</i>. June 2008.• Dana Vantrease. Commods on the Rez: The Impact of US Government Supplied Foodstuffs on the Identity of American Indians. <i>The American Folklore Society 2006 Annual Meeting</i>. Sept 2006.	
SKILLS	<ul style="list-style-type: none">• Familiar with a large array of uni- and multi- processor architectures.• Architectural simulator experience includes PharmSim, M5, Pin, SimpleScalar.• Familiar with programming in a Unix environment with C, C++, Python, and assembly.	
PROFESSIONAL EXPERIENCE	Qualcomm , Austin, Texas USA <i>Senior Engineer</i> September 2010-Present <ul style="list-style-type: none">• Member of Qualcomm's DSP architecture team; designing next-generation processors with higher performance, lower power, and new functionality (like augmented reality and gesture-based interactions). Hewlett Packard Labs , Palo Alto, California USA <i>Intern (mentor Nathan Binkert)</i> Summer 2007, 2008 <ul style="list-style-type: none">• Investigated the opportunities nanophotonics has to offer to on-chip interconnect arbitration, cache coherency, and memory consistency. Three patents pending. IBM , Rochester, Minnesota USA <i>Intern (mentor Chris Francois)</i> Summer 2004 <ul style="list-style-type: none">• Designed tasking, scheduling, and queuing policies in the iSeries System Licensed Internal Code.	
VOLUNTEER WORK	<ul style="list-style-type: none">• Organizer of UW CS Architecture Reading Group. Fall 2009.• Founder of UW CS Graduates Anonymous, a graduate mentoring group. Fall 2006 - 2010.• Volunteer tutor for Minority Youth Career Awareness Program. Weekly 2007 - 2009.	