

**CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING
COMPUTER SCIENCES DEPARTMENT
UNIVERSITY OF WISCONSIN-MADISON**

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Midterm Examination 2
In Class (50 minutes)
Friday, October 26, 2007
Weight: 15%

CLOSED BOOK, NOTE, CALCULATOR, PHONE, & COMPUTER.

The exam is two-sided and has 11 pages, including two blank pages at the end.

Plan your time carefully, since some problems are longer than others.

NAME: _____

SECTION: _____

ID# _____

Problem Number	Maximum Points	Graded by
1	3	SR
2	4	SR
3	3	SJ
4	2	SJ
5	3	GJ
6	4	EH
7	3	EH
8	4	NEJ
9	4	GJ
Total	30	

Problem 1 (3 points)

Write the Boolean expression corresponding to the following truth table. You need not simplify the expression.

Inputs			Output
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$$Z = ((\text{NOT}(A)) \text{ AND } (\text{NOT}(B)) \text{ AND } C) \text{ OR } ((\text{NOT}(A)) \text{ AND } B \text{ AND } (\text{NOT}(C))) \text{ OR } (A \text{ AND } B \text{ AND } C)$$

Problem 2 (4 points)

Suppose a 32-bit instruction takes the following format:

OPCODE	DR	SR1	SR2	UNUSED
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If there are 500 opcodes and 60 registers:

- a) What is the minimum number of bits required to represent the OPCODE?

9 bits

- b) What is the minimum number of bits required to represent the destination register DR, and source registers SR1 and SR2? (Give the total number of bits.)

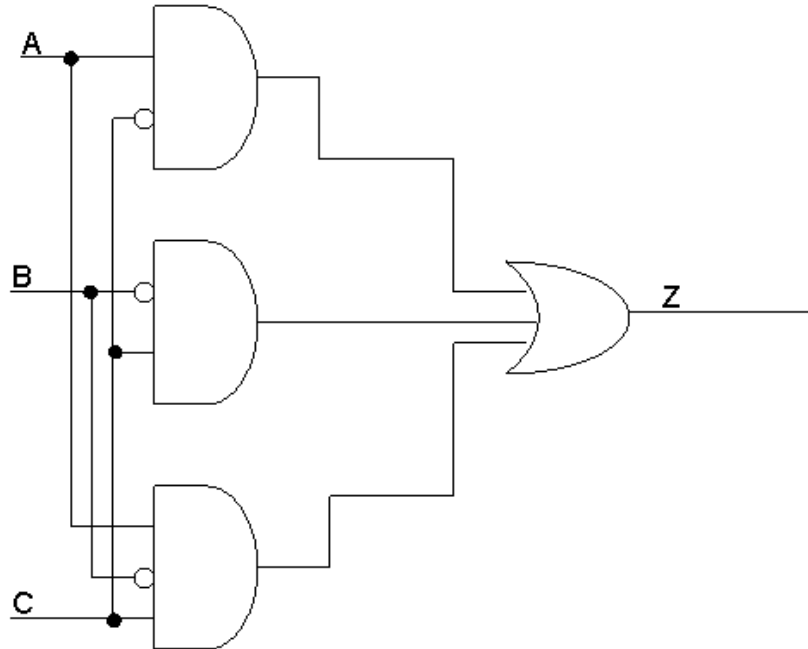
3 * 6 = 18 bits

- c) What is the maximum number of UNUSED bits in the instruction encoding?

32 - 9 - 18 = 5 bits

Problem 3 (3 points)

The figure below shows a combinational logic circuit. Complete the truth table corresponding to this circuit.



Inputs			Output
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

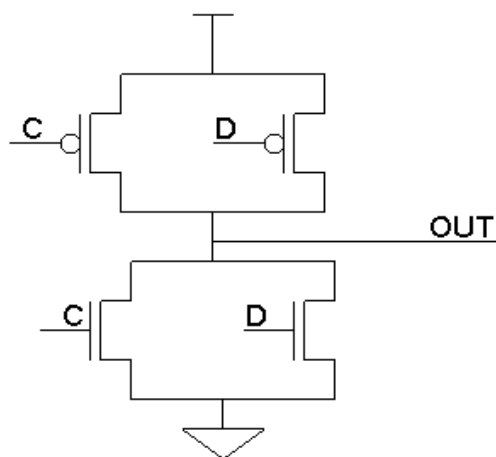
Problem 4 (2 points)

You know a byte is 8 bits. A 4-bit quantity is called a *nibble*. If a byte-addressable memory has a 64-bit address, how many nibbles of storage are in this memory?

$$2^{64} * 8/4 = 2^{65} \text{ nibbles}$$

Problem 5 (3 points)

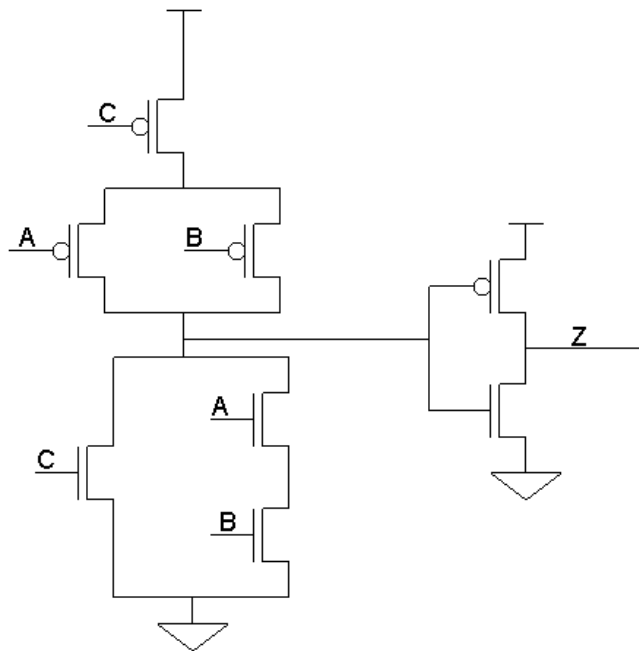
The circuit below has a major flaw. Can you identify it? *Hint*: Evaluate the circuit for all sets of inputs.



There is short circuit (path from Power to Ground) when either C = 1 and D = 0 or C = 0 and D = 1.

Problem 6 (4 points)

Fill in the truth table for the following transistor level circuit. Note that two wires with the same name are assumed to be connected to each other.

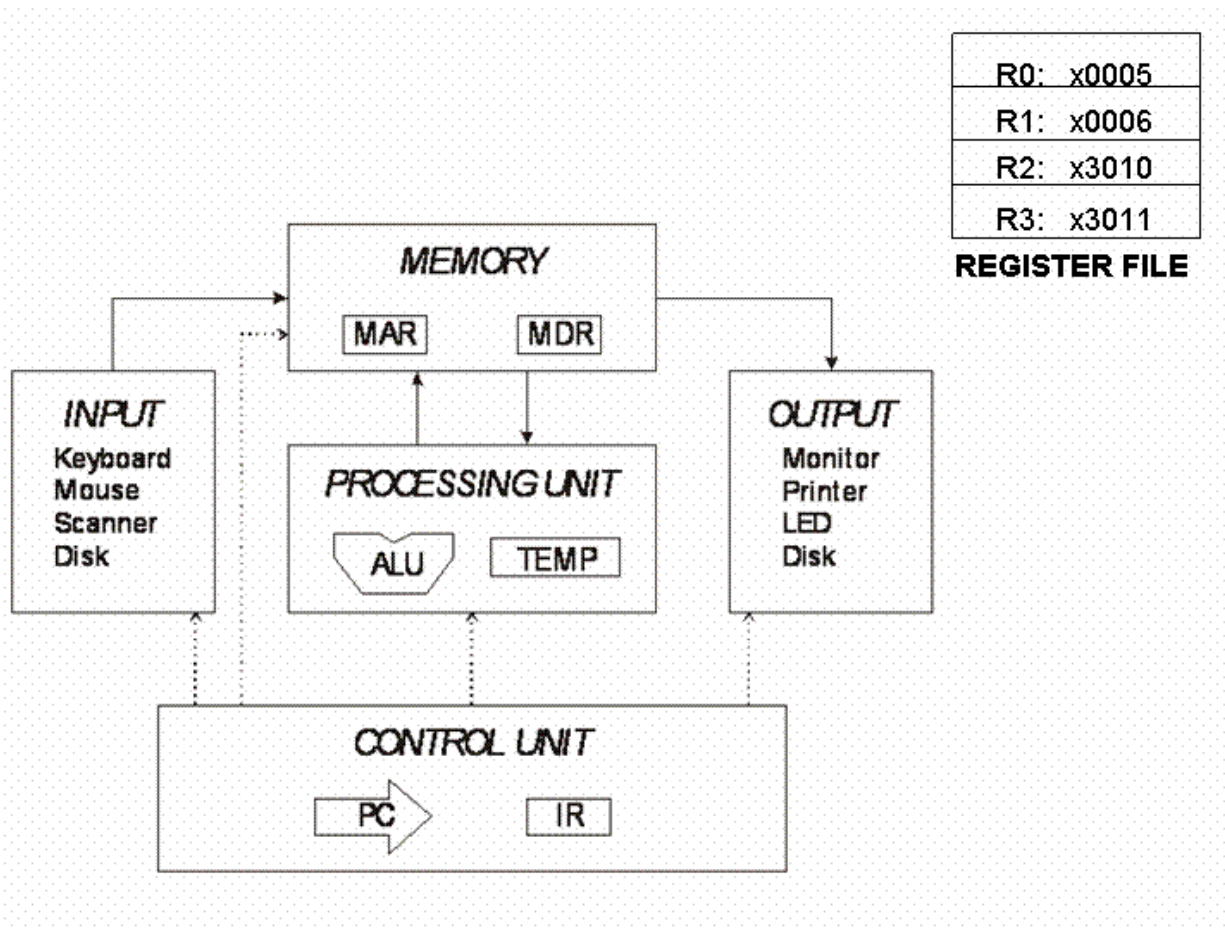


Inputs			Output
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1

1	1	1	1
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Problem 7 (3 points)

The figure below shows a block diagram of the Von Neumann model.



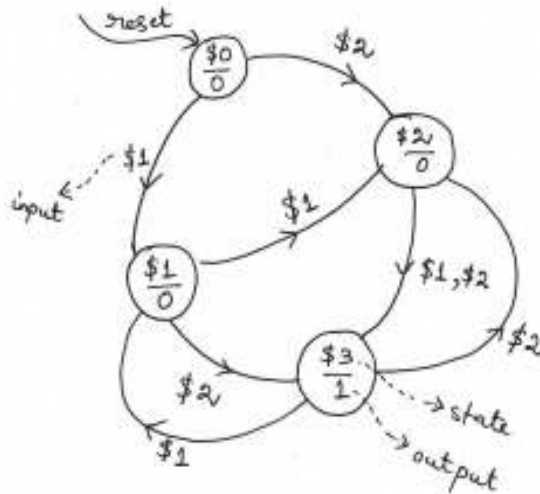
List the steps in writing a value x0005 to a location x3011 in the memory. Your steps should mention the MAR and MDR where applicable.

- 1) Write the data x0005 to MDR
- 2) Write the address x3011 into the MAR
- 3) Send a "write" signal to the memory

Problem 8 (4 points)

A Vending machine delivers a package of gum after 3 dollars are deposited. It has a single bill slot which accepts only \$1 or \$2 bills. (No other types of bills/coins are accepted). The vending machine does not return back changes.

- I. Draw the finite state machine diagram for the vending machine. The machine takes one input every clock cycle which can be \$1, \$2 or reset. The machine outputs a 1 when it opens to deliver a gum package, otherwise it outputs a 0.



- II. How many flip-flops (storage elements) will be needed to implement this finite state machine designed in your answer to part I?

2 flip-flops

Problem 9 (4 points)

Circle the correct answer for the following questions:

- I. Circuit A is a 1-bit adder calculating the sum only and no carry; circuit B is a 1 bit multiplier. Both the circuits are implemented using AND, OR and NOT gates only.
- a. Circuit A has the same number of gates as circuit B
 - b. **Circuit A has more gates than circuit B**
 - c. Circuit B has more gates than circuit A

(Hint: Construct the truth table for the adder and the multiplier)

- II. If the number of address bits in a memory is reduced by 2 and the addressability is doubled, the size of the memory (i.e., the number of bits stored in the memory)
- a. Doubles
 - b. Increases by $2^{(\text{address bits})/\text{addressability}}$
 - c. Remains unchanged
 - d. **Halves**
- III. The minimum number of transistors required to implement a CMOS 3 input OR gate is
- a. **8**
 - b. 6
 - c. 4
 - d. 10
- IV. The Decode phase of the Instruction Cycle always examines which part of the instruction?
- a. Immediate (literal) value
 - b. Register
 - c. **Opcode**
 - d. Offset