CS552 Final Project

Team Name
Team Members

Overview

Less than a page describing overall what the project is about and what you did. Discuss each of the pipeline stages and cache design.

Design and Optimizations

Design overview which should include your high-level processor schematics. Your design hierarchy must be clear. One high-level schematic that shows only the high-level pipeline is too little detail. Showing schematics for every MUX is too much. Use your discretion.

Discussion of optimizations implemented. (Maximum 1 page)

For partial credit if there are failures: A discussion of what does not work and why. Also include what you would have liked to implement given more time. For each part of the implementation that does not work, turn in an annotated output in the form of a trace or script run that clearly shows the error. Give your thoughts as to why the error occurs and what could be done to fix it. (without counting traces this section should not exceed half a page)

Design Analysis

A table describing the performance of the "552marks". Include CPI, cycles, and total execution time for each benchmark. Be sure to include your processor's cycle time, and the final 552mark score.

A table listing the possible hazards that arise in your pipelined design and the number of stall cycles that each hazard incurs. (Maximum half a page)

A brief discussion of your cache design that explains the number of cycles for a cache-hit, cache-hiss (with eviction of a line), cache-miss (without any eviction). (Maximum half a page)

A state diagram for any state machine controllers in your design. All other controllers should include a high-level textual description. (This also can be short, maximum 4 pages)

Conclusions and Final Thoughts

A conclusion outlining what you learned by doing this project and what you would have done differently. (Maximum half a page)