Problem 1

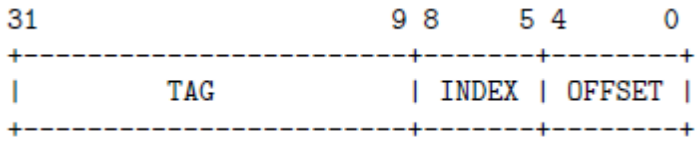
Verilog based design. A working version of direct mapped cache might be uploaded later

Problem 3

1.

- Number of cache lines = size / blocksize = 512 / 32 = 16 lines
- Number of index bits = log_2 (number of lines) = 4 bits
- Number of offset bits = log_2 (blocksize) = 5 bits
- Number of Tag bits = 32 bit address – 4 bit index – 5 bit offset = 23 bits

Address layout is shown in the diagram below



2. See table below (All values in HEX)

ADDRESS	TAG	INDEX	OFFSET	HIT / MISS	MISS TYPE
0x0001B596	0x0000DA	C	16	M	Compulsory
0x000092E8	0x000049	7	08	M	Compulsory
0x00000EF4	0x000007	7	14	M	Conflict
0x00004182	0x000020	C	02	M	Conflict
0x0000780A	0x00003C	0	0A	M	Compulsory
0x0000A690	0x000053	4	10	M	Compulsory
0x0000408E	0x000020	4	0E	M	Conflict
0x0000A798	0x000053	C	18	M	Conflict
0x00007800	0x00003C	0	00	H	-
0x000092FC	0x000049	7	1C	M	Conflict

3. Contents of the address tags is shown below

INDEX	TAG
0	0x00003C
4	0x000020
7	0x000049
C	0x000053

4.

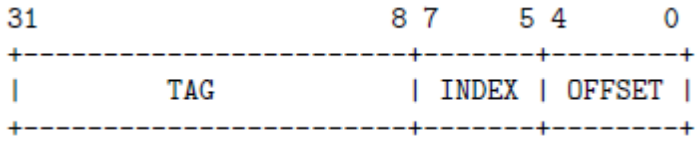
(a) Compulsory misses – Can be reduced by increasing the block size
(b) Conflict misses – Can be reduced by increasing the associativity
(c) Capacity misses – Can be reduced by increasing the cache size

Problem 4

1.

- Number of cache lines = size / blocksize = 512 / 32 = 16 lines
- Number of index bits = log_2 (number of lines / number of ways) = 3 bits
- Number of offset bits = log_2 (blocksize) = 5 bits
- Number of Tag bits = 32 bit address – 3 bit index – 5 bit offset = 24 bits

Address layout is shown in the diagram below



2. See the table below (All values in HEX)

ADDRESS	TAG	INDEX	OFFSET	HIT / MISS	MISS TYPE
0x0001B596	0x0001B5	4	16	M	Compulsory
0x000092E8	0x000092	7	08	M	Compulsory
0x00000EF4	0x00000E	7	14	M	Compulsory
0x00004182	0x000041	4	02	M	Compulsory
0x0000780A	0x000078	0	0A	M	Compulsory
0x0000A690	0x0000A6	4	10	M	Conflict
0x0000408E	0x000040	4	0E	M	Conflict
0x0000A798	0x0000A7	4	18	M	Conflict
0x00007800	0x000078	0	00	H	-
0x000092FC	0x000092	7	1C	H	-

3. Contents of the address tags is shown below

INDEX	TAG 1	TAG 2
0	0x000078	-
4	0x0000A7	0x000040
7	0x000092	0x00000E

4. (NOTE: Here 8 and 9 refer to the number of misses)
Average CPI of Direct Mapped Cache = [(1 + (25 * 9)) / 10] = 22.6
Average CPI of Seat Associative Cache = [((1*2) + (25 * 8)) / 10] = 20.2

Speedup = 22.6 / 20.2 = 1.119

Problem 5

1. Total storage = 64 byte blocks * 512 sets * 5 –ways = 163840 bytes (160 KB)
   Note that this follows the formula $\#\ of\ sets = \frac{\text{size}}{\text{blocksize X associativity}}$

2.
   Tag bits = 41 bit address – (# of index bits) – (# of offset bits)
   = 41 – log_2(512) - log_2(64)
   = 41 -9 -6
   = 26 bits

   Line size = valid bit + dirty bit + LRU bits + tag bits + data
   = 1 + 1 + 2 + 26 + (64 * 8 bits)
   = 542 bits

   Cache size = (# of ways) * (# of sets) * (line size)
   = 5 * 512 * 542
   = 1387520 bits