U. Wisconsin CS/ECE 752
Advanced Computer Architecture I

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Unit 3: Pipelining

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This Unit: Pipelining

- Basic Pipelining
  - Single, in-order issue
  - Clock rate vs. IPC
- Data Hazards
  - Hardware: stalling and bypassing
  - Software: pipeline scheduling
- Control Hazards
  - Branch prediction
- Precise state
Quick Review

- **Basic datapath**: fetch, decode, execute
- **Single-cycle control**: hardwired
  + Low CPI (1)
    - Long clock period (to accommodate slowest instruction)
- **Multi-cycle control**: micro-programmed
  + Short clock period
  - High CPI
- Can we have both low CPI and short clock period?
  - Not if datapath executes only one instruction at a time
  - No good way to make a single instruction go faster
Pipelining

- Important performance technique
  - **Improves instruction throughput rather instruction latency**
- Begin with multi-cycle design
  - When instruction advances from stage 1 to 2
  - Allow next instruction to enter stage 1
  - Form of parallelism: “insn-stage parallelism”
  - Individual instruction takes the same number of stages
  + **But instructions enter and leave at a much faster rate**
- Automotive assembly line analogy
5 Stage Pipelined Datapath

- Temporary values (PC, IR, A, B, O, D) re-latched every stage
  - Why? 5 insns may be in pipeline at once, they share a single PC?
  - Notice, PC not latched after ALU stage (why not?)
Pipeline Terminology

- Five stage: **Fetch**, **Decode**, **eXecute**, **Memory**, **Writeback**
  - Nothing magical about the number 5 (Pentium 4 has 22 stages)
- Latches (pipeline registers) named by stages they separate
  - **PC**, **F/D**, **D/X**, **X/M**, **M/W**
Pipeline Control

- One single-cycle controller, but pipeline the control signals
This is an **integer pipeline**
- Execution stages are X,M,W

Usually also one or more **floating-point (FP) pipelines**
- Separate FP register file
- One “pipeline” per functional unit: E+, E*, E/
  - “Pipeline”: functional unit need not be pipelined (e.g., E/)
- Execution stages are E+, E+’, W (no M)
Floating Point Pipelines
• **Pipeline diagram**
  - Cycles across, insns down
  - Convention: X means `ld r4,0(r5)` finishes execute stage and writes into X/M latch at end of cycle 4

• **Reverse stream analogy**
  - “Downstream”: earlier stages, younger insns
  - “Upstream”: later stages, older insns
  - Reverse? instruction stream fixed, pipeline flows over it
    - Architects see instruction stream as fixed by program/compiler
Pipeline Performance Calculation

- Back of the envelope calculation
  - Branch: 20%, load: 20%, store: 10%, other: 50%

- Single-cycle
  - Clock period = 50ns, CPI = 1
  - Performance = 50ns/insn

- Pipelined
  - Clock period = 12ns
  - CPI = 1 (each insn takes 5 cycles, but 1 completes each cycle)
  - Performance = 12ns/insn
Principles of Pipelining

- Let: insn execution require $N$ stages, each takes $t_n$ time
- Single-cycle execution
  - $L_1$ (1_insn latency) = $\Sigma t_n$
  - $T$ (throughput) = $1/L_1$
  - $L_M$ (M_insn latency, where $M >> 1) = M* L_1$

- Now: $N$-stage pipeline
  - $L_{1+P} = L_1$
  - $T_{+P} = 1/\max(t_n) \leq N/L_1$
  - If $t_n$ are equal (i.e., $\max(t_n) = L_1/N$), throughput = $N/L_1$
  - $L_{M+P} = M*\max(t_n) \geq M* L_1/N$
  - $S_{+P}$ (speedup) = $[M*L_1 / (\geq M*L_1/N)] = \leq N$

- Q: for arbitrarily high speedup, use arbitrarily high $N$?
No, Part I: Pipeline Overhead

- Let: $O$ be extra delay per pipeline stage
  - Latch overhead: pipeline latches take time
  - Clock/data skew

- Now: N-stage pipeline with overhead
  - Assume $\max(t_n) = L_1/N$
  - $L_{1+P+O} = L_1 + N*O$
  - $T_{+P+O} = 1/(L_1/N + O) = 1/(1/T + O) \leq T, \leq T/O$
  - $L_{M+P+O} = M*L_1/N + M*O = L_{M+P} + M*O$
  - $S_{+P+O} = [M*L_1 / (M*L_1/N + M*O)] = \leq N = S_{+P}, \leq L_1/O$

- $O$ limits throughput and speedup $\rightarrow$ useful $N$
No, Part II: Hazards

- **Dependence:** relationship that serializes two insns
  - **Data:** two insns use the same value or storage location
  - **Control:** one instruction affects whether another executes at all
  - **Maybe:** two insns *may* have a dependence

- **Hazard:** dependence causes potential incorrect execution
  - Possibility of using or corrupting data or execution flow
  - **Structural:** two insns want to use same structure, one must wait
  - Often fixed with **stalls:** insn stays in same stage for multiple cycles

- Let: **H** be average number of hazard stall cycles per instruction
  - \( L_{1+P+H} = L_{1+P} \) (no hazards for one instruction)
  - \( T_{+P+H} = \left[ N/(N+H) \right] * N/L_1 = \left[ N/(N+H) \right] * T_P \)
  - \( L_{M+P+H} = M * L_1/N * \left[ (N+H)/N \right] = \left[ (N+H)/N \right] * L_{M+P} \)
  - \( S_{+P+H} = M*L_1 / M*L_1/N*\left[ (N+H)/N \right] = \left[ N/(N+H) \right]*S_P \)

- **H** also limit throughput, speedup \(\rightarrow\) useful \(N\)
  - \(N\uparrow\rightarrow H\uparrow\) (more insns “in flight” \(\rightarrow\) more dependences become hazards)
  - Exact \(H\) depends on program, requires detailed simulation/model
Clock Rate vs. IPC

- Deeper pipeline (bigger N)
  - + frequency↑
  - - IPC↓
    - Ultimate metric is $IPC \times frequency$
      - But Intel got people to buy frequency, not $IPC \times frequency$
- Trend has been for deeper pipelines
  - Intel example:
    - 486: 5 stages (50+ gate delays / clock)
    - Pentium: 7 stages
    - Pentium II/III: 12 stages
    - Pentium 4: 22 stages (10 gate delays / clock)
    - 800 MHz Pentium III was faster than 1 GHz Pentium4
    - Intel Core2: 14 stages, less than Pentium 4
Optimizing Pipeline Depth

- Parameterize clock cycle in terms of gate delays
  - G gate delays to process (fetch, decode, execute) a single insn
  - O gate delays overhead per stage
  - X average stall per instruction per stage
    - Simplistic: real X function much, much more complex

- Compute optimal N (pipeline stages) given G,O,X
  - $\text{IPC} = \frac{1}{1 + X \cdot N}$
  - $f = \frac{1}{G / N + O}$
  - Example: $G = 80$, $O = 1$, $X = 0.16$,

<table>
<thead>
<tr>
<th>N</th>
<th>$\text{IPC} = 1/(1+0.16\cdot N)$</th>
<th>freq=1/(80/N+1)</th>
<th>IPC*freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0.56</td>
<td>0.059</td>
<td>0.033</td>
</tr>
<tr>
<td>10</td>
<td>0.38</td>
<td>0.110</td>
<td>0.042</td>
</tr>
<tr>
<td>20</td>
<td>0.33</td>
<td>0.166</td>
<td>0.040</td>
</tr>
</tbody>
</table>

Optimizes performance!

What about power?
Managing a Pipeline

- Proper flow requires two pipeline operations
  - Mess with latch write-enable and clear signals to achieve

- Operation I: **stall**
  - Effect: stops some insns in their current stages
  - Use: make younger insns wait for older ones to complete
  - Implementation: de-assert write-enable

- Operation II: **flush**
  - Effect: removes insns from current stages
  - Use: see later
  - Implementation: assert clear signals

- Both stall and flush must be propagated to younger insns
Structural Hazards

- **Structural hazard**: resource needed twice in one cycle
  - Example: shared I/D$
Fixing Structural Hazards

<table>
<thead>
<tr>
<th>Instruction</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>ld r2,0(r1)</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>add r1,r3,r4</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>sub r1,r3,r5</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>and r6,r1,r2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>s*</td>
<td>F</td>
<td>D</td>
<td>X</td>
</tr>
</tbody>
</table>

- Can fix structural hazards by stalling
  - **s* =** structural stall
  - Q: which one to stall: `ld` or `and`?
    - Always safe to stall younger instruction (here `and`)
      - Fetch stall logic: `(X/M.op == ld || X/M.op == st)`
      - But not always the best thing to do performance wise (?)
- Low cost, simple
- Decreases IPC
- Upshot: better to avoid by design than to fix
Avoiding Structural Hazards (PRS)

- **Pipeline** the contended resource
  - No IPC degradation, low area, power overheads
  - Sometimes tricky to implement (e.g., for RAMs)
  - For multi-cycle resources (e.g., multiplier)

- **Replicate** the contended resource
  - No IPC degradation
  - Increased area, power, latency (interconnect delay?)
  - For cheap, divisible, or highly contended resources (e.g., I$/$D$)

- **Schedule** pipeline to reduce structural hazards (RISC)
  - Design ISA so insn uses a resource at most once
    - Eliminate same insn hazards
  - Always in same pipe stage (hazards between two of same insn)
    - Reason why integer operations forced to go through M stage
  - And always for one cycle
Data Hazards

• Real insn sequences pass values via registers/memory
  • Three kinds of **data dependences** (where’s the fourth?)

<table>
<thead>
<tr>
<th>RAW</th>
<th>WAR</th>
<th>WAW</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>add r2, r3 → r1</code></td>
<td><code>add r2, r3 → r1</code></td>
<td><code>add r2, r3 → r1</code></td>
</tr>
<tr>
<td><code>sub r1, r4 → r2</code></td>
<td><code>sub r5, r4 → r2</code></td>
<td><code>sub r1, r4 → r2</code></td>
</tr>
<tr>
<td><code>or r6, r3 → r1</code></td>
<td><code>or r6, r3 → r1</code></td>
<td><code>or r6, r3 → r1</code></td>
</tr>
<tr>
<td>Read-after-write (RAW)</td>
<td>Write-after-read (WAR)</td>
<td>Write-after-write (WAW)</td>
</tr>
<tr>
<td>True-dependence</td>
<td>Anti-dependence</td>
<td>Output-dependence</td>
</tr>
</tbody>
</table>

• Only one dependence between any two insns (RAW has priority)
• Dependence is property of the program and ISA

• **Data hazards**: function of data dependences and pipeline
  • Potential for executing dependent insns in wrong order
  • Require both insns to be in pipeline (“in flight”) simultaneously
Dependences and Loops

- Data dependences in loops
  - **Intra-loop**: within same iteration
  - **Inter-loop**: across iterations
  - Example: DAXPY (Double precision $A \times X$ Plus $Y$)

```plaintext
for (i=0; i<100; i++)
    Z[i] = A*X[i] + Y[i];
```

```
0: ldf  f2,X(r1)
1: mulf f2,f0,f4
dataf  f4,f6,f8
3: addf f4,f6,f8
4: stf  f8,Z(r1)
5: addi r1,8,r1
6: cmplti r1,800,r2
7: beq r2,Loop
```

- RAW intra: $0 \rightarrow 1(f2), 1 \rightarrow 3(f4), 2 \rightarrow 3(f6), 3 \rightarrow 4(f8), 5 \rightarrow 6(r1), 6 \rightarrow 7(r2)$
- RAW inter: $5 \rightarrow 0(r1), 5 \rightarrow 2(r1), 5 \rightarrow 4(r1), 5 \rightarrow 5(r1)$
- WAR intra: $0 \rightarrow 5(r1), 2 \rightarrow 5(r1), 4 \rightarrow 5(r1)$
- WAR inter: $1 \rightarrow 0(f2), 3 \rightarrow 1(f4), 3 \rightarrow 2(f6), 4 \rightarrow 3(f8), 6 \rightarrow 5(r1), 7 \rightarrow 6(r2)$
- WAW intra: none
- WAW inter: $0 \rightarrow 0(f2), 1 \rightarrow 1(f4), 2 \rightarrow 2(f6), 3 \rightarrow 3(f8), 6 \rightarrow 6(r2)$
Read-after-write (RAW)

- **Problem**: swap would mean `sub` uses wrong value for `r1`
- **True**: value flows through this dependence
  - Using different output register for `add` doesn’t help
**Stall logic**: detect and stall reader in D

\[(F/D.rs1 & (F/D.rs1==D/X.rd \; | \; F/D.rs1==X/M.rd \; | \; F/D.rs1==M/W.rd)) \; | \; (F/D.rs2 & (F/D.rs2==D/X.rd \; | \; F/D.rs2==X/M.rd \; | \; F/D.rs2==M/W.rd))\]

- Re-evaluated every cycle until no longer true
  + Low cost, simple
  - IPC degradation, dependences are the common case
Two Stall Timings (without bypassing)

- Depend on how D and W stages share regfile
  - Each gets regfile for half a cycle
    - 1st half D reads, 2nd half W writes 3 cycle stall
  - \( d^* \) = data stall, \( p^* \) = propagated stall

\[
\begin{array}{cccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
\hline
\text{add } r2, r3 \rightarrow r1 & F & D & X & M & W \\
\text{sub } r1, r4 \rightarrow r2 & F & d^* & d^* & d^* & D & X & M & W \\
\text{add } r5, r6 \rightarrow r7 & F & d^* & d^* & d^* & D & X & M & W \\
\end{array}
\]

+ 1st half W writes, 2nd half D reads 2 cycle stall

- How does the stall logic change here?

\[
\begin{array}{cccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
\hline
\text{add } r2, r3 \rightarrow r1 & F & D & X & M & W \\
\text{sub } r1, r4 \rightarrow r2 & F & d^* & d^* & D & X & M & W \\
\text{add } r5, r6 \rightarrow r7 & F & p^* & p^* & F & D & X & M & W \\
\end{array}
\]
Reducing RAW Stalls with Bypassing

- Why wait until W stage? Data available after X or M stage
  - Bypass (aka forward) data directly to input of X or M
    - MX: from beginning of M (X output) to input of X
    - WX: from beginning of W (M output) to input of X
    - WM: from beginning of W (M output) to data input of M
  - Two each of MX, WX (figure shows 1) + WM = full bypassing
    + Reduces stalls in a big way
    - Additional wires and muxes may increase clock cycle
Bypass Logic

- Bypass logic: similar to but separate from stall logic
  - Stall logic controls latches, bypass logic controls mux inputs
  - Complement one another: can't bypass → must stall
  - ALU input mux bypass logic
    - \((D/X.rs2 \& X/M.rd==D/X.rs2) \rightarrow 2\)  // check first
    - \((D/X.rs2 \& M/W.rd==D/X.rs2) \rightarrow 1\)  // check second
    - \((D/X.rs2) \rightarrow 0\)  // check last
Pipeline Diagrams with Bypassing

- If bypass exists, “from”/“to” stages execute in same cycle
  - Example: full bypassing, use MX bypass
    
    \[
    \begin{array}{cccccccccc}
    1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
    \text{add } r_2,r_3 \rightarrow r_1 & F & D & X & M & W \\
    \text{sub } r_1,r_4 \rightarrow r_2 & F & D & X & M & W \\
    \end{array}
    \]

- Example: full bypassing, use WX bypass
  
  \[
  \begin{array}{cccccccccc}
  1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
  \text{add } r_2,r_3 \rightarrow r_1 & F & D & X & M & W \\
  \text{ld } [r_7] \rightarrow r_5 & F & D & X & M & W \\
  \text{sub } r_1,r_4 \rightarrow r_2 & F & D & X & M & W \\
  \end{array}
  \]

- Example: WM bypass
  
  \[
  \begin{array}{cccccccccc}
  1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
  \text{add } r_2,r_3 \rightarrow r_1 & F & D & X & M & W \\
  ? & F & D & X & M & W \\
  \end{array}
  \]

- Can you think of a code example that uses the WM bypass?
Load-Use Stalls

- Even with full bypassing, stall logic is unavoidable
  - **Load-use stall**
    - Load value not ready at beginning of M → can’t use MX bypass
    - Use WX bypass

\[
\begin{array}{ccccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
\text{ld } [r3+4] & \rightarrow r1 & F & D & X & M & W \\
\text{sub } r1, r4 & \rightarrow r2 & F & D & d^* & X & M & W \\
\end{array}
\]

- Aside: with WX bypassing, stall logic can be in D or X

\[
\begin{array}{ccccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
\text{ld } [r3+4] & \rightarrow r1 & F & D & X & M & W \\
\text{sub } r1, r4 & \rightarrow r2 & F & d^* & D & X & M & W \\
\end{array}
\]

- Aside II: how does stall/bypass logic handle cache misses?
Research: Razor

- **Razor** [Uht, Ernst+]
  - Identify pipeline stages with narrow signal margins (e.g., X)
  - Add “Razor” X/M latch: relatches X/M input signals after safe delay
  - Compare X/M latch with “safe” razor X/M latch, different?
    - Flush F,D,X & M
    - Restart M using X/M razor latch, restart F using D/X latch
  + Pipeline will not “break” → reduce $V_{DD}$ until flush rate too high
  + Alternatively: “over-clock” until flush rate too high
Compiler Scheduling

- Compiler can schedule (move) insns to reduce stalls
  - **Basic pipeline scheduling**: eliminate back-to-back load-use pairs
  - Example code sequence: \( a = b + c; \ d = f - e; \)
  - MIPS Notation:
    - “ld r2,4(sp)” is “ld [sp+4] \( \rightarrow \) r2”
    - “st r1, 0(sp)” is “st r1 \( \rightarrow [sp+0]\)”

Before

\[
\begin{align*}
\text{ld } r2,4 (sp) \\
\text{ld } r3,8 (sp) \\
\text{add } r3,r2,r1 & \quad //\text{stall} \\
\text{st } r1,0 (sp) \\
\text{ld } r5,16 (sp) \\
\text{ld } r6,20 (sp) \\
\text{sub } r5,r6,r4 & \quad //\text{stall} \\
\text{st } r4,12 (sp)
\end{align*}
\]

After

\[
\begin{align*}
\text{ld } r2,4 (sp) \\
\text{ld } r3,8 (sp) \\
\text{ld } r5,16 (sp) \\
\text{add } r3,r2,r1 & \quad //\text{no stall} \\
\text{ld } r6,20 (sp) \\
\text{st } r1,0 (sp) \\
\text{sub } r5,r6,r4 & \quad //\text{no stall} \\
\text{st } r4,12 (sp)
\end{align*}
\]
Compiler Scheduling Requires

- **Large scheduling scope**
  - Independent instruction to put between load-use pairs
    - Original example: large scope, two independent computations
    - This example: small scope, one computation

```
Before
ld r2,4(sp)
ld r3,8(sp)
add r3,r2,r1  //stall
st r1,0(sp)

After
ld r2,4(sp)
ld r3,8(sp)
add r3,r2,r1  //stall
st r1,0(sp)
```
Compiler Scheduling Requires

- **Enough registers**
  - To hold additional “live” values
  - Example code contains 7 different values (including sp)
  - Before: max 3 values live at any time → 3 registers enough
  - After: max 4 values live → 3 registers not enough → WAR violations

Original

```
ld r2, 4(sp)
ld r1, 8(sp)
add r1, r2, r1 //stall
st r1, 0(sp)
ld r2, 16(sp)
ld r1, 20(sp)
sub r2, r1, r1 //stall
st r1, 12(sp)
```

Wrong!

```
ld r2, 4(sp)
ld r1, 8(sp)
add r1, r2, r1 //WAR
ld r2, 16(sp)
add r1, r2, r1 //WAR
ld r1, 20(sp)
st r1, 0(sp) //WAR
sub r2, r1, r1 //stall
sub r2, r1, r1
st r1, 12(sp)
```
Compiler Scheduling Requires

- **Alias analysis**
  - Ability to tell whether load/store reference same memory locations
  - Effectively, whether load/store can be rearranged
  - Example code: easy, all loads/stores use same base register \((sp)\)
  - New example: can compiler tell that \(r8 = sp\)?

Before

\[
\begin{align*}
\text{ld } r2,4 (sp) \\
\text{ld } r3,8 (sp) \\
\text{add } r3,r2,r1  \quad \text{//stall} \\
\text{st } r1,0 (sp) \\
\text{ld } r5,0 (r8) \\
\text{ld } r6,4 (r8) \\
\text{sub } r5,r6,r4  \quad \text{//stall} \\
\text{st } r4,8 (r8)
\end{align*}
\]

Wrong(?)

\[
\begin{align*}
\text{ld } r2,4 (sp) \\
\text{ld } r3,8 (sp) \\
\text{ld } r5,0 (r8) \\
\text{add } r3,r2,r1  \quad \text{//stall} \\
\text{ld } r6,4 (r8) \\
\text{st } r1,0 (sp) \\
\text{sub } r5,r6,r4  \quad \text{//stall} \\
\text{st } r4,8 (r8)
\end{align*}
\]
WAW Hazards

• **Write-after-write (WAW)**
  
  ```
  add r2, r3, r1
  sub r1, r4, r2
  or r6, r3, r1
  ```

• **Compiler effects**
  
  • Scheduling problem: reordering would leave wrong value in `r1`
  
  • Later instruction reading `r1` would get wrong value
  
  • **Artificial**: no value flows through dependence

  • Eliminate using different output register name for `or`

• **Pipeline effects**
  
  • Doesn’t affect in-order pipeline with single-cycle operations

  • One reason for making ALU operations go through M stage

  • Can happen with multi-cycle operations (e.g., FP or cache misses)
Handling WAW Hazards

- What to do?
  - Option I: stall younger instruction (\texttt{addf}) at writeback
    + Intuitive, simple
    - Lower performance, cascading W structural hazards
  - Option II: cancel older instruction (\texttt{divf}) writeback
    + No performance loss
    - What if \texttt{divf} or \texttt{stf} cause an exception (e.g., /0, page fault)?
## Handling Interrupts/Exceptions

- How are interrupts/exceptions handled in a pipeline?
  - **Interrupt**: external, e.g., timer, I/O device requests
  - **Exception**: internal, e.g., /0, page fault, illegal instruction
  - We care about **restartable** interrupts (e.g. `stf` page fault)

```
\[
\begin{array}{c|cccccccccc}
 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 \\
\hline
divf f0, f1 \rightarrow f2 & F & D & E/ & E/ & E/ & E/ & E/ & W \\
stf f2 \rightarrow [r1] & F & D & d* & d* & d* & X & M & W \\
addf f0, f1 \rightarrow f2 & F & D & E+ & E+ & W \\
\end{array}
\]
```

- **VonNeumann** says
  - “Insn execution should appear sequential and atomic”
    - Insn X should complete before instruction X+1 should begin
    - Doesn’t physically have to be this way (e.g., pipeline)
  - But be ready to restore to this state at a moments notice
  - Called **precise state** or **precise interrupts**
Handling Interrupts

- In this situation
  - Make it appear as if `divf` finished and `stf`, `addf` haven’t started
  - Allow `divf` to writeback
  - **Flush** `stf` and `addf` (so that’s what a flush is for)
    - But `addf` has already written back
      - Keep an “undo” register file? Complicated
      - Force in-order writebacks? Slow
      - Other solutions? Later
  - Invoke exception handler
  - Restart `stf`
More Interrupt Nastiness

• What about two simultaneous in-flight interrupts
  • Example: \texttt{stf} page fault, \texttt{divf} /0
  • Interrupts must be handled in program order (\texttt{stf} first)
    • Handler for \texttt{stf} must see program as if \texttt{divf} hasn’t started
    • Must defer interrupts until writeback and force in-order writeback

• In general: interrupts are really nasty
  • Some processors (Alpha) only implement precise integer interrupts
  • Easier because fewer WAW scenarios
  • Most floating-point interrupts are non-restartable anyway
    • \texttt{divf} /0 \rightarrow rescale computation to prevent underflow
    • Typically doesn’t restart computation at excepting instruction

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<tbody>
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<td>\texttt{stf f2\rightarrow [r1]}</td>
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<td>\texttt{divf f0,f4\rightarrow f2}</td>
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Research: Runahead Execution

- In-order writebacks essentially imply stalls on D$ misses
  - Can save power ... or use idle time for performance

- Runahead execution [Dundas+]
  - Shadow regfile kept in sync with main regfile (write to both)
  - D$ miss: continue executing using shadow regfile (disable stores)
  - D$ miss returns: flush pipe and restart with stalled PC
  + Acts like a smart prefetch engine
  + Performs better as cache $t_{miss}$ grows (relative to clock period)
WAR Hazards

- **Write-after-read (WAR)**
  
  \[
  \begin{align*}
  &\text{add } r2, r3, r1 \\
  &\text{sub } r5, r4, r2 \\
  &\text{or } r6, r3, r1
  \end{align*}
  \]

- **Compiler effects**
  
  - Scheduling problem: reordering would mean \texttt{add} uses wrong value for \texttt{r2}
  - \textbf{Artificial}: solve using different output register name for \texttt{sub}

- **Pipeline effects**
  
  - Can’t happen in simple in-order pipeline
  - Can happen with out-of-order execution
Memory Data Hazards

• So far, have seen/dealt with register dependences
  • Dependences also exist through memory

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<td>ld [r1]⇒r4</td>
<td>ld [r1]⇒r4</td>
<td>ld [r1]⇒r4</td>
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<td>st r5⇒[r1]</td>
<td>st r5⇒[r1]</td>
<td>st r5⇒[r1]</td>
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<tr>
<td>Read-after-write (RAW)</td>
<td>Write-after-read (WAR)</td>
<td>Write-after-write (WAW)</td>
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• But in an in-order pipeline like ours, they do not become hazards
• Memory read and write happen at the same stage
  • Register read happens three stages earlier than register write
• In general: memory dependences more difficult than register

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<td>ld [r1]⇒r4</td>
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<tr>
<td>1 2 3 4 5 6 7 8 9 10</td>
<td>F  D  X  M  W</td>
<td>F  D  X  M  W</td>
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CS/ECE 725 (Wood): Pipelining
Control Hazards

- **Control hazards**
  - Must fetch post branch insns before branch outcome is known
  - Default: assume "not-taken" (at fetch, can’t tell it’s a branch)
  - Control hazards indicated with c* (or not at all)
  - Taken branch penalty is 2 cycles

Back of the envelope calculation
- **Branch: 20%**, other: 80%, **75% of branches are taken**
- CPI\(_{\text{BASE}}\) = 1
- CPI\(_{\text{BASE+BRANCH}}\) = 1 + 0.20*0.75*2 = 1.3
  - **Branches cause 30% slowdown**
ISA Branch Techniques

- **Fast branch**: resolves at D, not X
  - Test must be comparison to zero or equality, no time for ALU
    + New taken branch penalty is 1
    - Additional comparison insns (e.g., `cmpl`, `slt`) for complex tests
    - Must bypass into decode now, too

- **Delayed branch**: branch that takes effect one insn later
  - Insert insns that are independent of branch into “branch delay slot”
  - Preferably from before branch (always helps then)
  - But from after branch OK too
    - As long as no undoable effects (e.g., a store)
  - Upshot: short-sighted feature (MIPS regrets it)
    - Not a big win in today’s pipelines
    - Complicates interrupt handling
Big Idea: Speculation

- **Speculation**
  - “Engagement in risky transactions on the chance of profit”

- **Speculative execution**
  - Execute before all parameters known with certainty

- **Correct speculation**
  - Avoid stall, improve performance

- **Incorrect speculation (mis-speculation)**
  - Must abort/flush/squash incorrect instructions
  - Must undo incorrect changes (recover pre-speculation state)

The “game”: $[\%_{\text{correct}} \times \text{gain}] > [(1-\%_{\text{correct}}) \times \text{penalty}]$
Control Hazards: Control Speculation

- Deal with control hazards with **control speculation**
  - Unknown parameter: are these the correct insns to execute next?
- Mechanics
  - Guess branch target, start fetching at guessed position
  - Execute branch to verify (check) guess
    - Correct speculation? keep going
    - Mis-speculation? Flush mis-speculated insns
  - Don’t write registers or memory until prediction verified
- Speculation game for in-order 5 stage pipeline
  - Gain = 2 cycles
  - Penalty = 0 cycles
    - No penalty → mis-speculation no worse than stalling
  - $\%_{\text{correct}} = \text{branch prediction}$
    - Static (compiler) $\sim$85%, **dynamic** (hardware) $>$95%
    - Not much better? Static has 3X mispredicts!
Control Speculation and Recovery

- **Mis-speculation recovery**: what to do on wrong guess
  - Not too painful in an in-order pipeline
  - Branch resolves in X
  - Younger insns (in F, D) haven’t changed permanent state
- **Flush** insns currently in F/D and D/X (i.e., replace with nops)

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### Correct:

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### Recovery:

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CS/ECE 725 (Wood): Pipelining
Dynamic Branch Prediction

- **BP part I: target predictor**
  - Applies to all control transfers
  - Supplies target PC, tells if insn is a branch prior to decode
    + Easy
- **BP part II: direction predictor**
  - Applies to conditional branches only
  - Predicts taken/not-taken
    - Harder
Branch Target Buffer

- **Branch target buffer (BTB)**
  - A small cache: address = PC, data = target-PC
    - Hit? This is a control insn and it’s going to target-PC (if “taken”)
    - Miss? Not a control insn, or one I have never seen before
  - Partial data/tags: full tag not necessary, target-PC is just a guess
    - **Aliasing**: tag match, but not actual match (OK for BTB)
  - Pentium4 BTB: 2K entries, 4-way set-associative
Why Does a BTB Work?

- Because control insn targets are stable
  - **Direct** means constant target, **indirect** means register target
    + Direct conditional branches? Check
    + Direct calls? Check
    + Direct unconditional jumps? Check
    
    + Indirect conditional branches? Not that useful → not widely supported
  - Indirect calls? Two idioms
    + Dynamically linked functions (DLLs)? Check
    + Dynamically dispatched (virtual) functions? Pretty much check
  - Indirect unconditional jumps? Two idioms
    - Switches? Not really, but these are rare
    - Returns? Nope, but...
Return Address Stack (RAS)

- Return addresses are easy to predict without a BTB
  - Hardware return address stack (RAS) tracks call sequence
  - Calls push PC+4 onto RAS
  - Prediction for returns is RAS[TOS]
  - Q: how can you tell if an insn is a return before decoding it?
    - A1: Add tags to make RAS a cache
    - A2: (Better) attach pre-decode bits to I$
      - Written after first time insn executes
      - Two useful bits: return?, conditional-branch?
Branch Direction Prediction

- **Direction predictor (DIRP)**
  - Map conditional-branch PC to taken/not-taken (T/N) decision
  - Seemingly innocuous, but quite difficult to do well
  - Individual conditional branches often unbiased or weakly biased
    - 90%+ one way or the other considered “biased”
Branch History Table (BHT)

- **Branch history table (BHT):** simplest direction predictor
  - PC indexes table of bits (0 = N, 1 = T), no tags
  - Essentially: branch will go same way it went last time
  - Problem: consider *inner loop branch* below (* = mis-prediction)

```plaintext
for (i=0; i<100; i++)
    for (j=0; j<3; j++)
        // whatever
```

<table>
<thead>
<tr>
<th>State/prediction</th>
<th>N*</th>
<th>T</th>
<th>T</th>
<th>T*</th>
<th>N*</th>
<th>T</th>
<th>T</th>
<th>T*</th>
<th>N*</th>
<th>T</th>
<th>T</th>
<th>T*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outcome</td>
<td>T</td>
<td>T</td>
<td>T</td>
<td>T</td>
<td>N</td>
<td>T</td>
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<td>T</td>
<td>N</td>
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</table>

- Two “built-in” mis-predictions per inner loop iteration
- Branch predictor “changes its mind too quickly”
Two-Bit Saturating Counters (2bc)

- **Two-bit saturating counters (2bc) [Smith]**
  - Replace each single-bit prediction
    - \((0,1,2,3) = (N,n,t,T)\)
  - Force DIRP to mis-predict twice before “changing its mind”

<table>
<thead>
<tr>
<th>State/prediction</th>
<th>(N^*)</th>
<th>(n^*)</th>
<th>(t)</th>
<th>(T^*)</th>
<th>(t)</th>
<th>(T)</th>
<th>(T)</th>
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<tr>
<td>Outcome</td>
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+ Fixes this pathology (which is not contrived, by the way)
Correlated Predictor

- **Correlated (two-level) predictor** [Patt]
  - Exploits observation that branch outcomes are correlated
  - Maintains separate prediction per (PC, BHR)
    - **Branch history register (BHR):** recent branch outcomes
  - Simple working example: assume program has one branch
    - BHT: one 1-bit DIRP entry
    - BHT+2BHR: 4 1-bit DIRP entries

<table>
<thead>
<tr>
<th>State/prediction</th>
<th>BHR=NN</th>
<th>N*</th>
<th>T</th>
<th>T</th>
<th>T</th>
<th>T</th>
<th>T</th>
<th>T</th>
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<tr>
<td>&quot;active pattern&quot;</td>
<td>BHR=NT</td>
<td>N</td>
<td>N*</td>
<td>T</td>
<td>T</td>
<td>T</td>
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<td></td>
<td>BHR=TN</td>
<td>N</td>
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<td>N</td>
<td>N*</td>
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<td>BHR=TT</td>
<td>N</td>
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Correlated Predictor

- What happened?
  - BHR wasn’t long enough to capture the pattern
  - Try again: BHT+ 3BHR: 8 1-bit DIRP entries

<table>
<thead>
<tr>
<th>State/prediction</th>
<th>BHR=NNN</th>
<th>( \text{N*} )</th>
<th>T</th>
<th>T</th>
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<td>N</td>
<td>( \text{N*} )</td>
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<td>BHR=NTN</td>
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+ No mis-predictions after predictor learns all the relevant patterns
Correlated Predictor

- **Design choice I:** one *global* BHR or one per PC (*local*)?
  - Each one captures different kinds of patterns
  - Global is better, captures local patterns for tight loop branches

- **Design choice II:** how many history bits (BHR size)?
  - Tricky one
    - Longer BHRs are better for some apps, shorter better for others
      - BHT utilization decreases w/ long BHRs
        - Many history patterns are never seen
        - Many branches are history independent (don’t care)
  - PC $^\land$ BHR allows multiple PCs to dynamically share BHT
    - BHR length $< \log_2(\text{BHT size})$
  - Predictor takes longer to train
  - Typical length: 8–12
Hybrid Predictor

- **Hybrid (tournament) predictor** [McFarling]
  - Attacks correlated predictor BHT utilization problem
  - Idea: combine two predictors
    - **Simple BHT** predicts history independent branches
    - **Correlated predictor** predicts only branches that need history
    - **Chooser** assigns branches to one predictor or the other
  - Branches start in simple BHT, move mis-prediction threshold
  - Correlated predictor can be made smaller, handles fewer branches
  - 90–95% accuracy
Research: Perceptron Predictor

- **Perceptron predictor** [Jimenez]
  - Attacks BHR size problem using machine learning approach
  - BHT replaced by table of function coefficients $F_i$ (signed)
  - Predict taken if $\sum(BHR_i \cdot F_i) >$ threshold
  + Table size $\#PC \cdot |\text{BHR}| \cdot |F|$ (can use long BHR: $\sim60$ bits)
    - Equivalent correlated predictor would be $\#PC \cdot 2^{\text{BHR}}$
  - How does it learn? Update $F_i$ when branch is taken
    + $\text{BHR}_i == 1 \ ? \ F_i++ : F_i--$;
    + “don’t care” $F_i$ bits stay near 0, important $F_i$ bits saturate
  + Hybrid BHT/perceptron accuracy: 95–98%

---

![Diagram of Perceptron Predictor]
Branch Prediction Performance

- Same parameters
  - **Branch: 20%**, load: 20%, store: 10%, other: 50%
  - 75% of branches are taken
- Dynamic branch prediction
  - Branches predicted with 95% accuracy
  - CPI = 1 + 0.20*0.05*2 = **1.02**
Pipeline Performance Summary

- Base CPI is 1, but hazards increase it.

- Nothing magical about a 5 stage pipeline
  - Pentium4 has 22 stage pipeline

- Increasing **pipeline depth**
  - Increases clock frequency (that’s why companies do it)
    - But decreases IPC
  - Branch mis-prediction penalty becomes longer
    - More stages between fetch and whenever branch computes
  - Non-bypassed data hazard stalls become longer
    - More stages between register read and write
  - At some point, CPI losses offset clock gains, question is when?
Dynamic Pipeline Power

• Remember control-speculation game
  - \[2 \text{ cycles} \times \%_{\text{correct}}\] – \[0 \text{ cycles} \times (1-\%_{\text{correct}})\]
  - No penalty → mis-speculation no worse than stalling
  - This is a performance-only view
  - From a power standpoint, mis-speculation is worse than stalling

• Power control-speculation game
  - \[0 \text{ nJ} \times \%_{\text{correct}}\] – \[X \text{ nJ} \times (1-\%_{\text{correct}})\]
  - No benefit → correct speculation no better than stalling
    - Not exactly, increased execution time increases static power
  - How to balance the two?
Research: Speculation Gating

- **Speculation gating** [Manne+]
  - Extend branch predictor to give prediction + **confidence**
  - Speculate on high-confidence (mis-prediction unlikely) branches
  - Stall (save energy) on low-confidence branches

- **Confidence estimation**
  - What kind of hardware circuit estimates confidence?
  - Hard in absolute sense, but easy relative to given threshold
  - Counter-scheme similar to $\%_{miss}$ threshold for cache resizing
  - Example: assume 90% accuracy is high confidence
    - PC-indexed table of confidence-estimation counters
    - Prediction for PC is confident if table[PC] > 0;
Summary

- Principles of pipelining
  - Effects of overhead and hazards
  - Pipeline diagrams
- Data hazards
  - Stalling and bypassing
- Control hazards
  - Branch prediction
- Power techniques
  - Dynamic power: speculation gating
  - Static and dynamic power: razor latches