CS/ECE 755 VLSI SYSTEM DESIGN SPRING 1994
PROF. WOOD

Midterm Exam
In-Class -- March 23, 1994
Closed Book, Closed Notes

NAME: _____

DO NOT OPEN THE EXAM UNTIL TOLD TO DO SO!

Read over the entire exam before beginning. Verify that your exam includes all 8 pages. Use your time carefully. Budget your time according to the weight of the questions, and your ability to answer them. Limit your answers to the space provided, if possible. If not, write on the BACK OF THE SAME SHEET. Use the back of the sheet for scratch work. WRITE YOUR NAME ON EACH SHEET.

Problem 1 (15 points) _____

Problem 2 (10 points) _____

Problem 3 (15 points) _____

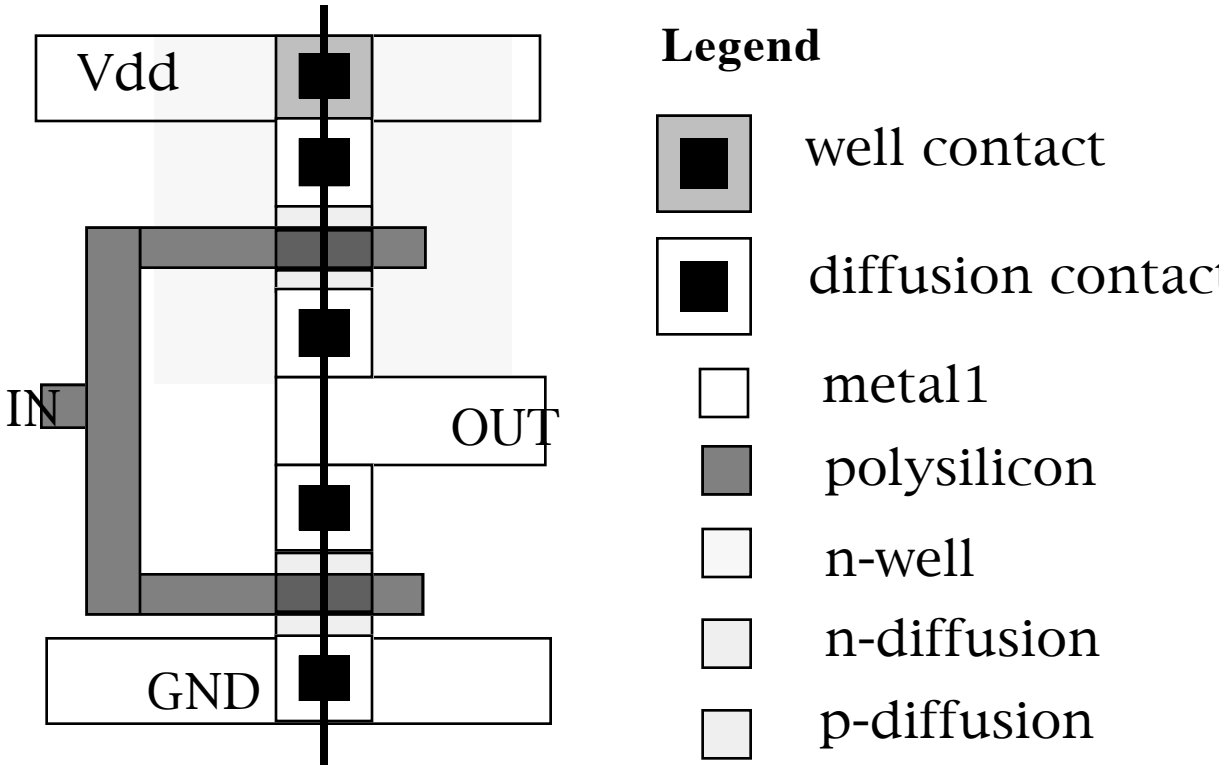
Problem 4 (20 points) _____

Problem 5 (20 points) _____

Total (80 points) _____

Problem 1 (15 points)

Draw the cross-sectional view of the CMOS inverter along the line shown in the figure below. Clearly label all layers and indicate all signal (node) names. Assume an n-well process.

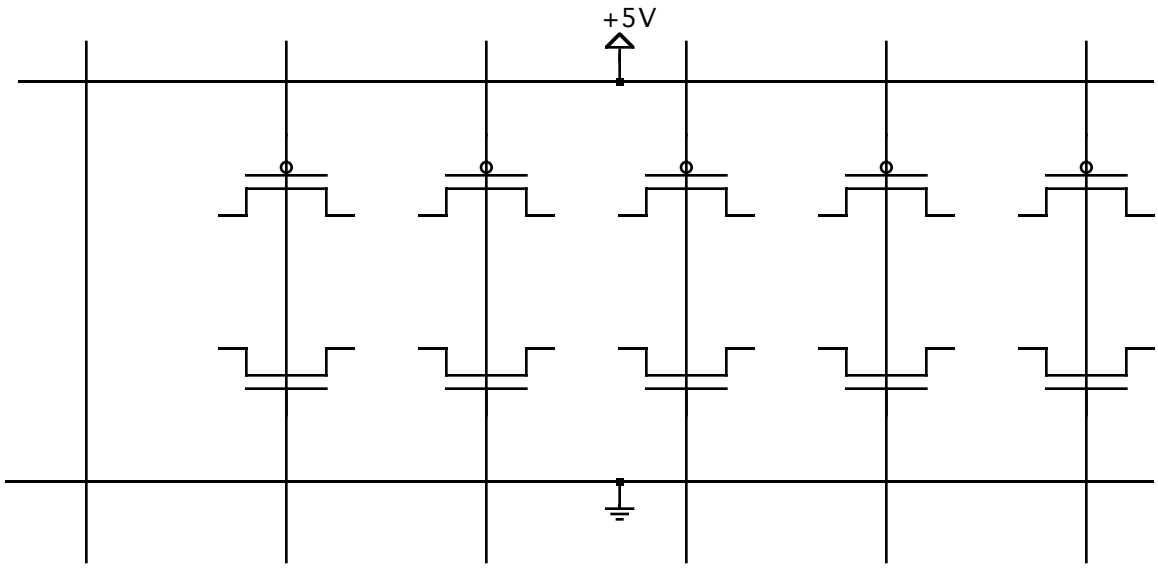


Problem 2 (10 points)

Connect the standard cell below so as to implement a full-complementary static-CMOS gate that implements the following logic function.

F(A,B,C) = A + BC'

Your interconnection is limited to two horizontal wiring tracks between the rows of n-type and p-type transistors and two wiring tracks between each pair of input wires (hence two adjacent transistors may connect to different signals). Horizontal wires run in metal1 and vertical wires run in metal2 (hence they can cross). The output must appear on the output pin (the leftmost vertical wire). You may assign the inputs to whichever vertical wires you prefer.



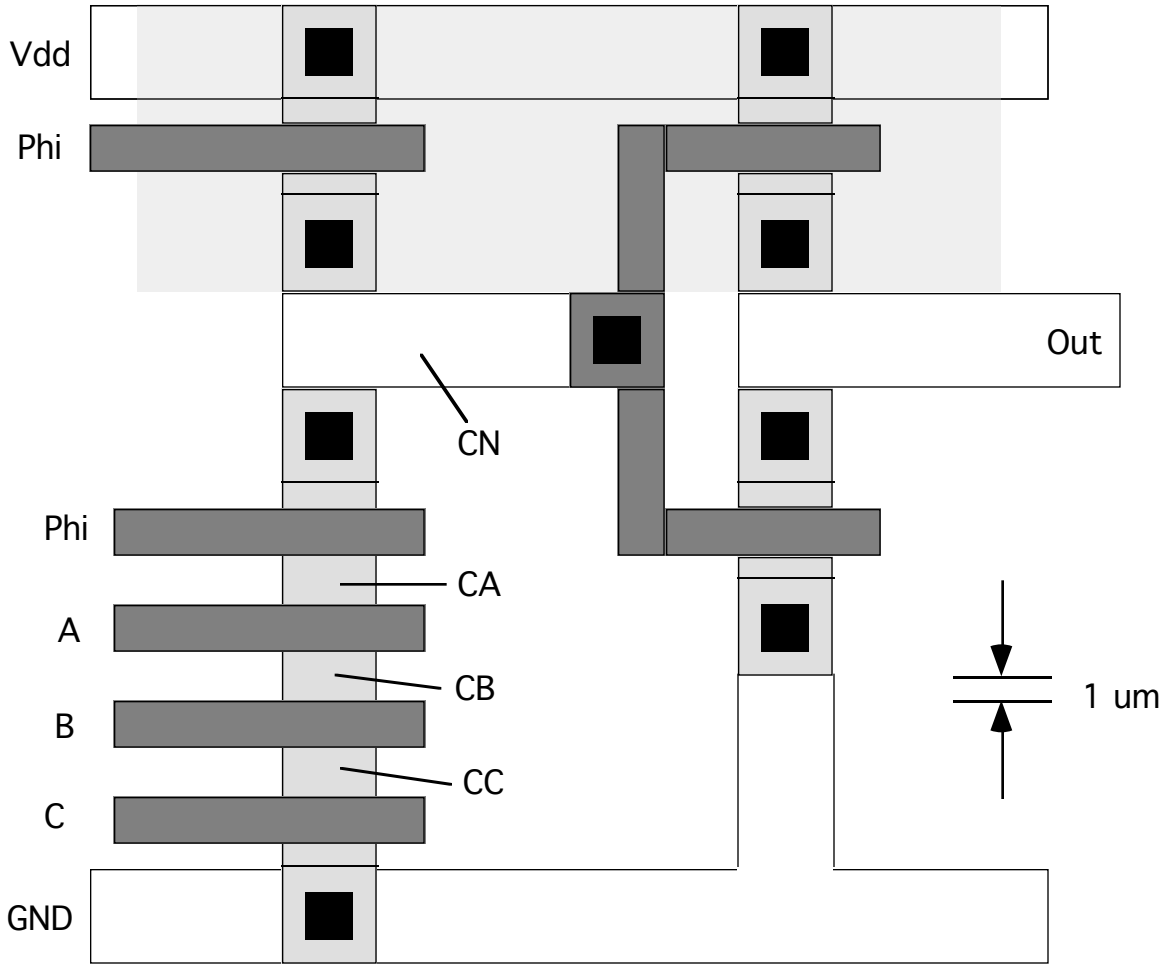
Problem 3 (15 points)

Part (a) (10 points)
What is a (4,2) counter? Give a schematic, truth-table, or other precise specification. What is it used for and why?

Part (b) (5 points)
Briefly, how does the Brent-Kung adder differ from the conventional carry-lookahead schemes long used in TTL designs?

Problem 4 (20 points)

Consider the 3-input Domino AND gate below. It is implemented in a 2μm (λ = 1μm) n-well process with the poly wires 2λ wide, transistors 4λ wide, and all metal wires 4λ wide. Poly-poly sp is 2λ.



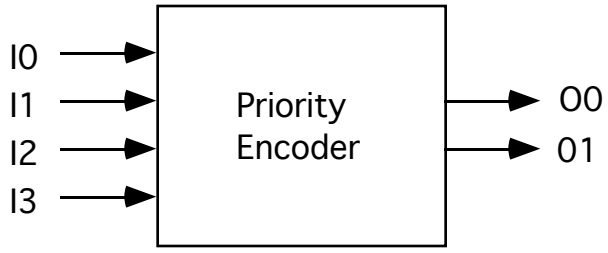
Part (a) (5 points)
Compute the capacitances of labeled nodes CA, CB, CC, and CN usi
the following values: gate oxide capacitance C_{ox} is 20 x 10^{-4} pF/
and both p-type and n-type diffusions have area capacitances
2 x 10^{-4} pF/μm^2 and periphery capacitances C_{jp} = 4 x 10^{-4} pF/μ
Consider only the transistor and diffusion capacitances and ign
parasitic and wiring (poly and metal) capacitances.

Part (b) (5 points)
If the inverter's V_{IH_L} is 2.8 volts, what is the high noise margin (NM_H) of this gate? (Hint: for the purposes of this problem, think about the dynamic NAND and inverter as separate gates).

Part (c) (10 points)
How could we redesign this circuit to increase its noise immunity? What affect would this have on its speed?

Problem 5 (20 points)
An N-bit priority encoder has N inputs, numbered 0 through N-1, and $\log_2 N$ outputs. The output of the priority encoder is the binary encoding of the the highest input that is asserted (i.e., a logic "1").

For example, consider a 4-bit priority encoder:



If I_1 and I_2 are asserted, then the output should be $O_1 = 1$ and $O_0 = 0$.

Small priority encoders can be implemented using two-levels of gate logic. However, larger ones are better implemented as a regular structure.

In this problem, you are to give the schematic of a 4-bit priority encoder. Your design should be a regular structure that can easily be extended to a general N-bit priority encoder. Your schematic should use only n-type and p-type transistors plus inverters (i.e., no multi-input gates). Your schematic should clearly indicate the regularity of the circuit and should (roughly) indicate the layout. You should indicate which routing layers you will use for each (major) signal type. Assume one polysilicon and two levels of metal are available.

Problem 5 (continued)