# CS/ECE 755: VLSI Systems Design

**Prof. David A. Wood**

**Midterm Exam**
**March 31, 1999**
**Approximate Weight: 20%**

**CLOSED BOOK**
**ONE SHEET OF NOTES**

**NAME: ________________________________**

**DO NOT OPEN THE EXAM UNTIL TOLD TO DO SO!**

Read over the entire exam before beginning. Verify that your exam includes all 10 pages. It is a long exam, so use your time carefully. Budget your time according to the weight of the questions, and your ability to answer them. Limit your answers to the space provided, if possible. If not, write on the BACK OF THE SAME SHEET. Use the back of the sheet for scratch work. WRITE YOUR NAME ON EACH SHEET.

| Problem | Possible Points | Points |
|---|---|---|
| **Problem 1** | 15 | |
| **Problem 2** | 10 | |
| **Problem 3** | 20 | |
| **Problem 4** | 20 | |
| **Problem 5** | 25 | |
| **Total** | **90** | |

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## Problem 1: (15 points)

### Part A: (5 points)

Describe the basic sequence of processing steps by which field oxide is grown and patterned in a semiconductor fabrication process.

### Part B: (10 points)

Describe the sequence of steps for construction of a pMOS device in an N-well process, starting with a bare wafer.

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**Problem 2: (10 points)**

Draw a *single* complementary CMOS gate that implements the following logic function:

$$F = A'BC + AB'C + ABC'$$

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## Problem 3: (20 points)

### Part A: (4 points)

What makes sign-digit arithmetic a potentially attractive approach for a VLSI multiplier?

### Part B: (4 points)

Why does carry-bypass perform faster than a Manchester carry chain?

### Part C: (4 points)

What is meant by “pitch matching”?

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**Part D: (4 points)**

Draw the transistor diagram of a 2-input complementary CMOS NAND gate. Size the transistors so that the rise and fall times are the same. Assume $\mu_n = 2\ \mu_p$

**Part E: (4 points)**

What is body effect and why do you need to worry about it?

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**Problem 4: (20 points)**

You are designing a chip that must be able to drive a signal in first-level metal (M1) from any point on the chip to any other. The chip is 20 mm on a side. Determine the worst-case RC delay of the longest wire (assume shortest rectilinear path).

Use the simplified distributed RC model: delay = $0.7\ rcl^2/2$ , where r is the resistance per unit length (μm), c is the capacitance per unit length (μm), and l is the length (μm).

You are given the following parameters:

Sheet resistance per square for M1: 0.07 Ω per square

Capacitance per square micron for M1: $50 * 10^{-18}$ F

Lambda (λ): 0.5 μm

Delay per inverting buffer: 200 ps

**Part A: (5 points)**

Calculate the parameters r and c for the simplified distributed RC model.

**Part B: (5 points)**

Calculate the worst-case delay of the maximum length wire without adding any buffers.

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**Part C: (10 points)**

Determine the optimal number of buffers to minimize the total delay and calculate the total delay of the optimized network.

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## Problem 5: (25 points)

In this problem you will design a 4-word by 4-bit register file based on a six-transistor static RAM cell. The register file should be precharged on $\phi 1$ and read during $\phi 2$. Label all transistors in your diagrams if you need to refer to them in the latter parts of the problem.

**Part A: (5 points)**

Draw a *transistor* diagram of a single six-transistor static RAM cell. Be sure to show the proper topology and layers of the word and bit lines as they flow through the cell.

**Part B: (5 points)**

Draw a *transistor-level* diagram of the *complete* address decoder. Use a Domino logic style. State any assumptions you need to make to avoid races in your Domino gates.

**Part C: (5 points)**

Draw the transistor-level schematics of the precharge and read-write circuits.

**Part D: (5 points)**

Describe the read operation of your register file. Do any transistors need to be sized for correct operation? For good performance? Label any transistors that need to be sized. Show your work.

**Part E: (5 points)**

Describe the *write* operation of your register file. Do any transistors need to be sized for correct operation? For good performance? Label any transistors that need to be sized.