VLSI Systems Design

CS/ECE 755 D. A. Wood
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Final Report Format

Your final report should have the following sections:

(1) Abstract

(2) System Overview

Describe the implementation goals for your chip design. Describe your design methodology and why this methodology was selected. Does your design satisfy the system requirements? What novel ideas or elegant solutions does the design include? Why did you choose to do it that way?

(3) Project Specification

Describe your chip's interface to the outside world, especially if if you changed the orginal specification in any way. Besides functionality, there are other aspects of interfacing to your chip. What assumptions about the supporting hardware environment are you making, e.g., clocking and signal levels? What are the detailed timing constraints on your chip, e.g., clock phase times and period? How is system reset on power up handled? Be detailed enough so a knowledgeable reader could understand how to use your chip in building a system.

(4) Project Scope

This section describes the difference between your ''grand plan'' and what you really were able to do. How much of what you wanted to implement has been realized by your chip? What portion was synthesized automatically and what portion was done by hand?

(5) Algorithm Description

Describe in detail the control sequencing of your design. Show a state diagram or similar method for describing control, such as documented Meg or C code. Give examples of its operation.

(6) Cell and Subsystem Designs

Describe your important cell designs. Include transistor diagrams and describe their area, and delay. You do not need to include layout plots, as we will examine these during your final demo. Show how these cells are composed to form subsystems and how subsystems are combined to form the high level floorplan.

(7) Control Design

Describe the implementation approach for your control: ROM-based, PLA, or standard cell. What is the area, and what is the critical delay path?

(8) Timing and Critical Paths

Describe overall system timing considerations for your chip. What clocking scheme did you use and why? What kinds of work gets done on each phase? What clock periods have you chosen for the phases, and how were they derived? Which paths are critical and why? Have you simulated their delays? What optimization techniques, if any, did you apply to try deceasing the critical path?

(9) Simulation Strategy

Describe your simulation strategy. Did you first simulate individual cells, and then larger composite cells? Did you simulate multiple copies of your design to see if they can communicate with each other? How did you generate the test cases? How confident are you that you covered all the cases?

(10) Test Strategy

Assume your chip will be fabricated. Describe how you would test the chips when you get them back?

(11) Chip Statistics

die size, number of transistors, layout density, pin count and distribution, maximum clock speed, etc.

(12) Tools Assessment

What was good and bad about the design tools you used? Please identify which tools worked well, and which didn't. What tools did you wish you had, but didn't? What tools did you use, but wish you hadn't? Please give specific suggestions on how the tools could have been used better, now that you have gone through the process. **This is a very important section! Next year we will use these tools again, and I hope to learn from your trials and tribulations.**

(13) Conclusion

What have you learned from you experience implementing the chip? What would you do differently on your next chip implementation?