CS/ECE 755: VLSI System Design

Prof. David A. Wood

HOMEWORK #2

Due Wednesday, February 24th, at end of class
Approximate Weight: 3%

Problem 1: (15 points)

Use color pens / pencils and show the sticks representations of the following gates. Use red for poly, green for n-type diffusion, brown or orange for p-type diffusion, and blue for metal-1. Use logical layers, not physical layers.

1. Complementary CMOS 2-2 AOI gate (F = (AB + CD)')
2. Domino CMOS carry logic for a full adder (Carry = A.B + A.C + B.C)
3. Pseudo-nMOS 8-input NOR gate

Problem 2: (10 points):

Using colored pens / pencils, draw the cross-section of the inverter (shown on the next page) where indicated with the horizontal dashed lines (note that there are four lines).

Problem 3: (75 points)

In this assignment you are to design the layout of a 19-bit carry-select adder. This assignment will focus on the standard cell implementation. In the next two assignments you will implement the same logic in full-custom and Schematic-Driven Layout (SDL).

Although these three design methodologies are not the only ones, they are representative of the modern major VLSI design practices. In this assignment we describe the design specification and give the detailed requirements for the standard cell implementation.

Design Specification

Design a 19-bit carry-select adder. The inputs are the vectors A(18:0) (where bit-0 is the LSB), B(18:0), and a carry-in bit C_i. The outputs are a vector S(18:0) and a carry-out bit C_o. Partition the carry-select adder in the following sequence of ripple-carry adders: 4-bits, 4-bits, 5-bits, and finally, 6 bits.

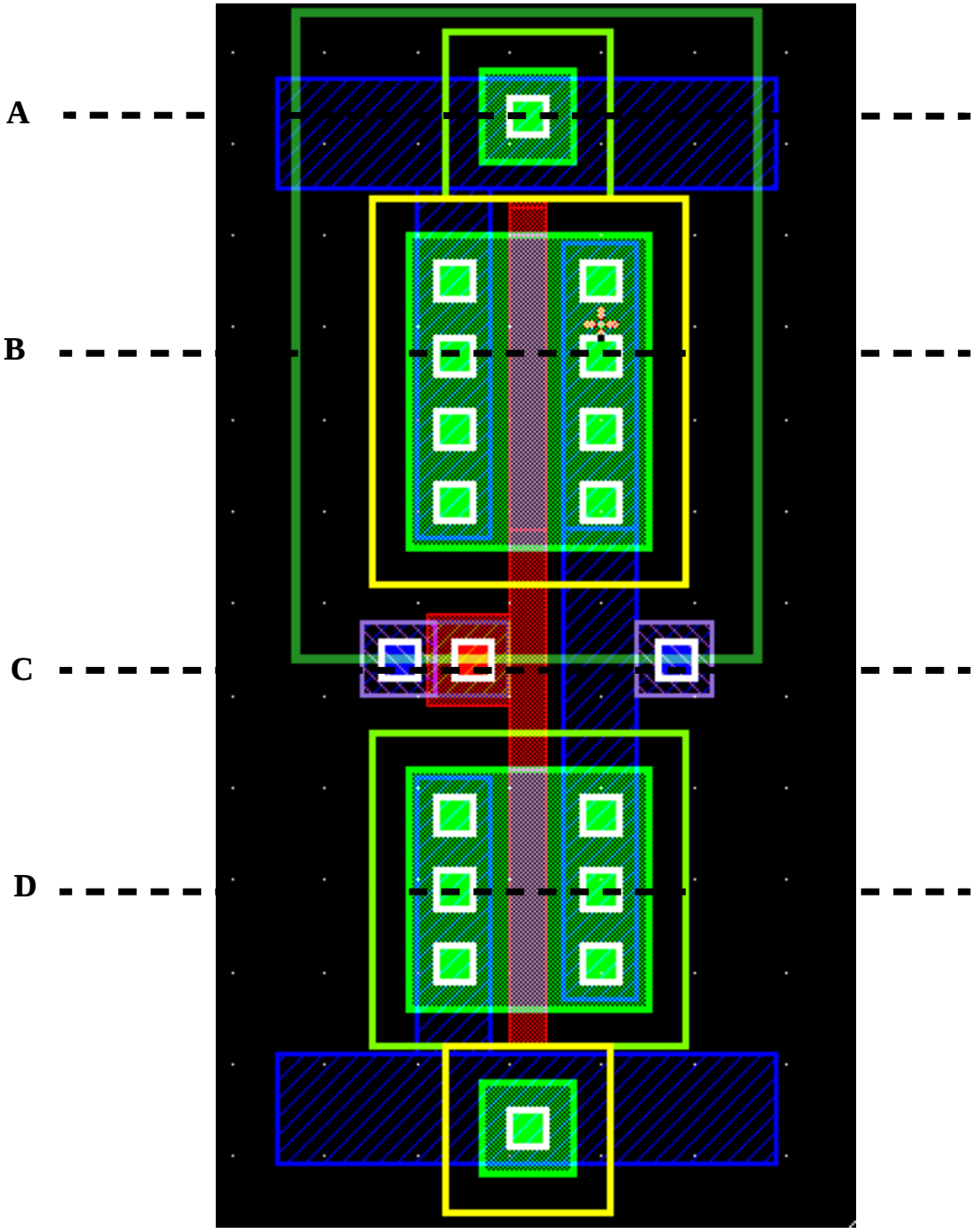
Note: If you are not familiar with carry-select adders, see section 8.2.1.6 of the textbook, or section A.8 from Hennessy & Patterson.

Do the logic design of the adder using Design Architect and the library scn08hp of logic components. Try to use as much as possible composite gates (AOIs, OAIs, etc), since the standard cells that implement these gates are faster than combinations of standard cells that implement more primitive gates. Report the number and type of cells that your design uses.

- Simulate your adder using QuickSim in the timing mode (as described in the second tutorial). These timing simulations should be done for the `nominal operation' of the logic components. After you make sure that the design is correct, identify the critical path and the input transitions that `excite' that path. Based on this analysis, measure the worst-case delay of your adder.
- Generate the layout of the design using the scn08hp library of standard cells (as described in the fourth tutorial). The `cell' (i.e., layout component) has to be a square (or close to a square). Also, the location of the ports should be as follows: the vector A ports are located at the top side of the cell, the vector B and signal C_i ports are located at the left side, while the vector S and signal C_o ports are located at the bottom side. Experiment with different floorplanning, placement, and routing options, until you get the most compact layout. Run DRC (Design-Rule Checking), and LVS (Layout-Versus-Schematic) checks, in order to make sure that the layout is correct and without any missing connections. Measure and report the total area of the layout.
- Run post-layout simulations with QuickSim, using a `backannotated' design viewpoint (as described in the fourth tutorial). What is the worst-case delay of your design in this case?

Deliverables

1. Printout of the logic design schematic.
2. Printout of QuickSim simulation traces (note: you do not have to include dozens of traces in your report; identify a few interesting cases (e.g., critical path excitation) and include annotated traces only for them). Include one set of traces for the pre-layout simulations, and one for the post-layout simulations, if these two are significantly different.
3. A short summary of your design methodology, measurements, and conclusions. For example, you can report the resulting cell area for each placement / routing option that you experimented with. Also, describe how you determined the critical path and the worst-case delay.
4. There will be a short (5 minutes or so) demo of the layout at the nova lab. The details for this demo will be announced later in this week through e-mail.



Inverter for problem 2.