

# Marc de Kruijf

## *Curriculum Vitae*

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Computer Sciences Department  
University of Wisconsin – Madison  
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## RESEARCH INTERESTS

- Architecture, compiler, and runtime support for unreliable and/or speculative hardware.
- Parallel programming models and runtime environments.
- Application characterization, analysis, and optimization.

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## EDUCATION

- Expected 2012 **Ph.D. Computer Science**, University of Wisconsin – Madison, WI  
Advisor: **Karthikeyan Sankaralingam**
- 2010 **M.S. Computer Science**, University of Wisconsin – Madison, WI
- 2004 **B.A. Computer Science**, *magna cum laude*, Macalester College, MN  
Study abroad: University of York, England

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## AWARDS AND HONORS

- 2011 Google U.S./Canada PhD Fellowship in Computer Architecture
- 2008 Honorable Mention, NSF Graduate Research Fellowship
- 2007 2<sup>nd</sup> place award, IBM Cell University Challenge '07 for Region 1 (Americas)
- 2007 Wisconsin Computer Science Departmental Summer Fellowship
- 2004 Phi Beta Kappa, National Honor Society

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## RESEARCH AND INDUSTRY EXPERIENCE

- Since 2007 **Research Assistant**, *Vertical Research Group*, University of Wisconsin – Madison
- Currently researching compiler-, and architecture-level techniques to allow efficient recovery from hardware faults and speculative execution. (See publications.)
  - Initial lead developer for the Pipelined Look-Up Grid (PLUG) compiler, built on top of the LLVM Compiler Infrastructure.
  - Initial lead architect for MapReduce on the Cell architecture. The initial prototype system won a 2<sup>nd</sup> place award at the IBM Cell University Challenge '07.

- Summer 2011 **Platforms Software Engineer Intern**, *Google Inc.*, Madison, WI
- Implemented mechanisms for transparent acceleration of network communication between processes running on the same host system.
- Summer 2009 **Platforms Software Engineer Intern**, *Google Inc.*, Madison, WI
- Developed ‘Page Tracker’, a tool for measuring the latency distribution of memory accesses in Google workloads using periodic and spatial page-access sampling inside the OS kernel.
- 2004 – 2006 **Product Developer**, *Objective Interface Systems Inc.*, Herndon, VA
- Performed product maintenance for *ORBexpress*, a high-performance implementation of the CORBA middleware standard targeted at embedded systems.
  - Project Manager for *ORBexpress* 2.6.5 product iteration.
  - Developed front-end web interface for in-house build-and-package automation system.
- Summer 2003 **IAESTE Research Trainee**, *Katedra Informatyki Stosowanej*, Łódź, Poland
- Developed tools for real-time visual analysis of process tomography data.

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## PUBLICATIONS

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### *Refereed Conference and Journal Publications*

**M. de Kruijf**, K. Sankaralingam, S. Jha. **Static Analysis and Compiler Design for Idempotent Processing**. *To appear in PLDI '12: Programming Language Design and Implementation*, June 2012.

**M. de Kruijf**, K. Sankaralingam. **Idempotent Processor Architecture**. *MICRO '11: International Symposium on Microarchitecture*, December 2011.

S. Nomura, M. Sinclair, C. Ho, V. Govindaraju, **M. de Kruijf**, K. Sankaralingam. **Sampling + DMR: Practical and Low-overhead Permanent Fault Detection**. *ISCA '11: International Symposium on Computer Architecture*, June 2011.

A. Kumar, L. De Carli, S. J. Kim, **M. de Kruijf**, K. Sankaralingam, C. Estan, and S. Jha. **Design and Implementation of the PLUG Architecture for Programmable and Efficient Network Lookups**. *PACT '10: International Conference on Parallel Architectures and Compilation Techniques*, September 2010.

**M. de Kruijf**, S. Nomura, and K. Sankaralingam. **Relax: An Architectural Framework for Software Recovery of Hardware Faults**. *ISCA '10: International Symposium on Computer Architecture*, June 2010.

**M. de Kruijf**, S. Nomura, and K. Sankaralingam. **A Unified Model for Timing Speculation: Evaluating the Impact of Technology Scaling, CMOS Design Style, and Fault Recovery Mechanism**. *DSN '10: International Conference on Dependable Systems and Networks*, June 2010.

**M. de Kruijf** and K. Sankaralingam. **MapReduce for the CELL B.E. Architecture**. *IBM Journal of Research and Development* 53:5, 2009.

## Workshop Publications and Technical Reports

**M. de Kruijf** and K. Sankaralingam. **Compiler Construction of Idempotent Regions.** *University of Wisconsin Computer Sciences Technical Report CS-TR-2007-1700*, October 2011.

**M. de Kruijf**, S. Nomura, and K. Sankaralingam. **The Design, Modeling, and Evaluation of the Relax Architectural Framework.** *University of Wisconsin Computer Sciences Technical Report CS-TR-2007-1672*, April 2010.

**M. de Kruijf** and K. Sankaralingam. **Exploring the Synergy of Emerging Workloads and Silicon Reliability Trends.** *SELSE 5: IEEE Workshop on Silicon Errors in Logic – System Effects*, March 2009.

**M. de Kruijf** and K. Sankaralingam. **MapReduce for the Cell B.E. Architecture.** *University of Wisconsin Computer Sciences Technical Report CS-TR-2007-1625*, October 2007.

## INVITED PRESENTATIONS

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### *Idempotent Processor Architecture*

- Jun. 2012 PLDI '12: Programming Language Design and Implementation – Beijing, China
- Dec. 2011 MICRO '11: International Symposium on Microarchitecture – Porto Alegre, Brazil
- Oct. 2011 Wisconsin Computer Architecture Industrial Affiliates Meeting – Madison, WI
- Apr. 2011 Google Tech Talk – Madison, WI

### *Relax: An Architectural Framework for Software Recovery of Hardware Faults*

- Oct. 2010 Wisconsin Computer Architecture Industrial Affiliates Meeting – Madison, WI
- Jun. 2010 ISCA '10: International Symposium on Computer Architecture – St. Malo, France

### *A Unified Model for Timing Speculation: Evaluating the Impact of Technology Scaling, CMOS Design Style, and Fault Recovery Mechanism*

- Jun. 2010 DSN '10: International Conference on Dependable Systems and Networks – Chicago, IL

### *Synergy of Emerging Workloads and Silicon Reliability Trends*

- Mar. 2009 SELSE 5: Silicon Errors in Logic – System Effects (poster) – Palo Alto, CA.
- Oct. 2008 Wisconsin Computer Architecture Industrial Affiliates Meeting – Madison, WI

### *MapReduce for the Cell B. E. Architecture*

- Oct. 2007 Computer Science Departmental Summer Research Colloquium – Madison, WI
- Oct. 2007 Wisconsin Computer Architecture Industrial Affiliates Meeting – Madison, WI
- Sep. 2007 2007 Power Architecture Developer Conference – Austin, TX

## TEACHING AND OTHER PROFESSIONAL DEVELOPMENT

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### *Wisconsin School of Business, University of Wisconsin – Madison, WI*

- Fall 2009 Emerging Entrepreneurship
- Spring 2009 Technology Entrepreneurship

*Delta Program, University of Wisconsin – Madison, WI*

Fall 2008 Diversity in the College Classroom  
Summer 2008 The College Classroom: Liberal Arts, UW System, and Technical College Classrooms

*Computer Sciences Department, University of Wisconsin – Madison, WI*

Fall 2007 Teaching Assistant for Advanced Computer Architecture I (CS 752)  
Spring 2007 Teaching Assistant for Introduction to Computer Engineering (CS 252)  
Fall 2006 Teaching Assistant for Discrete Mathematics (CS 240)

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## PROFESSIONAL ACTIVITIES AND SERVICE

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External Reviewer for ISPASS ('08), MICRO ('08, '09), Concurrency and Computation: Practice and Experience ('10), and Journal of Parallel and Distributed Computing ('10).

ACM (SIGARCH) and IEEE student member

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## TECHNICAL PROFICIENCIES

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**Python** for scripting and general-purpose programming  
**C++/C** for high-performance and/or low-level programming  
**LLVM** for compiler development; **M5** for processor simulation  
**jQuery** and **Google App Engine** for web development

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## PERSONAL INFORMATION

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Citizenship: The Netherlands  
Immigration status: U.S. Permanent Resident