Department of Electrical & Systems Engineering

ESE 570 Midterm Exam - March 22, 2003

Solutions

To maximize opportunity for partial credit, please show all work and all units. Please note that there are a total of five problems. For full credit, solve any four of the five problems. Each problem is worth 25 points.

1. An enhancement nMOS transistor has SPICE parameters in Table 4 on page 6 of the FORMULAS AND DATA handout.

(a) When the transistor is biased with V_G = 2.8V, V_D = 5V, V_S = 1V and V_B = 0V, all with respect to ground, the drain current I_D is measured to be 0.425 mA. Calculate the W/L for this transistor. (10 pts)

(b) Using the W/L ratio found in (a), calculate the drain current I_D for the bias conditions V_G = 5V, V_D = 4V, V_S = 2V and V_B = 0V. (10 pts)

(c) Using the W/L ratio in (a) and C_{gb} = 32 fF when the transistor is in cut-off mode, calculate the values for W and L. Assume that the overlap capacitances are negligible. (5 pts)

SOLUTION

The relevant SPICE parameters for the nMOS transistor from Table 4 of the FORMULAS AND DATA handout are as follows: VT0 = 0.5 V, KP = 8.5 E-5 A/V^2, PHI = 0.74 V, GAMMA = 0.48 $\sqrt{V}$, LAMBDA = 0.01 V^{-1}, U0 = 500 cm^2/Vs

(a) V_G = 2.8V, V_D = 5V, V_S = 1V and V_B = 0V => V_{GS} = 2.8V - 1V = 1.8 V; V_{DS} = 5V - 1V = 4V; V_{SB} = 1V - 0V = 1V

Since $V_{SB} \neq 0$; $V_T \neq$ VT0:

$$V_T = \text{VT0} + \text{GAMMA}\left(\sqrt{|-\text{PHI} + V_{SB}|} - \sqrt{|-\text{PHI}|}\right)$$

$$= 0.5\text{V} + 0.48\sqrt{\text{V}}\left(\sqrt{|-(-0.74\text{V}) + 1\text{V}|} - \sqrt{0.74\text{V}}\right) = 0.5\text{V} + 0.48(0.459)\text{V} = 0.720\text{V}$$

Since V_{GS} = 1.8 V > V_T and V_{DS} = 4V > V_{GS} - V_T => the nMOS is in Saturation Region

$$I_D(\text{sat}) = \frac{\text{KP}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \text{LAMBDA} \quad V_{DS}) \Rightarrow \frac{W}{L} = \frac{2I_D(\text{sat})}{\text{KP}(V_{GS} - V_T)^2(1 + \text{LAMBDA} \quad V_{DS})}$$

$$\frac{W}{L} = \frac{2\left(0.425 \times 10^{-3}\text{A}\right)}{8.5 \times 10^{-5}\text{A}/\text{V}^2(1.8 - 0.72)^2\text{V}^2\left(1 + 0.01\text{V}^{-1}4\text{V}\right)} = \frac{0.85 \times 10^{-3}\text{A}}{8.5 \times 10^{-5}\text{A}(1.17)(1.04)} = 8.22$$

(b) V_G = 5V, V_D = 4V, V_S = 2V and V_B = 0V => V_{GS} = 5V - 2V = 3V; V_{DS} = 4V - 2V = 2V; V_{SB} = 2V - 0V = 0V

Since $V_{SB} \neq 0$; $V_T \neq VT0$:

$$V_T = VT0 + GAMMA\left(\sqrt{|-PHI + V_{SB}|} - \sqrt{|-PHI|}\right)$$

$$= 0.5V + 0.48\sqrt{V}\left(\sqrt{|-(-0.74V) + 2V|} - \sqrt{0.74V}\right) = 0.5V + 0.48(0.795)V = 0.882V$$

Since $V_{GS} = 3\ V > V_T$ and $V_{DS} = 2V < V_{GS} - V_T = 2.118V$ => the nMOS is in Linear Region

$$I_D(lin) = \frac{KP}{2}\frac{W}{L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right](1 + LAMBDA \quad V_{DS})$$

$$= \frac{8.5 \times 10^{-5} V/A^2}{2}(8.22)\left[2(2.188)2V^2 - 4V^2\right]\left(1 + 0.01V^{-1} \quad 4V\right)$$

$$= \frac{8.5 \times 10^{-5} V/A^2}{2}(8.22)(4.47)V^2(1.04) = 1.62\ mA$$

(c) $C_{gb} = C_{ox}WL$ where $C_{ox} = \frac{\varepsilon_{SiO2}}{TOX} = \frac{KP}{U0} = 1.7 \times 10^{-7} F/cm^2$

$$=> WL = \frac{C_{gb}}{C_{ox}} = \frac{32 \times 10^{-15} F}{1.7 \times 10^{-7} F/cm^2} = 18.8 \times 10^{-8} cm^2 = 18.8 \mu m^2$$

Using $\frac{W}{L} = 8.22$ => $W = 8.22L$ => $8.22L^2 = 18.8 \mu m^2$ => $L = \sqrt{\frac{18.8}{8.22}}\mu m = 1.51 \mu m$

$W = 8.22L$ => $W = 8.22 \times 1.512 \mu m = 12.43 \mu m$

2. Consider the four-input NAND circuit in Fig. P2.

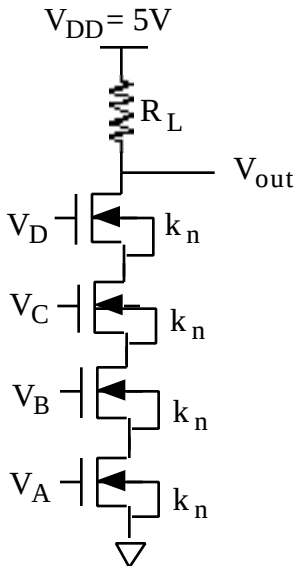


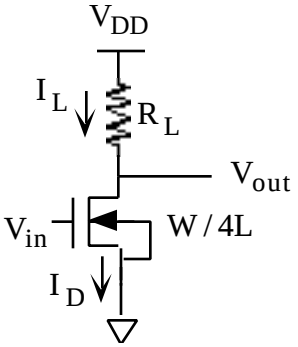
Figure P2

(a) With $V_A = V_B = V_C = V_D = V_{DD}$, derive expressions for V_{OH}, V_{OL} and V_{IL} in terms of V_{DD}, V_{T0n}, k_n and R_L (Assume that GAMMA = 0.0 $V^{1/2}$ and LAMBDA = 0.0 V^{-1} for all the transistors) (18 pts)

(b) Let GAMMA = 0.0 $V^{1/2}$ and LAMBDA = 0.0 V^{-1}, otherwise let the transistors have the SPICE parameters in Table 4 on page 6 of the FORMULAS AND DATA handout. Determine the value of $(W/L)R_L$ that realizes a $V_{OL} = 0.2V$. (7 pts)

SOLUTION

Using the equivalent inverter, where $k_{nEQV} = \frac{1}{4}k_n$, i.e.



where $V_{in} = V_A = V_B = V_C = V_D$

(a)

V_{OH}: Vin = 0V => nMOS cutt off; hence, $I_L = \frac{1}{R_L}(V_{DD} - V_{OH}) = I_D = 0$ $V_{OH} = V_{DD}$

V_{OL}: Vin = $V_{GS} = V_{DD}$ => $V_{out} = V_{OL} = V_{DS} < V_{GS}$ - VT0 => nMOS is in Linear Region

$I_L = I_D$ =>

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_{nEQV}}{2}\left[2\left(V_{DD} - V_{T0n}\right)V_{OL} - V_{OL}^2\right] \quad \text{where } V_{in} = V_{OH} = V_{DD} \text{ and } V_{out} = V_{OL}$$

i.e.

$$V_{OL}^2 - 2\left(V_{DD} - V_{T0n} + \frac{1}{k_{nEQV}R_L}\right)V_{OL} + \frac{2}{k_{nEQV}R_L}V_{DD} = 0$$

Solving for V_{OL}:

$$V_{OL} = V_{DD} - V_{T0n} + \frac{1}{k_{nEQV}R_L} \pm \sqrt{\left(V_{DD} - V_{T0n} + \frac{1}{k_{nEQV}R_L}\right)^2 - \frac{2}{k_{nEQV}R_L}V_{DD}}$$

Substituting $k_{nEQV} = \frac{1}{4}k_n$

$$V_{OL} = V_{DD} - V_{T0n} + \frac{4}{k_nR_L} \pm \sqrt{\left(V_{DD} - V_{T0n} + \frac{4}{k_nR_L}\right)^2 - \frac{8}{k_nR_L}V_{DD}}$$

V_{IL}: nMOS is ON and saturated

$I_L = I_D$ => $\frac{V_{DD} - V_{out}}{R_L} = \frac{k_{nEQV}}{2}\left(V_{in} - V_{T0n}\right)^2$

Differentiating wrt to V_{in} yields: $-\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = k_{nEQV}\left(V_{in} - V_{T0n}\right)$

Setting $dV_{out}/dV_{in} = -1$ and $V_{in} = V_{IL}$ yields: $V_{IL} = V_{T0n} + \frac{1}{k_{nEQV}R_L}$

Substituting $k_{nEQV} = \frac{1}{4}k_n$

$$V_{IL} = V_{T0n} + \frac{4}{k_nR_L}$$

(b) V_{OL} = 0.2V; The relevent SPICE parameters from Table 6 of the FORMULAS AND DATA handout are VT0 = 0.5 V, KP = 8.5 E-5 A/V^2, U0 = 500 cm^2/Vs

Solve $V_{OL}^2 - 2\left(V_{DD} - V_{T0n} + \frac{4}{k_nR_L}\right)V_{OL} + \frac{8}{k_nR_L}V_{DD} = 0$ for k_nR_L, i.e.

$$\frac{8}{k_nR_L}\left(V_{DD} - V_{OL}\right) = 2\left(V_{DD} - V_{T0n}\right)V_{OL} - V_{OL}^2 \Rightarrow \frac{8}{k_nR_L} = \frac{2\left(V_{DD} - V_{T0n}\right)V_{OL} - V_{OL}^2}{\left(V_{DD} - V_{OL}\right)}$$

$$k_n R_L = \frac{8(V_{DD} - V_{OL})}{2(V_{DD} - V_{T0n})V_{OL} - V_{OL}^2} = \frac{8(5 - 0.2)\,V}{2(5 - 0.5)0.2 - (0.2)^2\,V^2} = \frac{38.4}{1.76}\,V^{-1} = 21.82V^{-1}$$

$$KP\frac{W}{L}R_L = 21.82V^{-1} \qquad \frac{W}{L}R_L = \frac{21.82V^{-1}}{8.5 \times 10^{-5} A / V^2} = 256.7k\Omega$$

3. The unloaded inverter in Fig. P3a is fabricated in a 0.35 μm n-well CMOS process. The design rules for this process are obtained from the lambda design rules given on pages 6 and 7 of the FORMULAS AND DATA handout by setting λ to the value that establishes the minimum gate length at 0.35 μm. Templates for the layouts for the two transistors are shown in Fig. P3b without dimensions and labels for the mask levels.

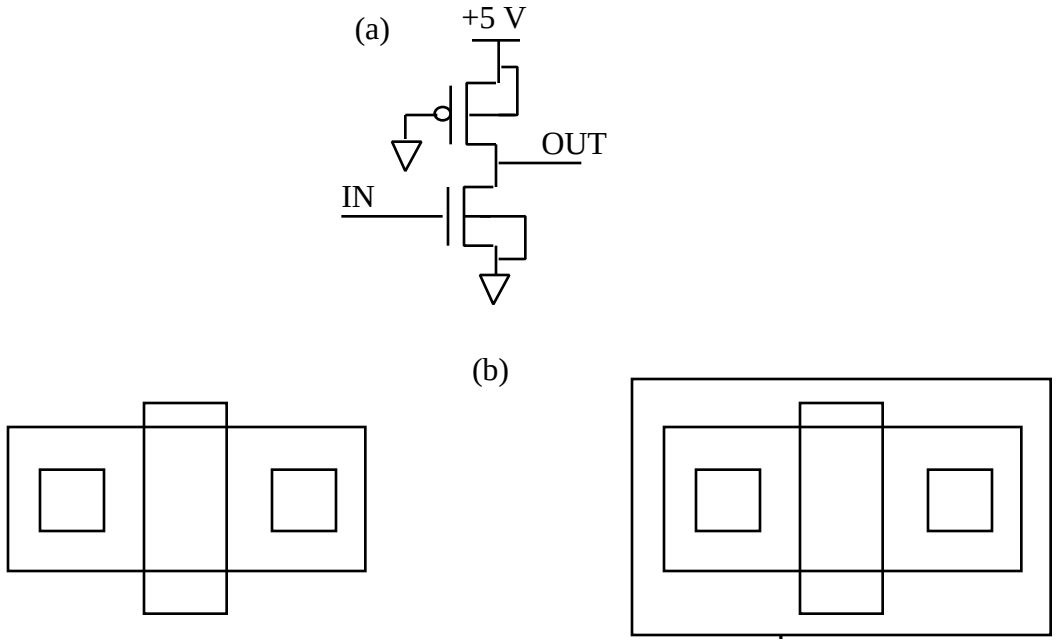


Figure P3

(a) To minimize die area, the inverter is to be designed with minimum sized transistors. Using the templates in Fig. 3b and the design the design rules for the 0.35 μm n-well CMOS process, develop the layouts for minimum size PMOS and NMOS transistors that enable their sources and drains to be properly contacted to metal1. Label the appropriate mask levels and provide all the mask dimensions. (9 pts)

(b) In order to take advantage of a new 0.18 μm n-well CMOS process with minimal design effort, a new mask set is being developed that scales the gate lengths for all transistors. What is the quantitative impact of this scaling on device currents, parasitic capacitances, power dissipation and propagation delay. (8 pts)

(c) The SPICE simulation for the pseudo NMOS gate yielded the following transfer characteristic data:

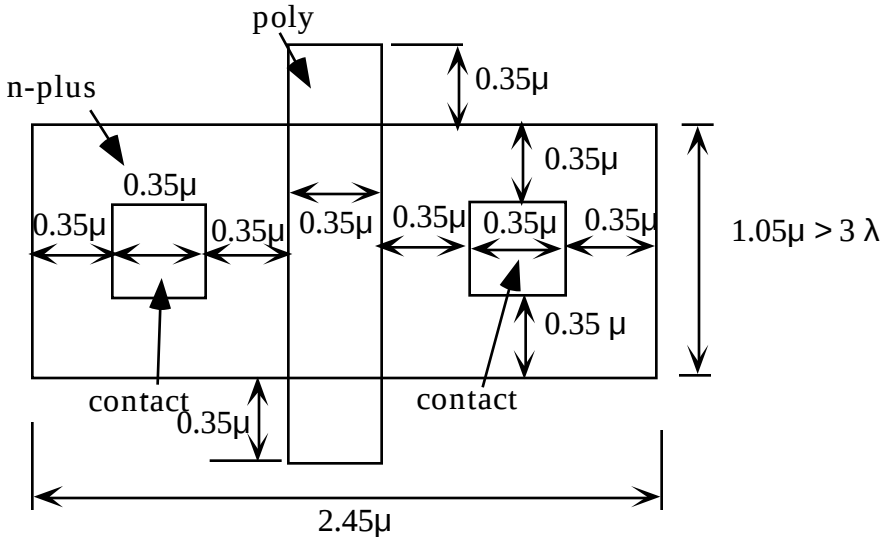
V_{in} (V)	0.00	1.00	1.10	1.20	1.40	1.60	1.80	2.00	2.20	2.30	4.00	5.00
V_{out} (V)	5.00	5.00	4.95	4.85	4.02	3.23	2.37	1.61	0.72	0.62	0.52	0.50

From the data determine V_{OL}, V_{OH} and estimate V_{IL}, V_{IH}, and the low and high noise margins. (8 pts)

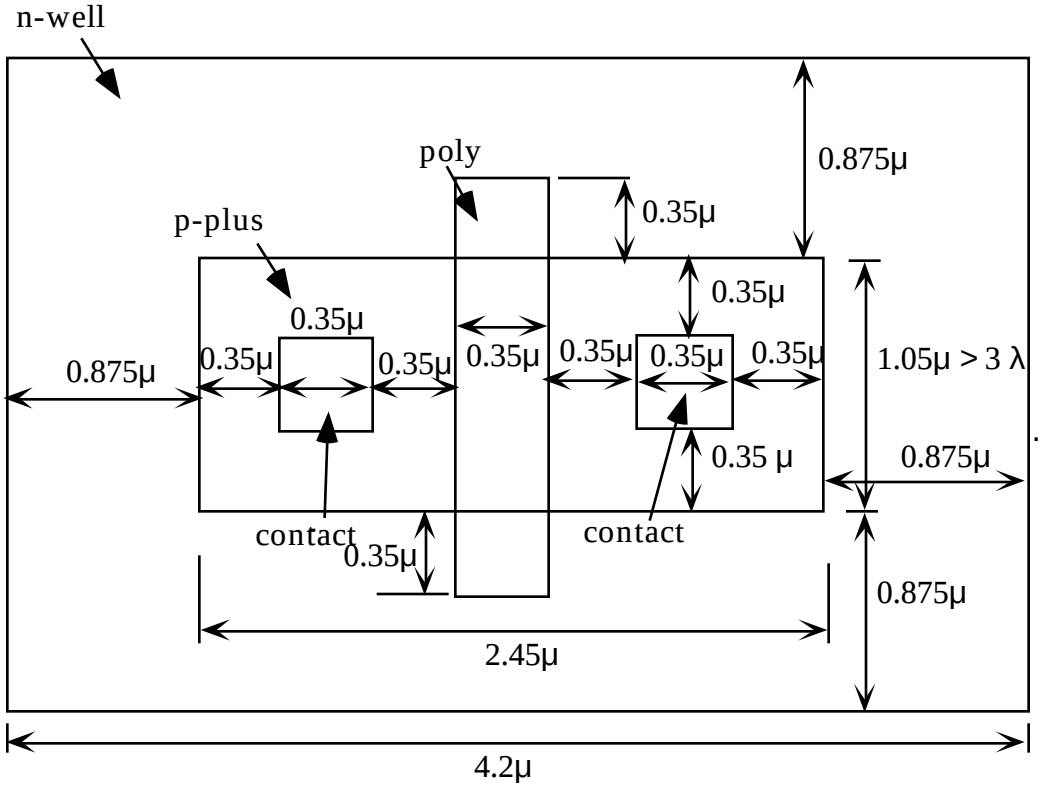
SOLUTION

For 0.35 μm minimum gate $\lambda = \frac{0.35\mu m}{2} = 0.175\mu m$

nMOS Transistor:



pMOS Transistor:



(b) Lateral scaling L is scaled by 1/α; hence, the scaling for the other parameters are unity for W, V, TOX, Xj and NA

The resulting scaling for parasitic capacitances, power dissipation and propagation delay are as follows:

$$\text{current}(I) \rightarrow \left(\frac{W}{L}\right)\frac{1}{TOX}V^2 \qquad \text{scaling} = \alpha$$

$$\text{powerdissipation}(P) \rightarrow IV \qquad \text{scaling} = \alpha$$

$$\text{parasitic capacitance}(C) \rightarrow WL\frac{1}{TOX} \qquad \text{scaling} = \frac{1}{\alpha}$$

$$\text{gatedelay}(T) \rightarrow \frac{VC}{I} \qquad \text{scaling} = \frac{1}{\alpha^2}$$

(c)

V_{in} (V) |	0.00	1.00	1.10	1.20	1.40	1.60	1.80	2.00	2.20	2.30	4.00	5.00
V_{out} (V) |	5.00	5.00	4.95	4.85	4.02	3.23	2.37	1.61	0.72	0.62	0.52	0.50
	^			^						^		^
	V_{OH}			V_{IL}						V_{IH}		V_{OH}

By inspection V_{OH} = 5 V and V_{OL} = 0.5 V. From the data $\Delta V_{out}/\Delta V_{in}$ = -1 at V_{IL} = 1.15 V and V_{IH} = 2.25 V. The noise margins are

$$NM_H = |V_{IL} - V_{OL}| = |1.15 - 0.50| = 0.65 \text{ V}$$

and $$NM_L = |V_{OH} - V_{IH}| = |5.00 - 2.25| = 2.75 \text{ V}$$

4. Let the behavior description for a CMOS (with pull-down net and complementary pull-up net) gate be the Boolean expression $Z = \overline{(A + B + C) \cdot (D + E) \cdot F}$.

(a) Draw the transistor level schematic for a CMOS implementation of this Boolean expression, where the CMOS structure is shown in Fig. P4. (7 pts)

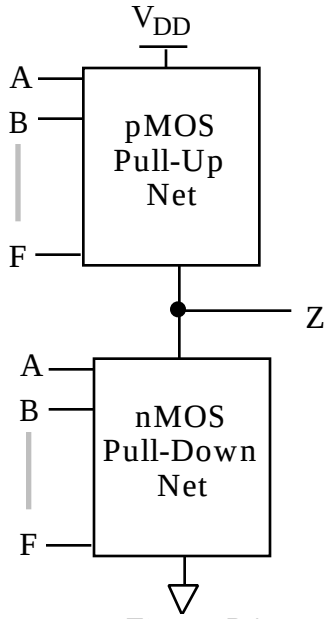


Figure P4

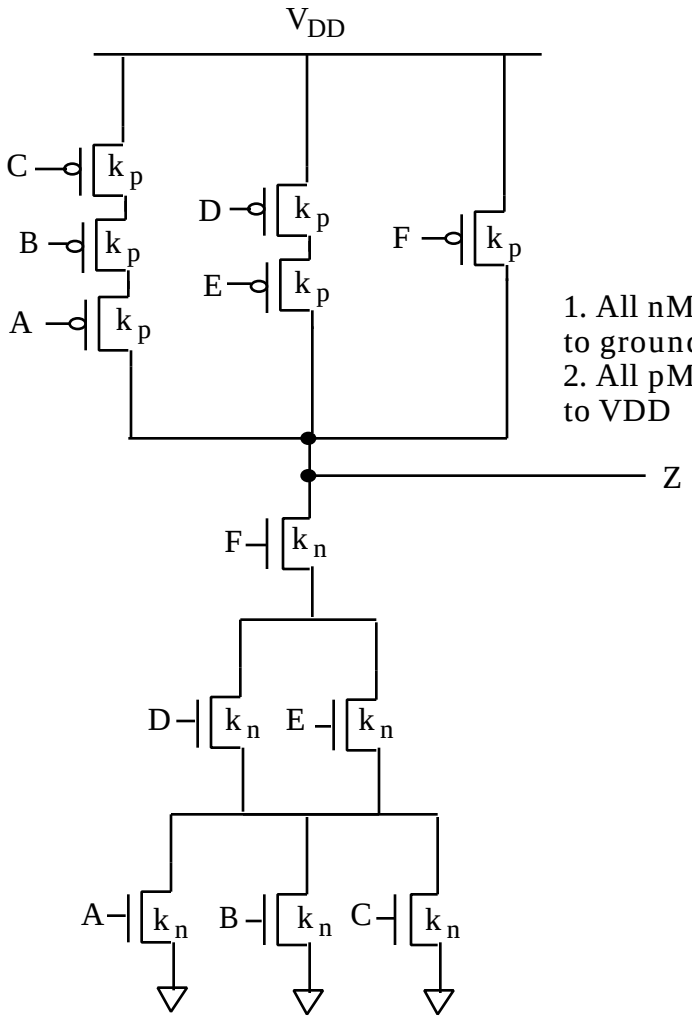
(b) Determine the equivalent inverter $k_{n,equiv}$ and $k_{p,equiv}$ for the case when all inputs A = B = C = D = E = F = 1 (or V_{DD}). Assume that all the nMOS transistors have identical transconductance parameters k_n and all the pMOS transistors have identical transconductance parameters are k_p. (8 pts)

(c) Derive the expression for the gate threshold voltage V_{th}. For $V_{T0n} = |V_{T0p}|$, determine the relationship between k_n and k_p to realize $V_{th} = V_{DD}/2$. (10 pts)

For (b) and (c) assume that the back gate and channel modulation effects for all transistors are zero.

SOLUTION

(a)



1. All nMOS back gates connected to ground
2. All pMOS back gates connected to VDD

(b)

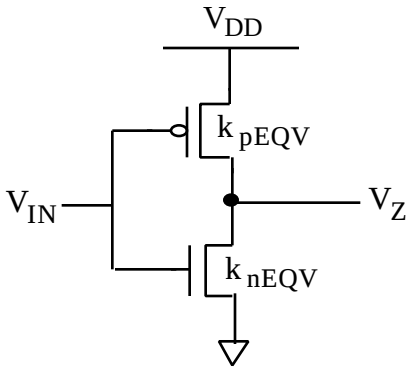
$$k_{nEQV} = \frac{1}{\frac{1}{3k_n} + \frac{1}{2k_n} + \frac{1}{k_n}} = \frac{1}{\frac{2}{6k_n} + \frac{3}{6k_n} + \frac{6}{6k_n}} = \frac{6}{11}k_n$$

All the pMOS tranistors are OFF.

I also excpet as correct solutions the complete eqivalent inverter with k_{nEQV} and k_{pEQV}, where

$$k_{pEQV} = \frac{1}{\frac{1}{k_p} + \frac{1}{k_p} + \frac{1}{k_p}} + \frac{1}{\frac{1}{k_p} + \frac{1}{k_p}} + k_p = \frac{1}{3}k_p + \frac{1}{2}k_p + k_p = \frac{11}{6}k_p$$

(c) Use the equivalent inverter, where $V_A = V_B = V_C = V_D = V_E = V_F = V_{IN} = V_Z = V_{th}$



where

$$k_{nEQV} = \frac{1}{\frac{1}{3k_n} + \frac{1}{2k_n} + \frac{1}{k_n}} = \frac{1}{\frac{2}{6k_n} + \frac{3}{6k_n} + \frac{6}{6k_n}} = \frac{6}{11}k_n$$

$$k_{pEQV} = \frac{1}{\frac{1}{k_p} + \frac{1}{k_p} + \frac{1}{k_p}} + \frac{1}{\frac{1}{k_p} + \frac{1}{k_p}} + k_p = \frac{1}{3}k_p + \frac{1}{2}k_p + k_p = \frac{11}{6}k_p$$

For V_{th}: $V_{IN} = V_Z = V_{th}$ and both nMOS and pMOS are in Saturation; hence,

$$\frac{k_n}{2}\left(V_{IN} - V_{T0n}\right)^2 = \frac{k_p}{2}\left(V_{IN} - V_{DD} - V_{T0p}\right)^2$$

Solving for V_{th}:

$$V_{th} = \frac{V_{T0n} + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \sqrt{\frac{k_{pEQV}}{k_{nEQV}}}\right)} = \frac{V_{T0n} + \frac{11}{6}\sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{T0p}\right)}{\left(1 + \frac{11}{6}\sqrt{\frac{k_p}{k_n}}\right)}$$

For $V_{T0n} = |V_{T0p}|$ and $V_{th} = V_{DD}/2$.

$$\frac{V_{T0n} + \frac{11}{6}\sqrt{\frac{k_p}{k_n}}\left(V_{DD} - V_{T0n}\right)}{\left(1 + \frac{11}{6}\sqrt{\frac{k_p}{k_n}}\right)} = \frac{V_{DD}}{2} \Rightarrow \frac{11}{6}\sqrt{\frac{k_p}{k_n}} = 1 \Rightarrow \frac{k_p}{k_n} = \left(\frac{11}{6}\right)^2$$

5. Consider the CMOS gate in Fig. P5, where A through H are logic inputs, Φ is a clock with period 4τ, X is an intermediate output node, Z is the gate's logic output and C is a parasitic capacitance.

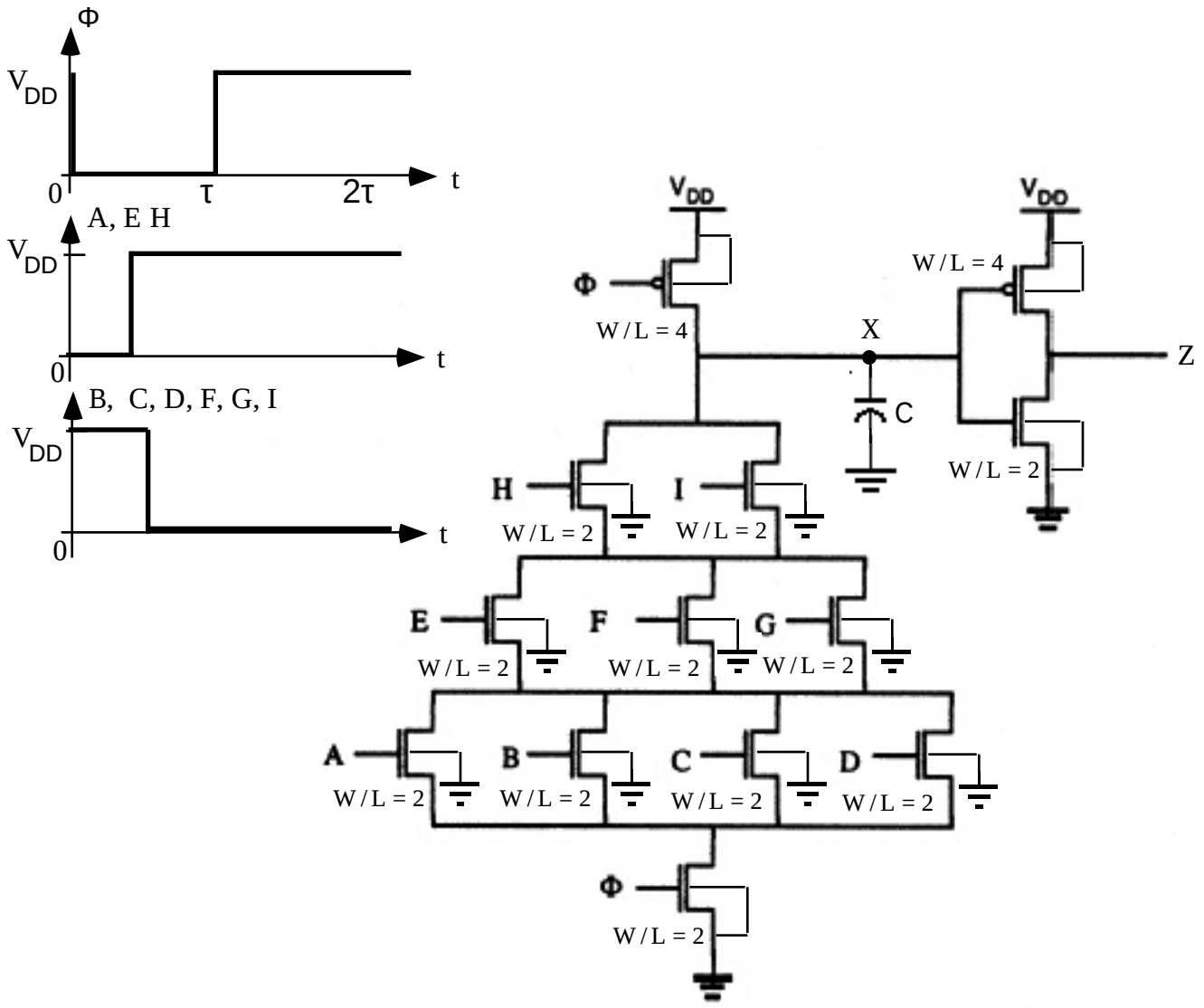


Figure P5

(a) Describe in detail the functional behavior of this circuit for outputs X and Z when Φ = 0 (or 0 V) and when Φ = 1 (or V_{DD}) for $0 \le t \le 2\tau$. Use Boolean expressions and timing diagrams where appropriate. What role does capacitor C play in this gate's operation? (15 pts)

(b) Let Φ = 1 and the inputs A, B, C, D, E, F, G, H, I be as shown in Fig. P5. The nMOS network in the circuit that drives node X can be approximated by a single transistor with an equivalent W/L. Determine this equivalent W/L for the input conditions given in Fig. P5. Assume that the back gate and channel modulation effects for all transistors are zero. (10 pts)

SOLUTION:

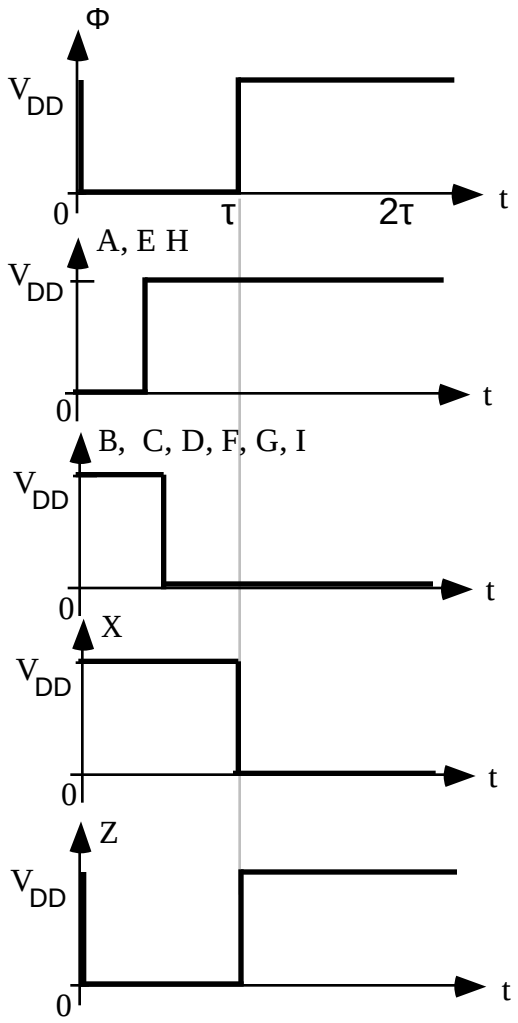
(a)
When $\Phi = 0$ for $t < \tau$, the nMOS and pMOS driven by Φ are OFF and ON, respectively. Hence, X is pulled high to $X = V_{DD}$ and $Z = 0$. During this phase of the clock, capacitance C is charged (or pre-charged) to V_{DD}.

When $\Phi = V_{DD}$ for $\tau \le t < 4\tau$, the nMOS and pMOS driven by Φ are ON and OF, respectively. During this phase, X is selectively pulled low depending on the logic levels of inputs A through I.

$$X = \overline{(A + B + C + D) \cdot (E + F + G) \cdot (H + I)}$$
$$Z = \overline{X} = (A + B + C + D) \cdot (E + F + G) \cdot (H + I)$$

In this particular case prior to $t = \tau$, inputs $A = E = H$ are set to V_{DD} and the remaining inputs are set to 0. Hence when $\Phi = V_{DD}$ for $t = \tau$, X is pulled down to zero by discharging C through the A, E and H. Hence, Z switches V_{DD}. The timing diagrams for X and Z are shown below, along with Φ and the inputs.

The role played by C is to hold the pre-charge to V_{DD} for time $\Phi = 0$ and the value of $X = \overline{Z}$ for the time $\Phi = V_{DD}$. Hence, Z is always at a well defined logic level.



(b)
When $\Phi = V_{DD}$, and the inputs A = E = H = V_{DD} and B = C = D = F = G = I = 0, the X is pulled down by the series tandem of four nMOS transistors A, E, H and Φ.

Hence, these four series connected transistors, ignoring the back gate and channel modulation effects, can be approximated by a single transistor with k_{nEQV}. Since four transistors are in series:

$$k_{nEQV} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{nEQV} = \frac{k_n}{4} = \frac{\mu_n C_{ox}}{4} \left(\frac{W}{L}\right)_n \qquad \left(\frac{W}{L}\right)_{nEQV} = \frac{1}{4}\left(\frac{W}{L}\right)_n = 1/2$$

Equivalent circuit for Φ = 1