CS 354: Lecture 28 - Notes

1. Suppose we have a system with the following properties:
    a. The memory is byte addressable.
    b. Memory accesses are to **1-byte words** (not to 4-byte words).
    c. Addresses are **12 bits** wide.
    d. The cache is **two-way set associative** (E = 2), with a **4-byte block size** (B = 4) and **four sets** (S = 4).

    The contents of the cache are as follows, with all numbers given in hexadecimal notation.

Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	00	1	40	41	42	43
0	83	1	FE	97	CC	D0
1	00	1	44	45	46	47
1	83	0	-	-	-	-
2	00	1	48	49	4A	4B
2	40	0	-	-	-	-
3	FF	1	9A	C0	03	FF
3	00	0	-	-	-	-

    A. The following figure shows the format of an address (one bit per box). Indicate (by labeling the diagram) the fields that would be used to determine the following:

    CO - The cache block offset
    CI - The cache set index
    CT - The cache tag

11	10	9	8	7	6	5	4	3	2	1	0
CT	CT	CT	CT	CT	CT	CT	CT	CI	CI	CO	CO

Suppose a program running on the machine references the 1-byte word at address **0x831**. Indicate the cache entry accessed and the cache byte value returned in hex. Indicate whether a cache miss occurs. If there is a cache miss, enter "–" for "Cache byte returned."

B. Address Format

11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	1	1	0	0	0	1

C. Memory Reference

Parameter	**Value**
Cache block offset (CO)	0x1
Cache set index (CI)	0x0
Cache tag (CT)	0x83
Cache hit? (Y / N)	Y
Cache byte returned	0x97

D. For each of the following memory accesses indicate if it will be a cache hit or miss when **carried out in sequence** as listed. Also give the value of a read if it can be inferred from the information in the cache.

Operation	**Address**	**Hit / Miss**	**Read Value (or unknown)**
Read	0x834	Miss	Unknown
Write	0x836	Hit	
Read	0xFFD	Hit	0xC0

E. What are the different addresses that have their tag bits as 0xFF and that would map to set 3?

0xFFC to OxFFF