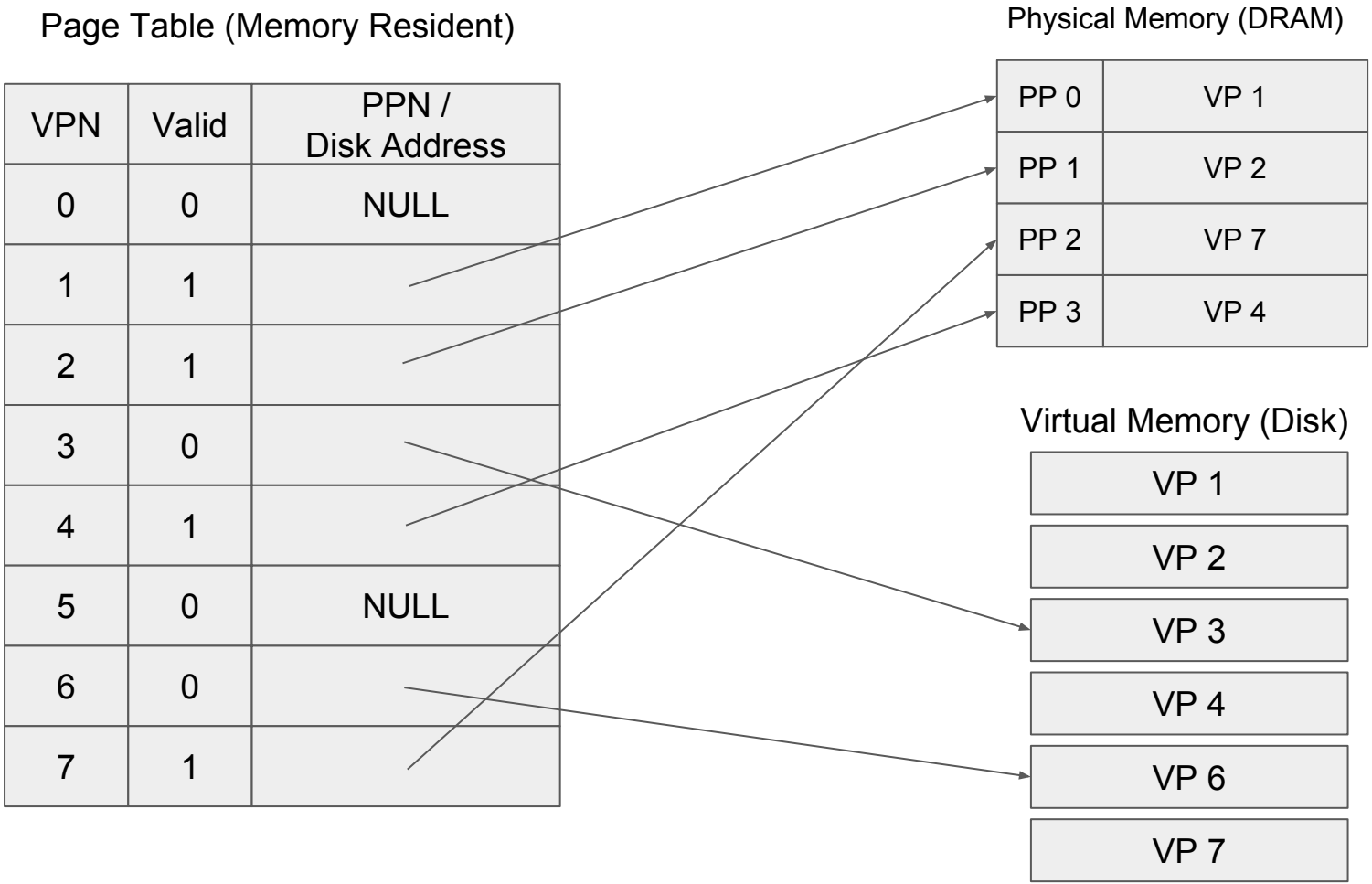
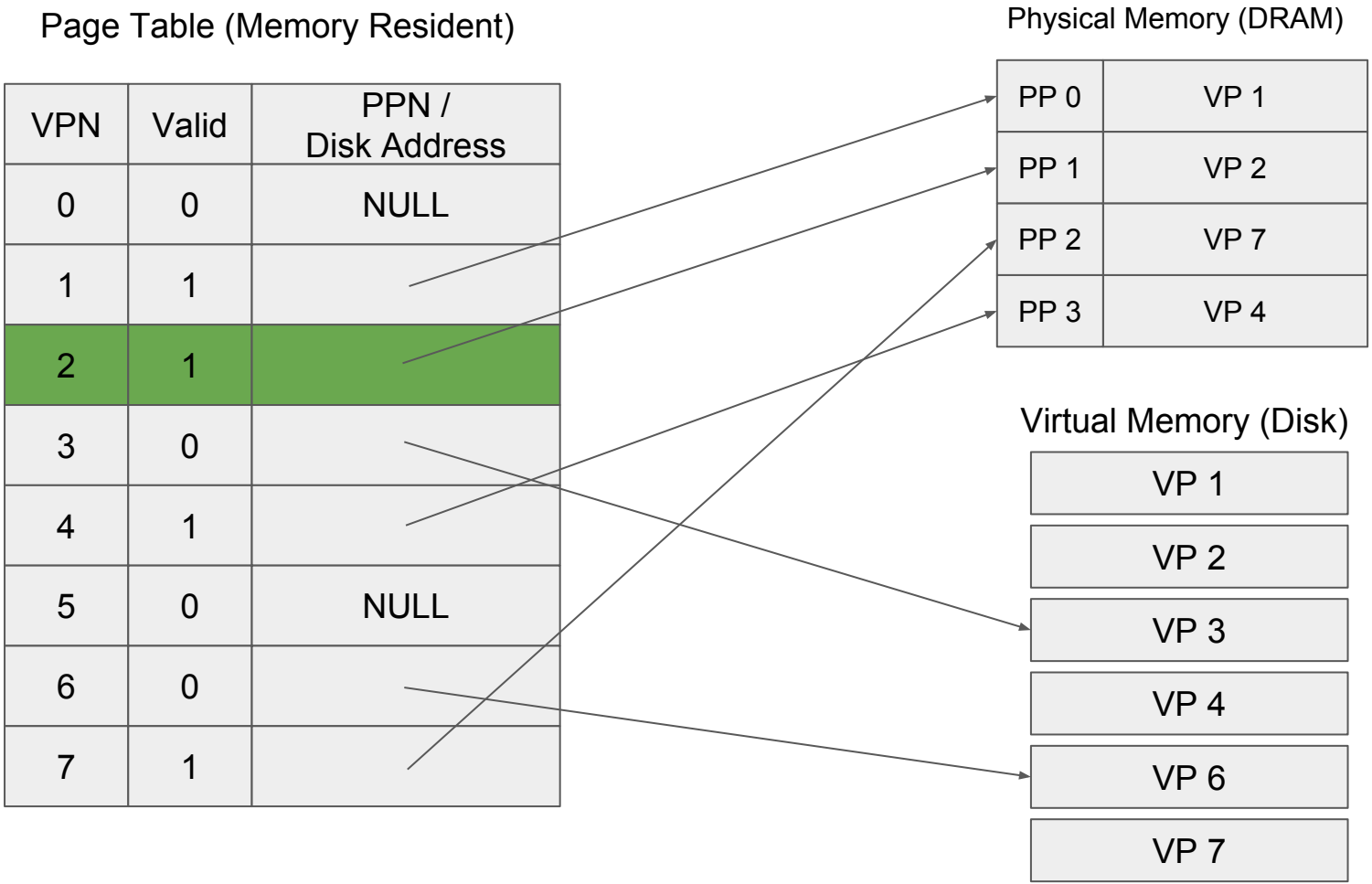
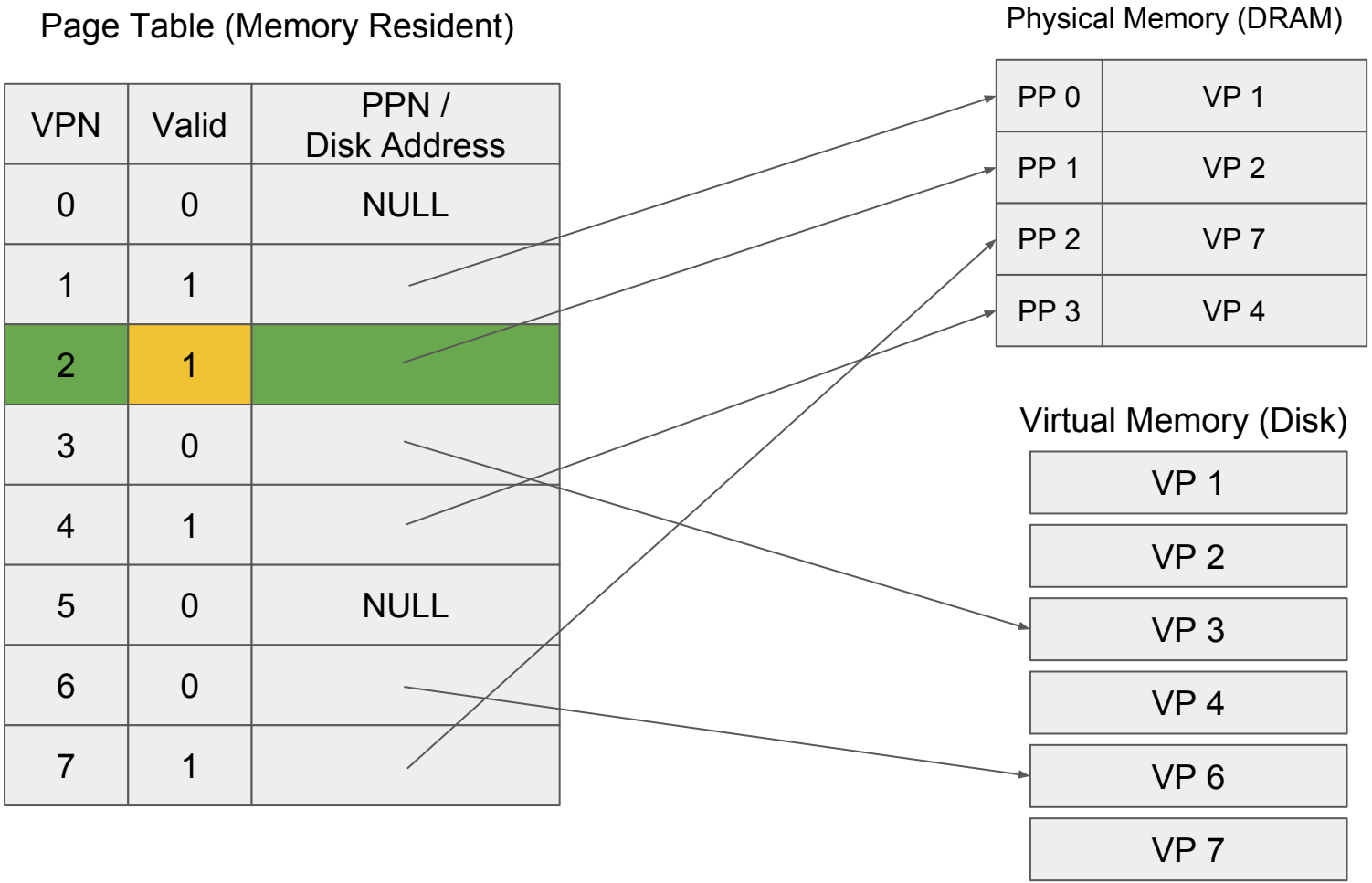
Virtual Memory

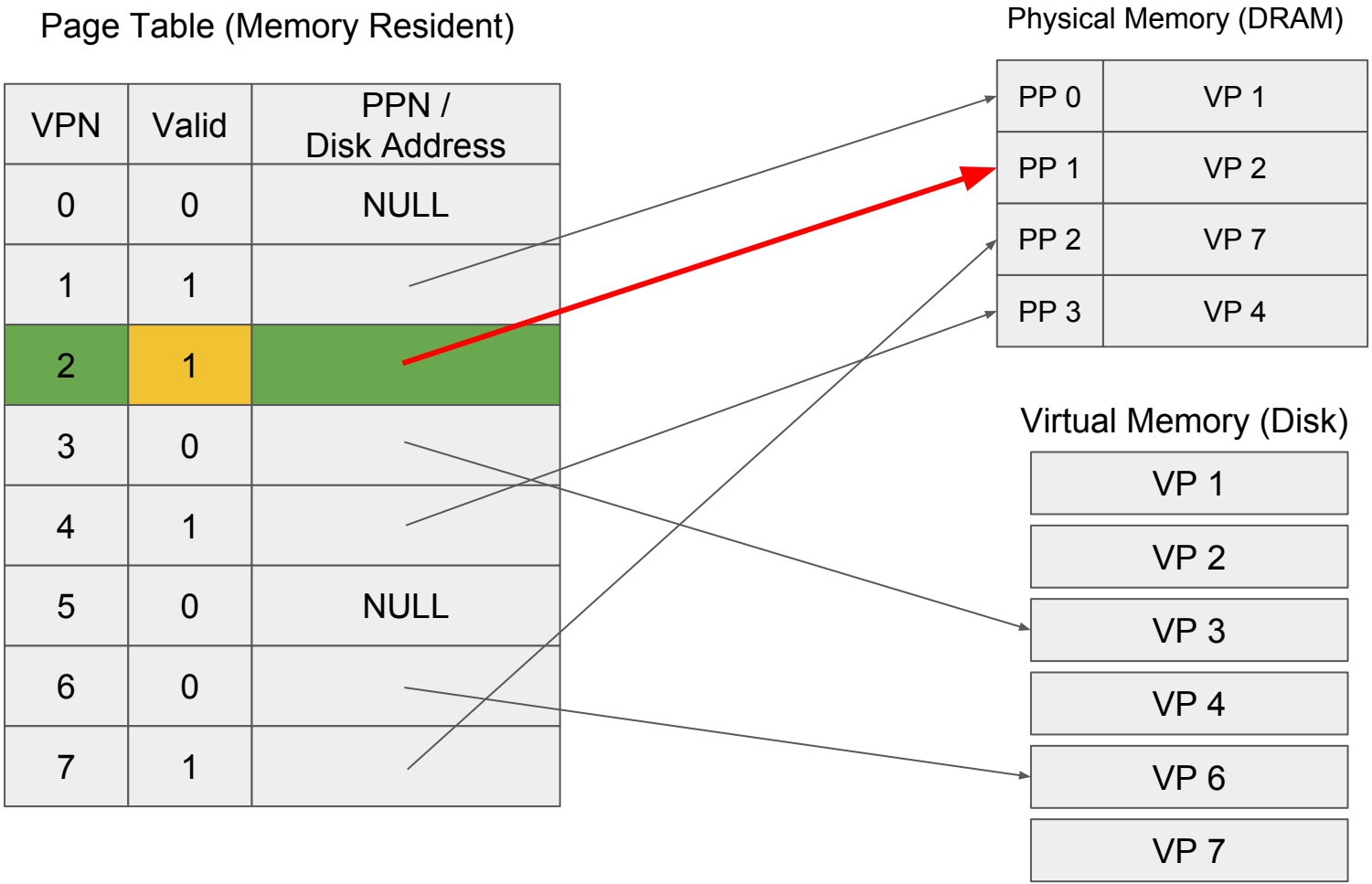
Adalbert **Gerald** Soosai Raj

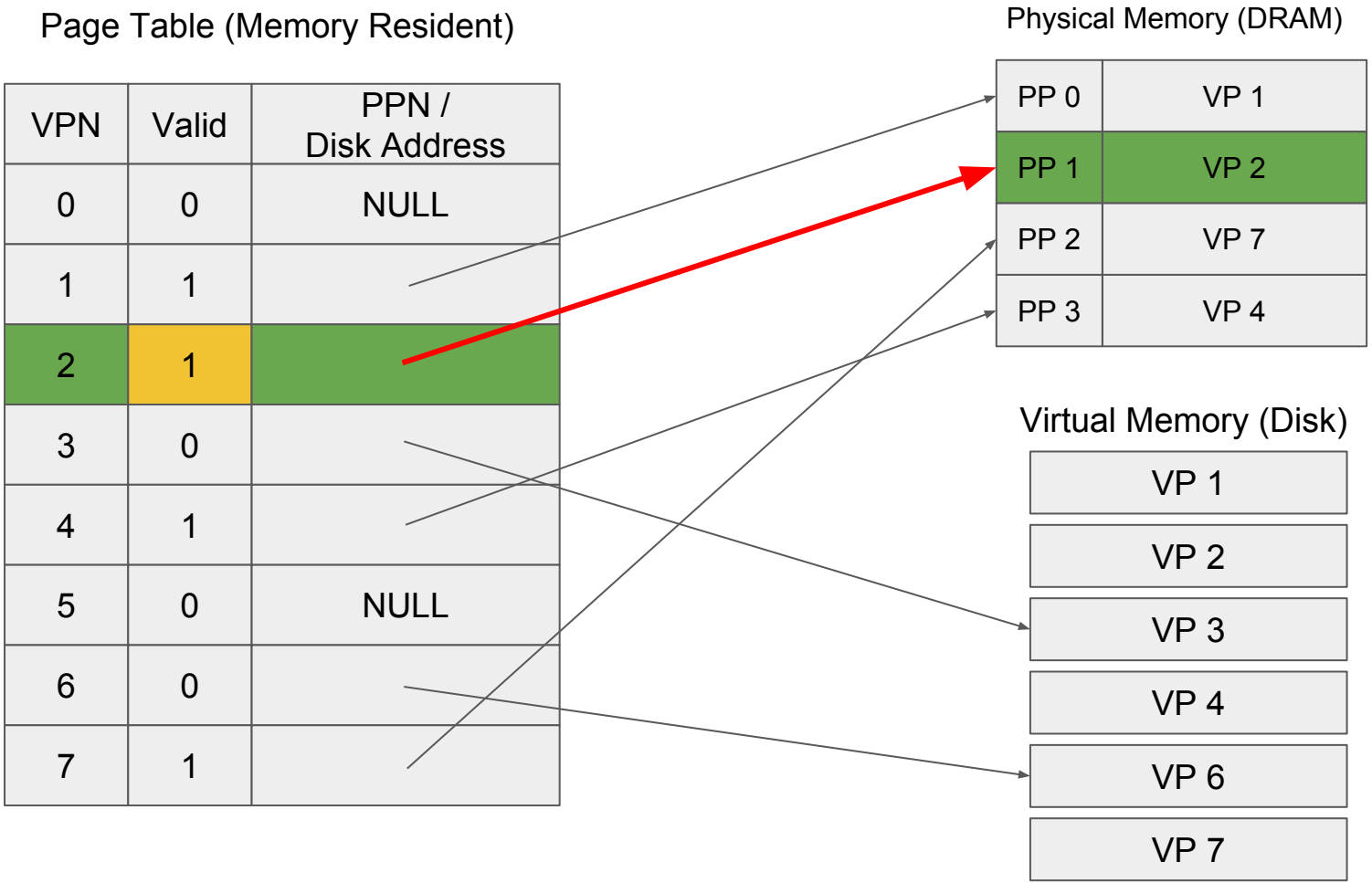

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

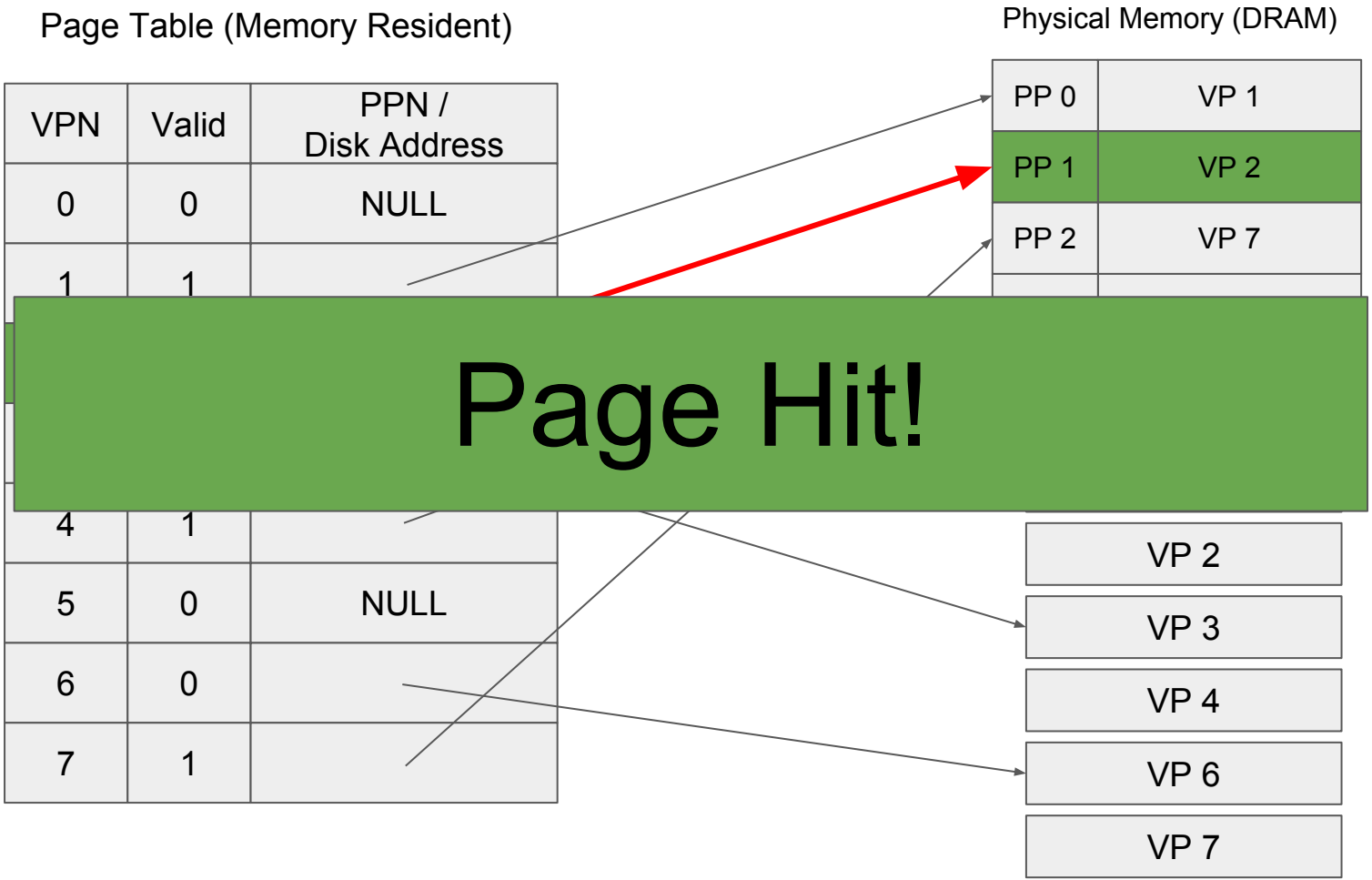
Read Virtual Page #2


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

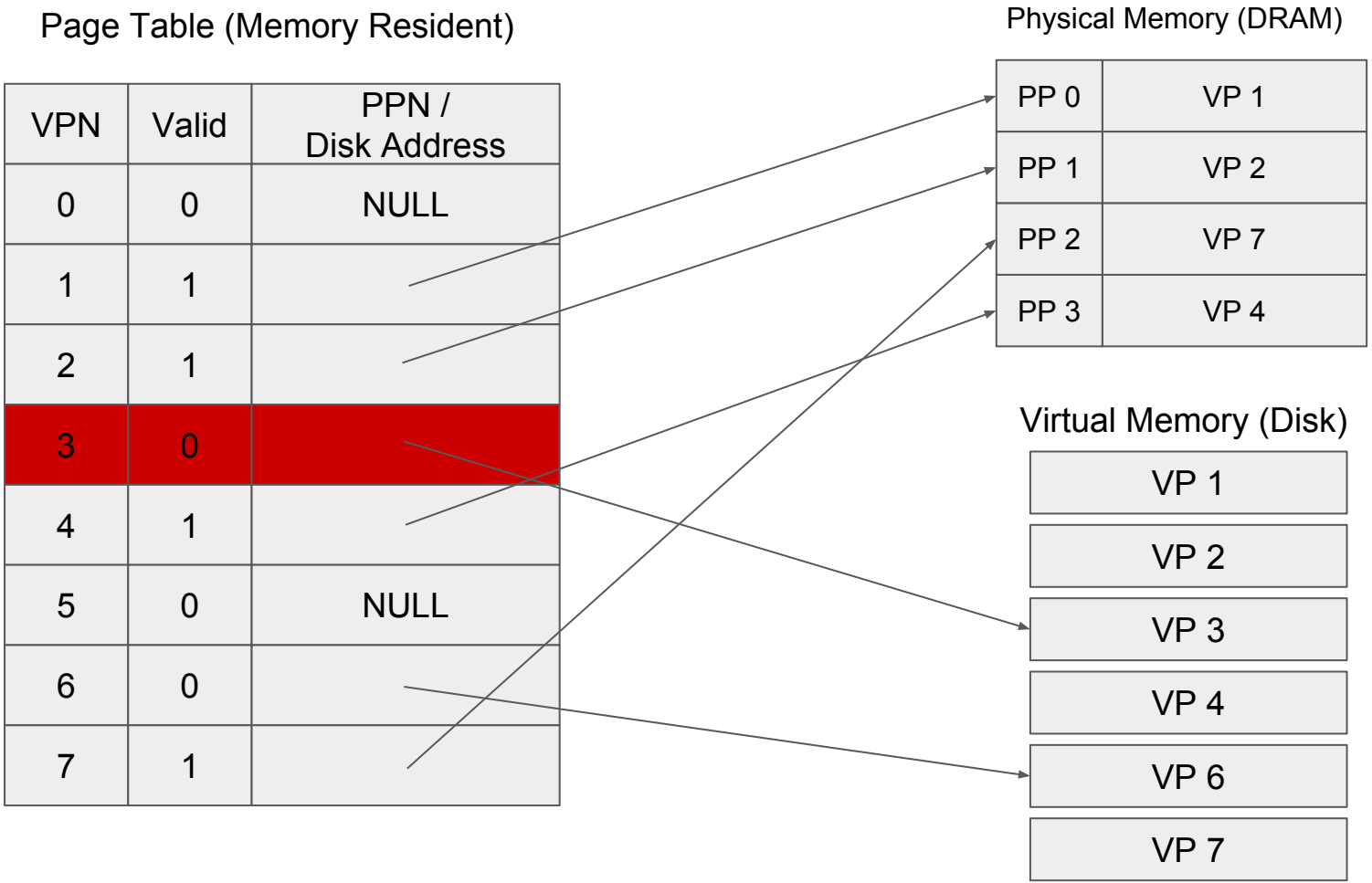

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

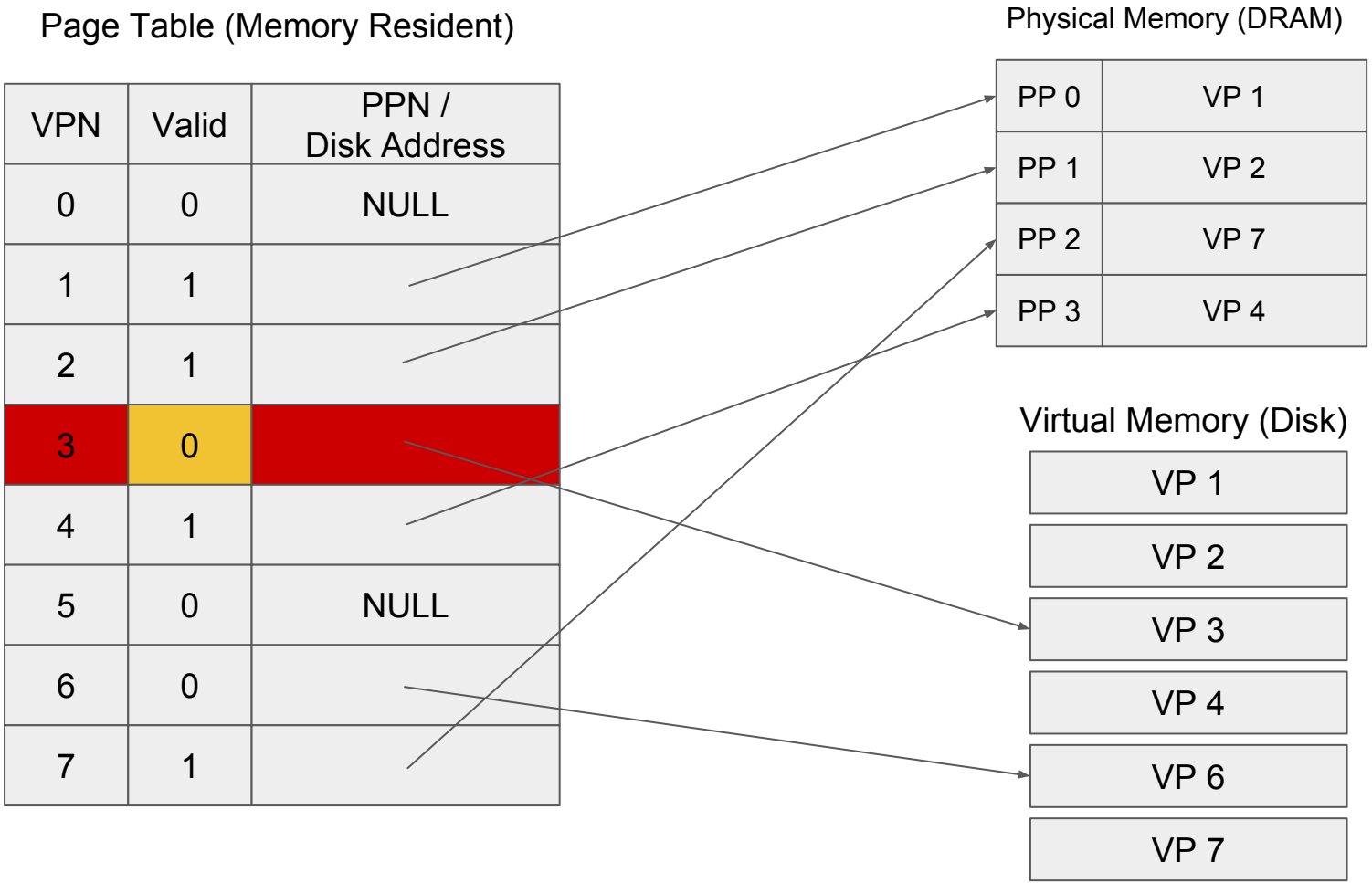

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

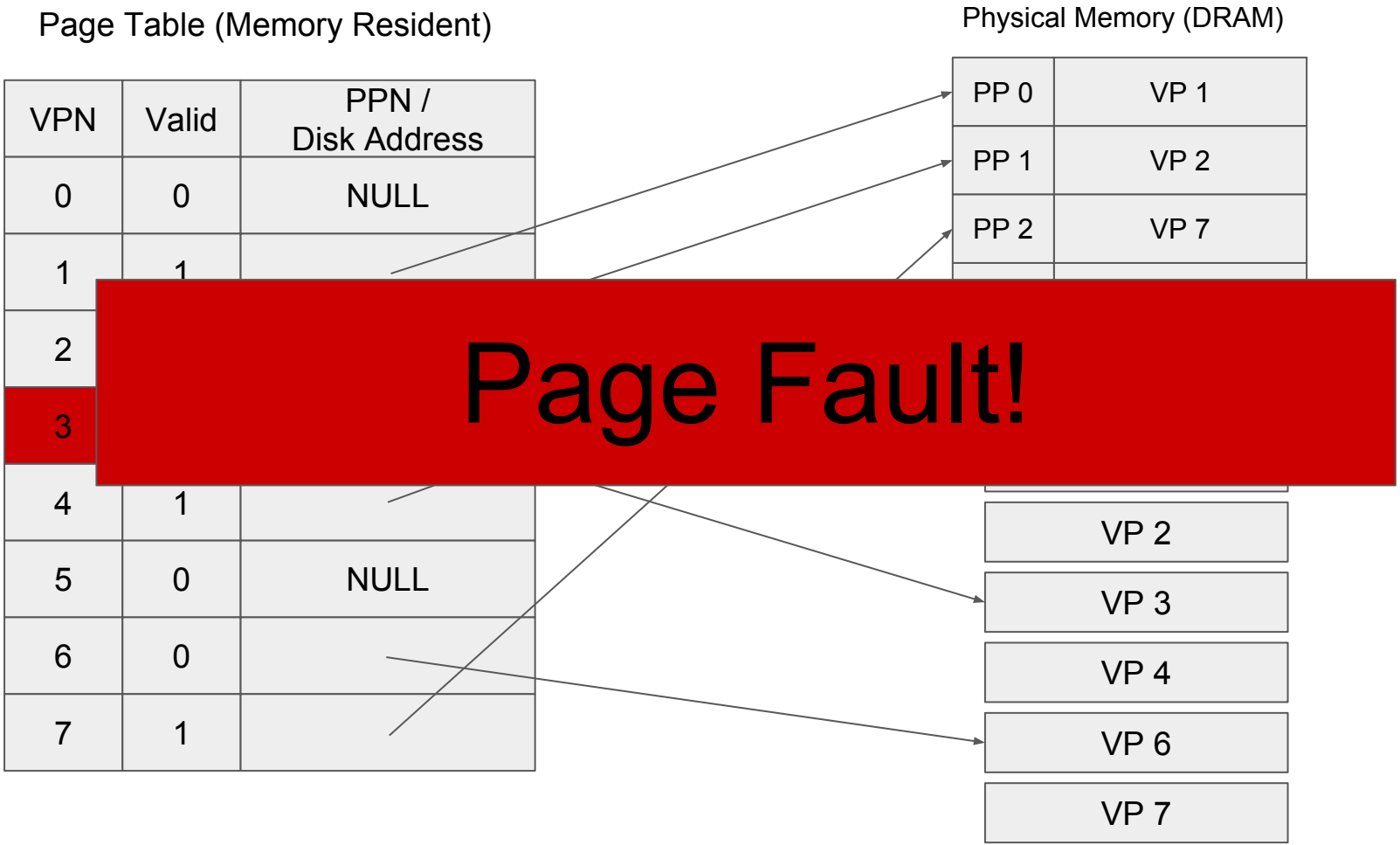

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
VP 2
VP 3
VP 4
VP 6
VP 7
Page Hit!

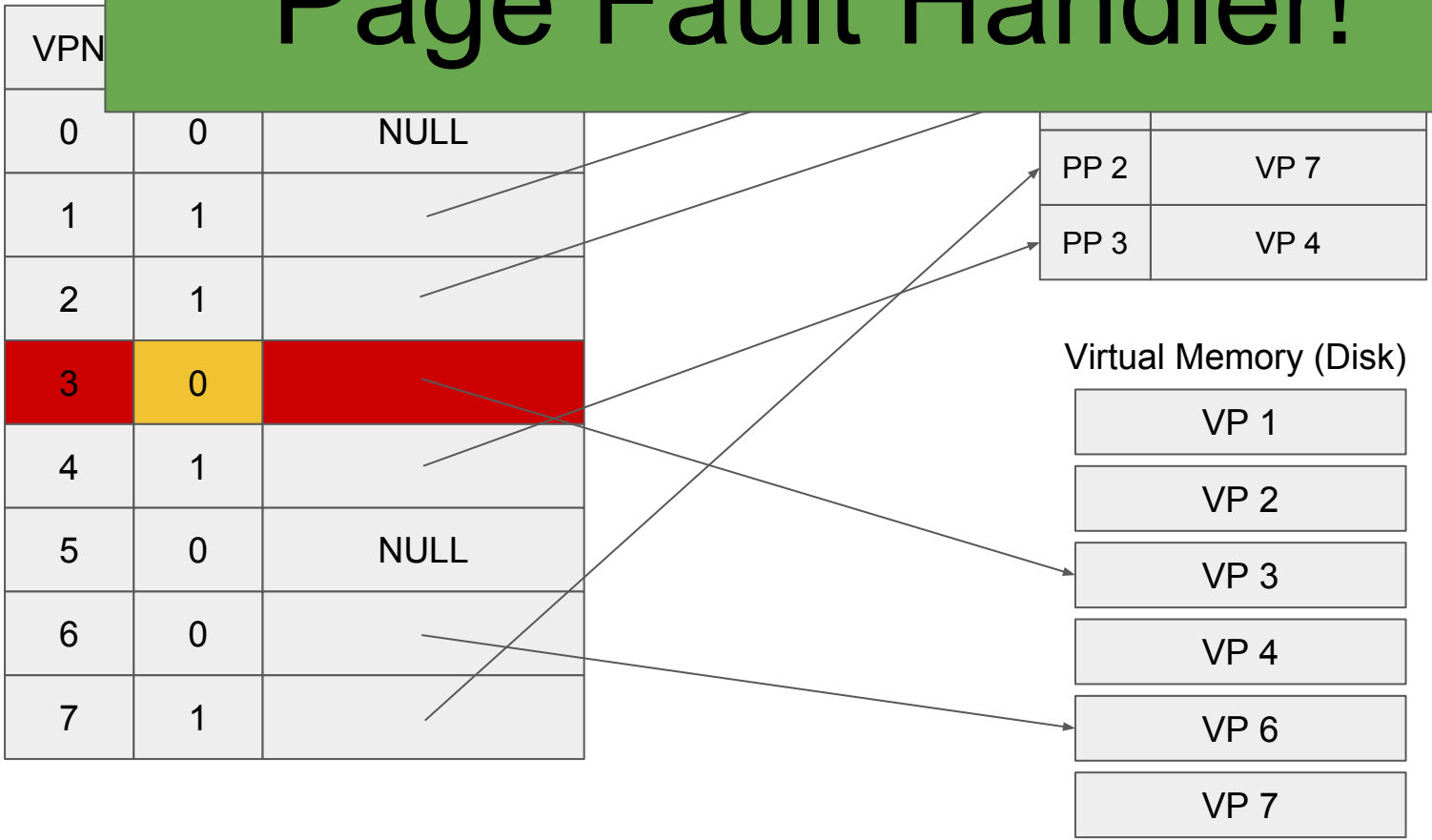
Read Virtual Page #3

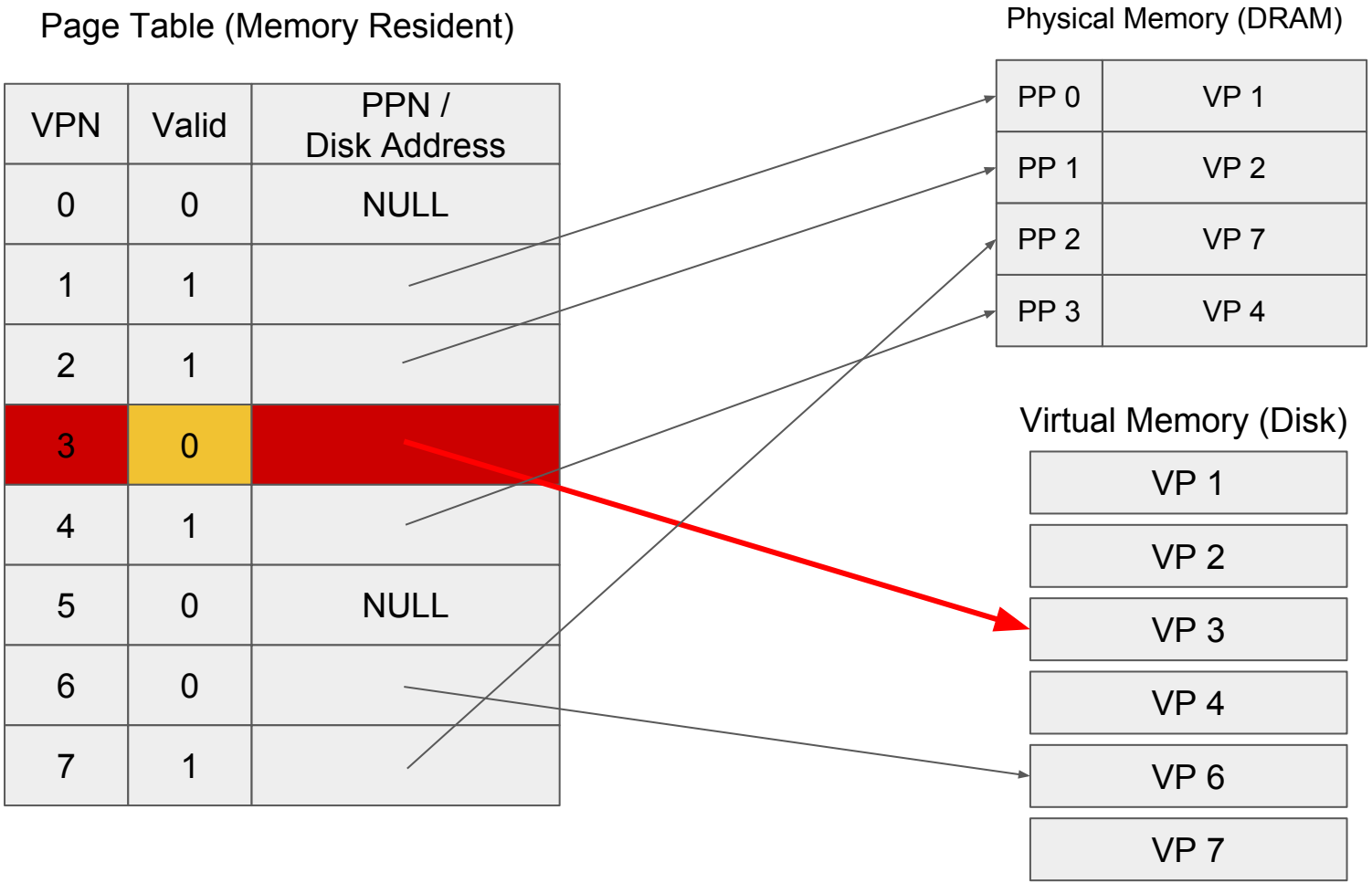

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

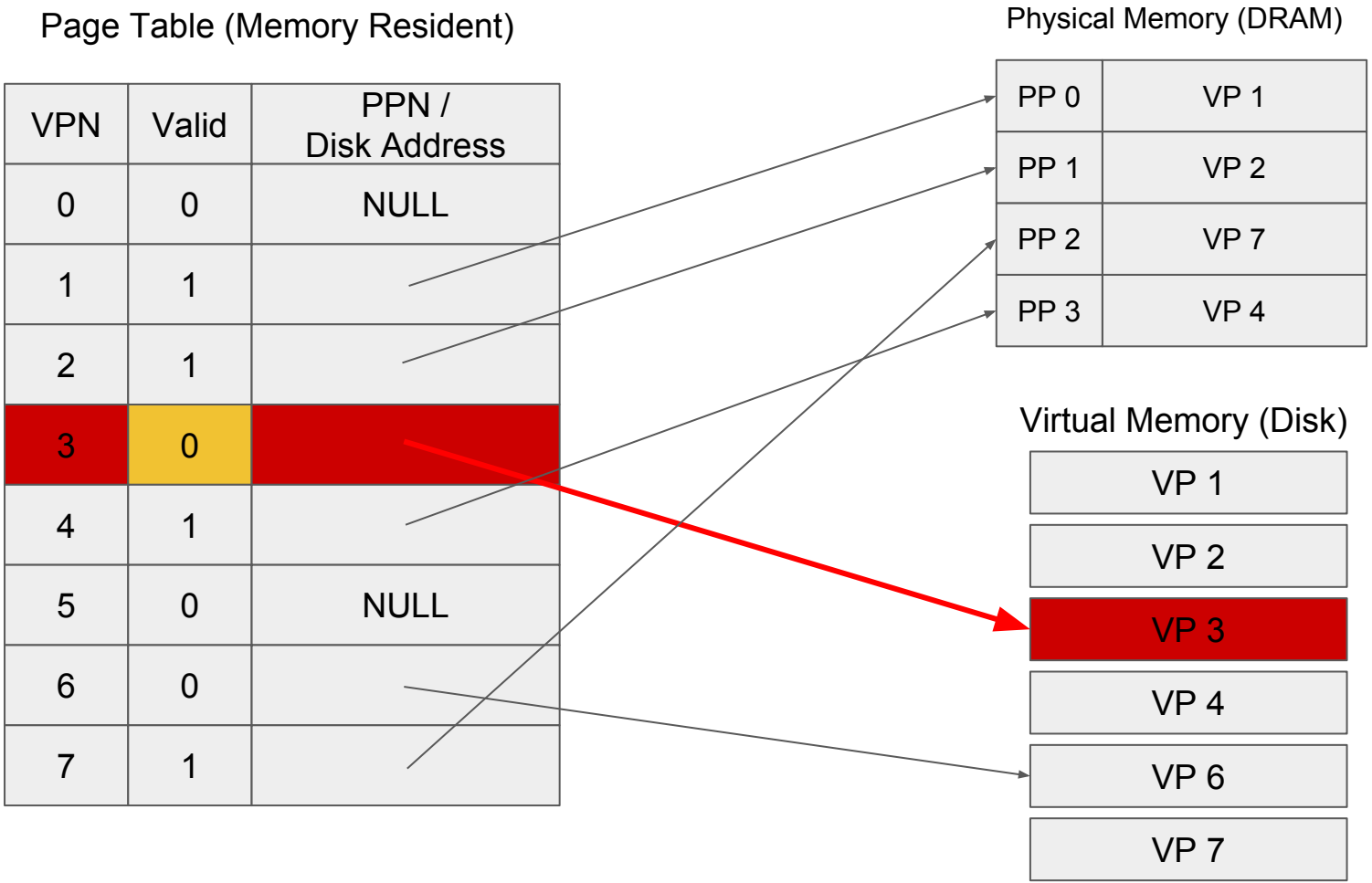

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

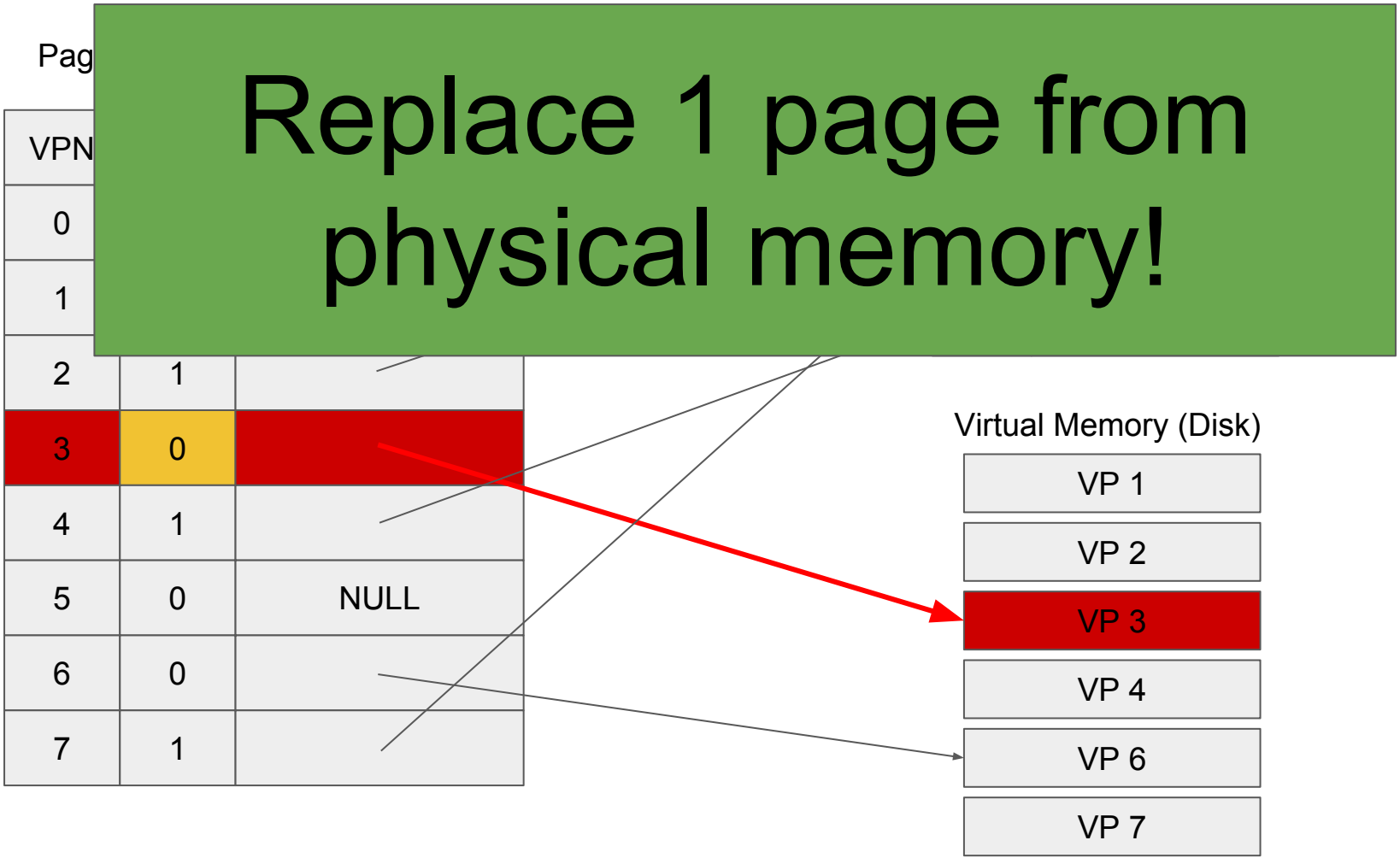

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
2
3
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
VP 2
VP 3
VP 4
VP 6
VP 7
Page Fault!

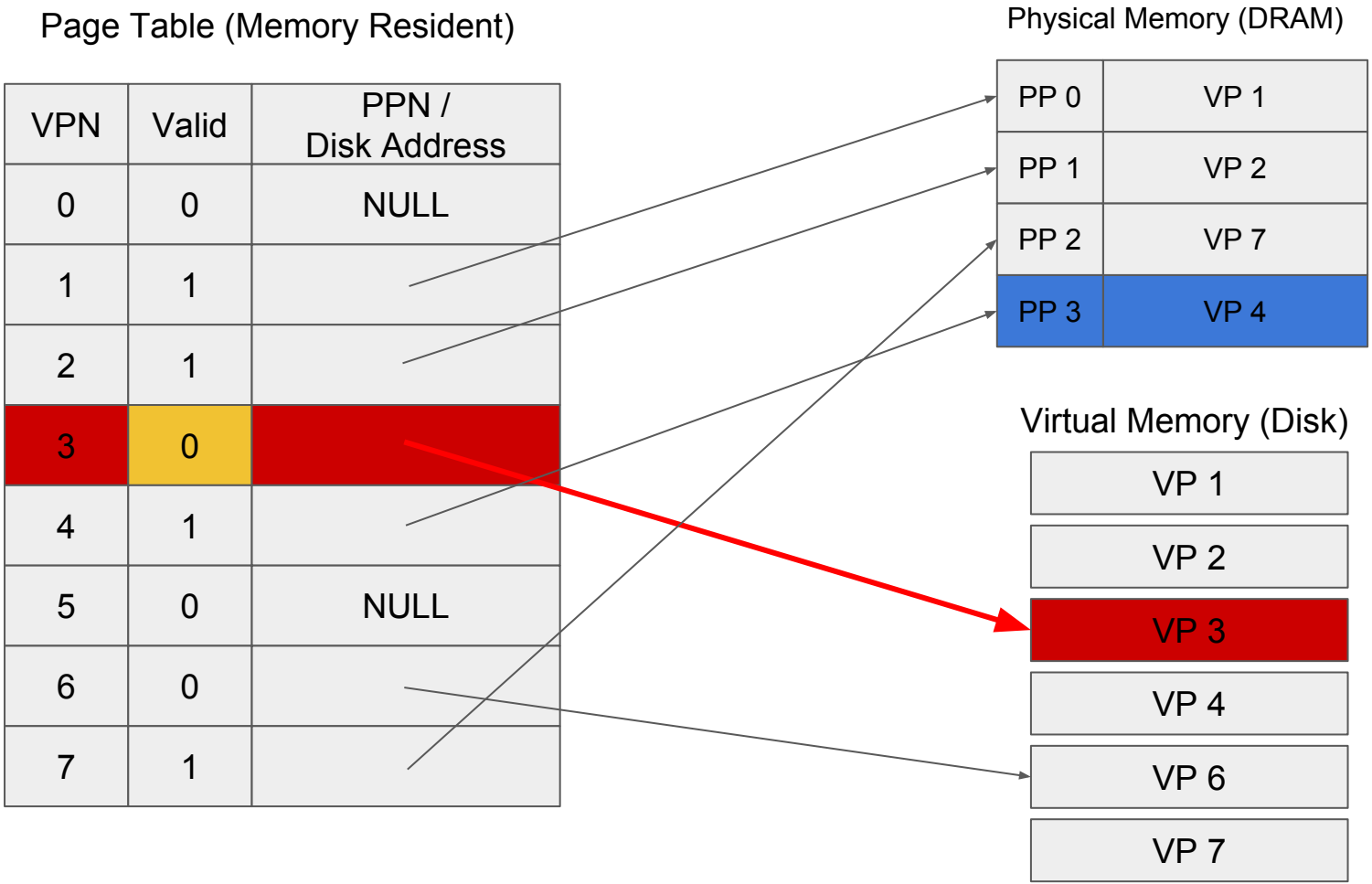
Page Fault Handler!

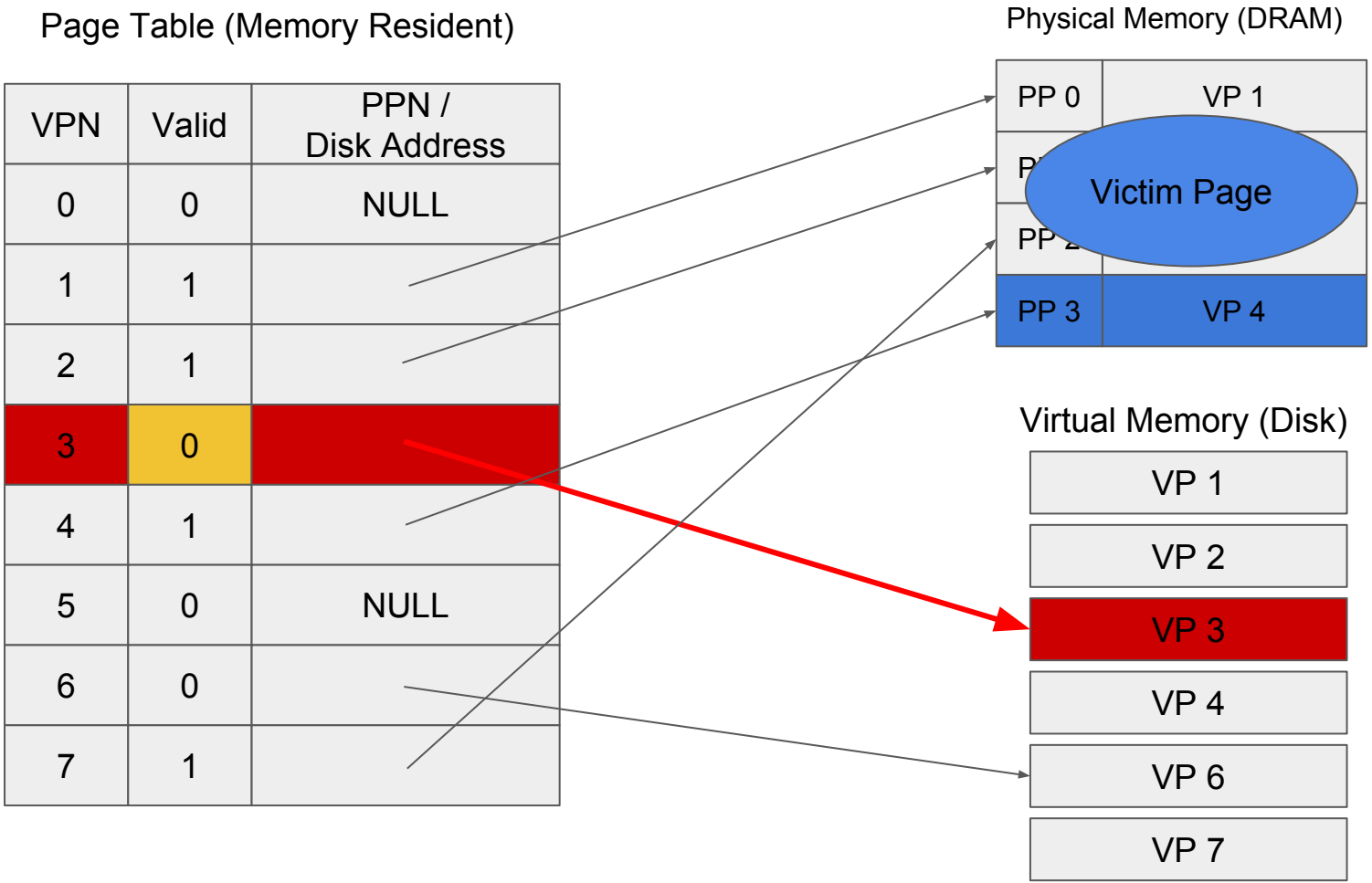


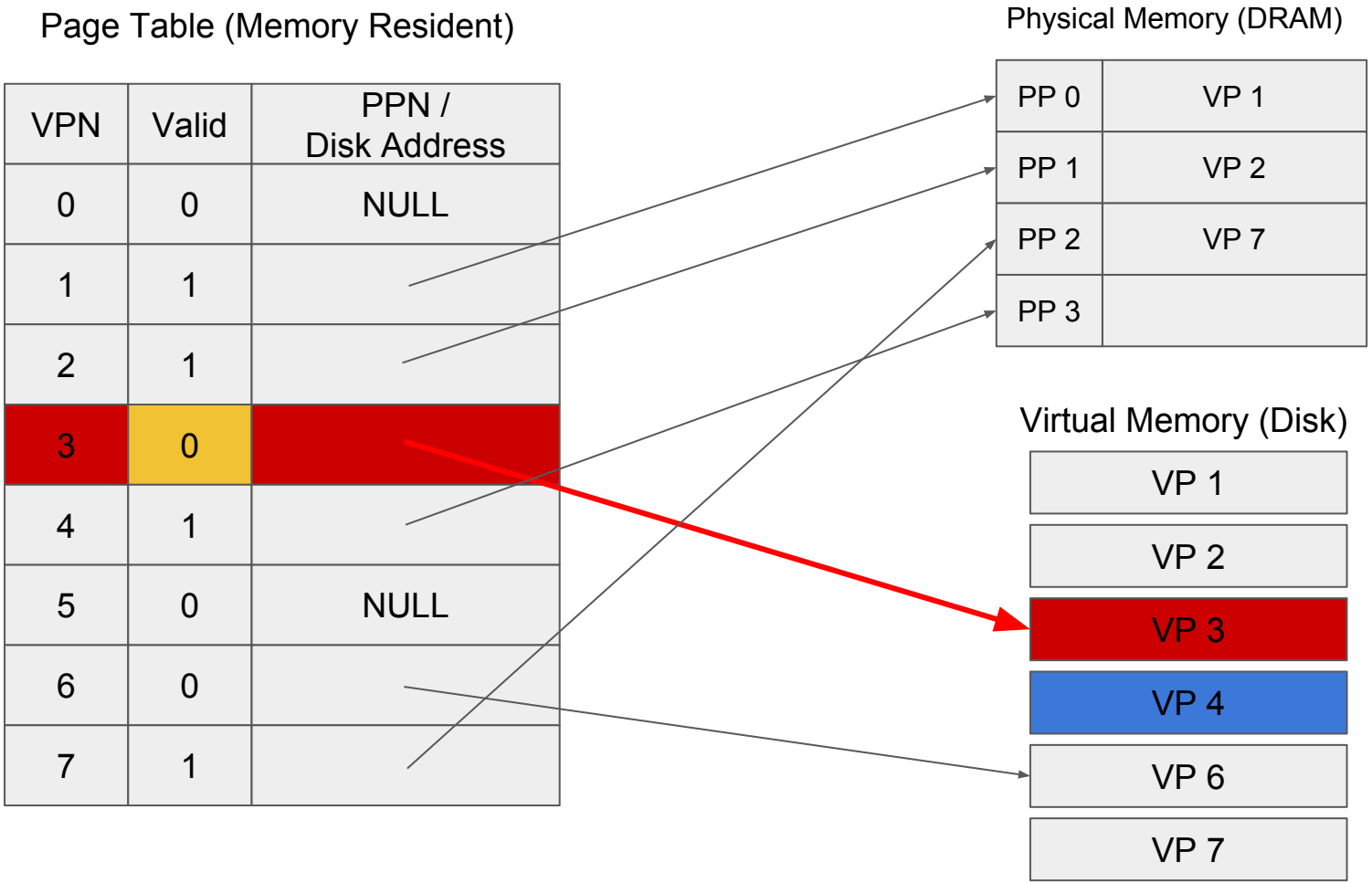

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

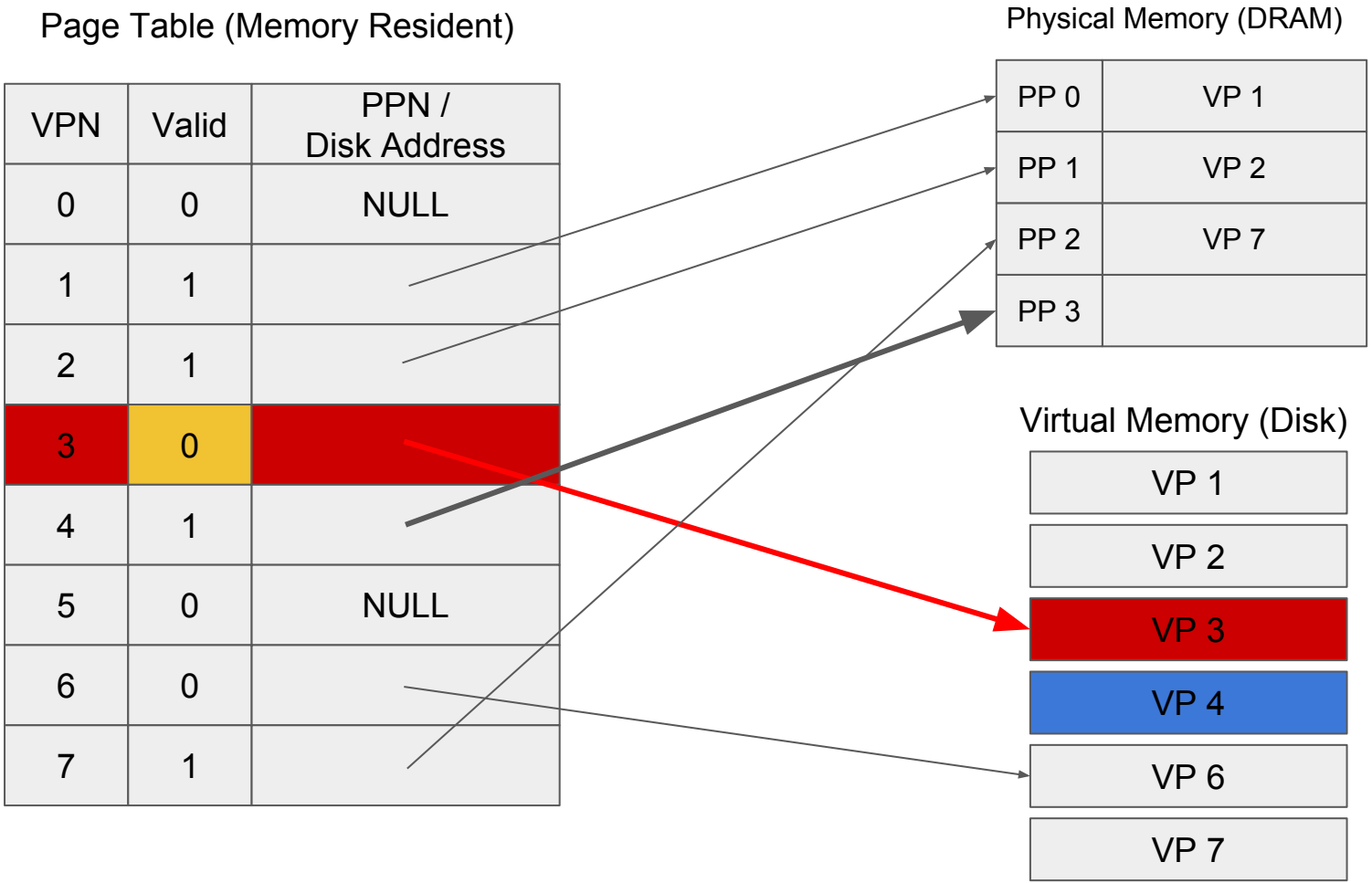

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

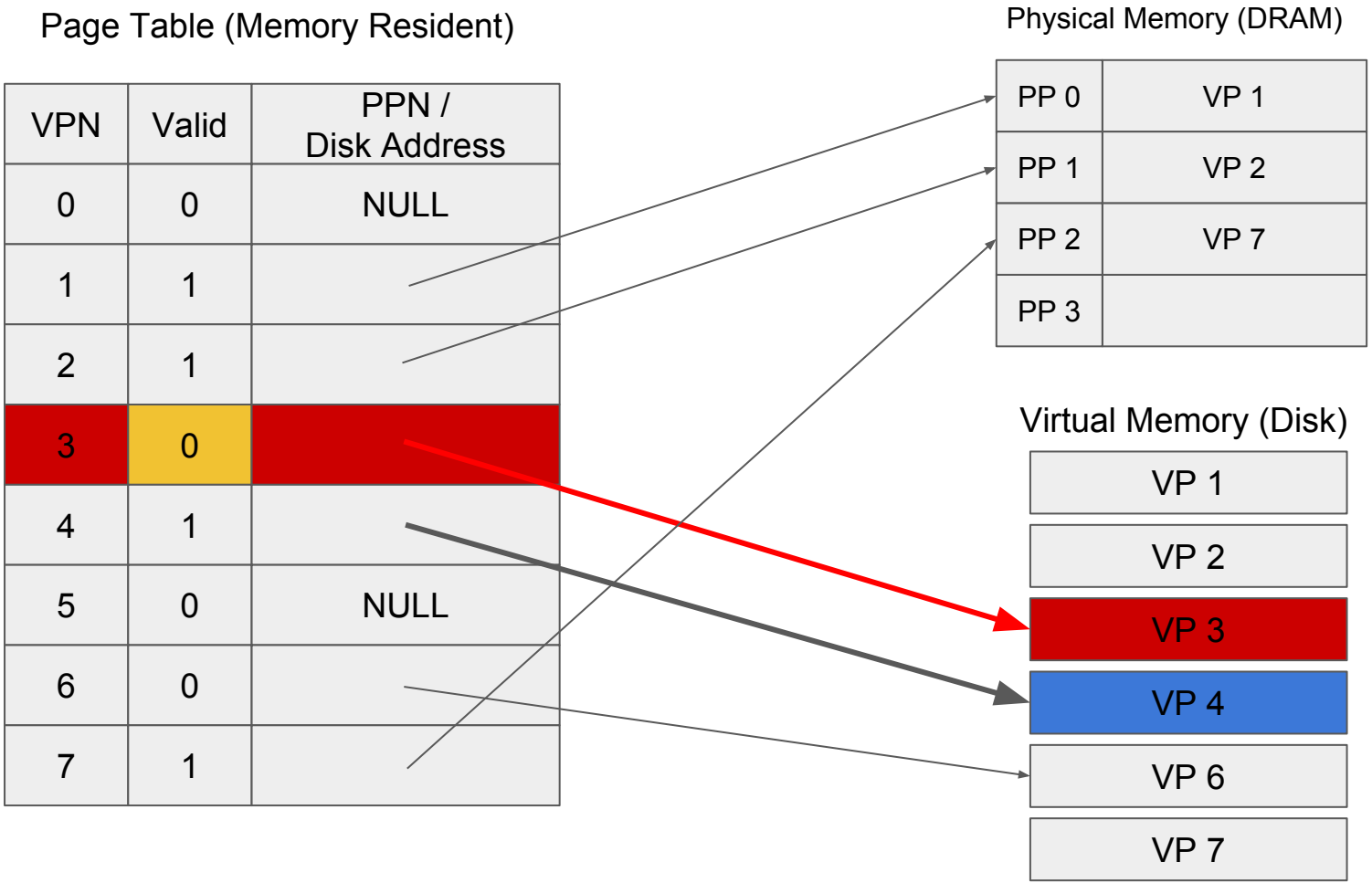

Pag
Replace 1 page from physical memory!
VPN
0
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

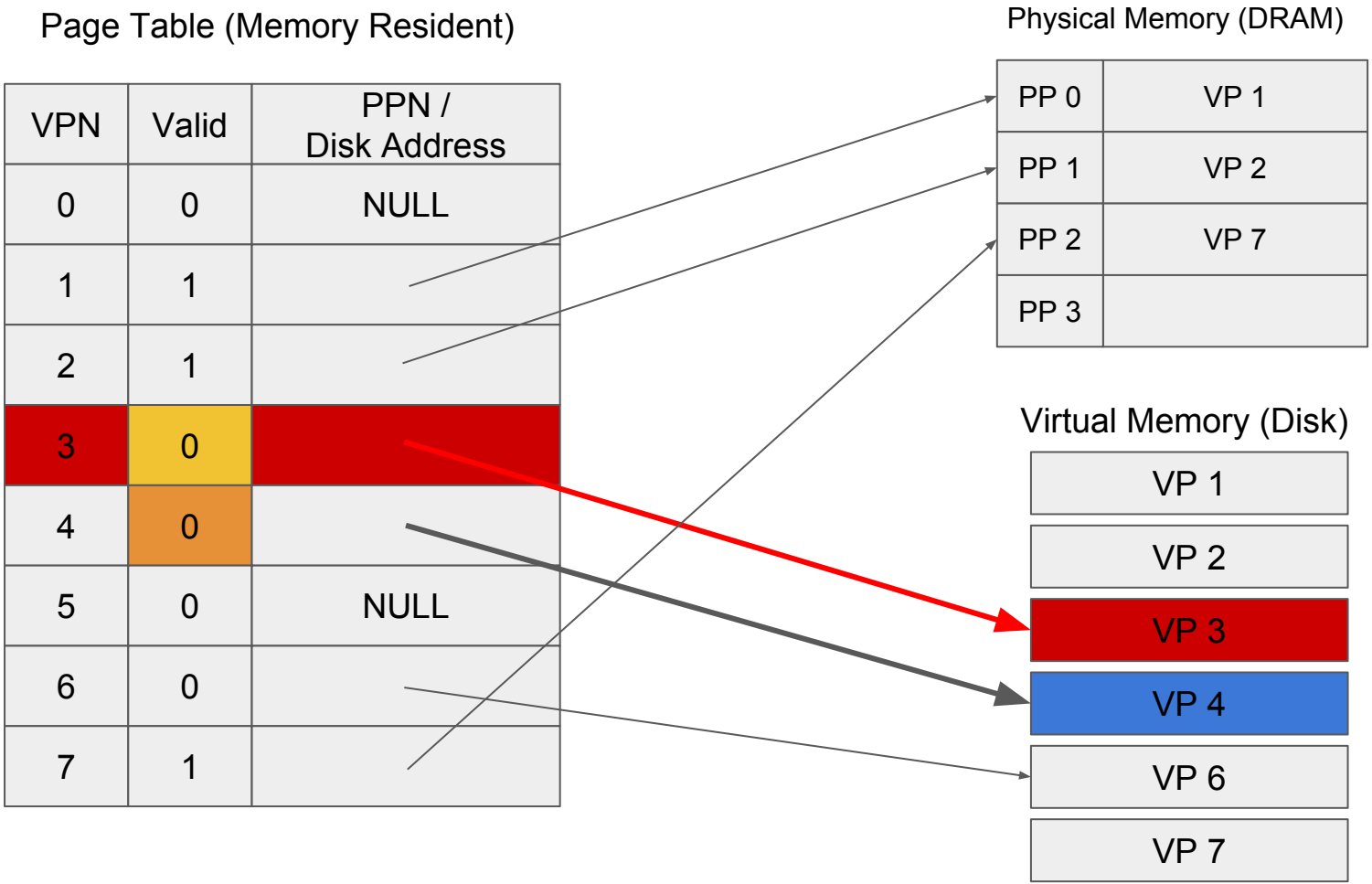

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

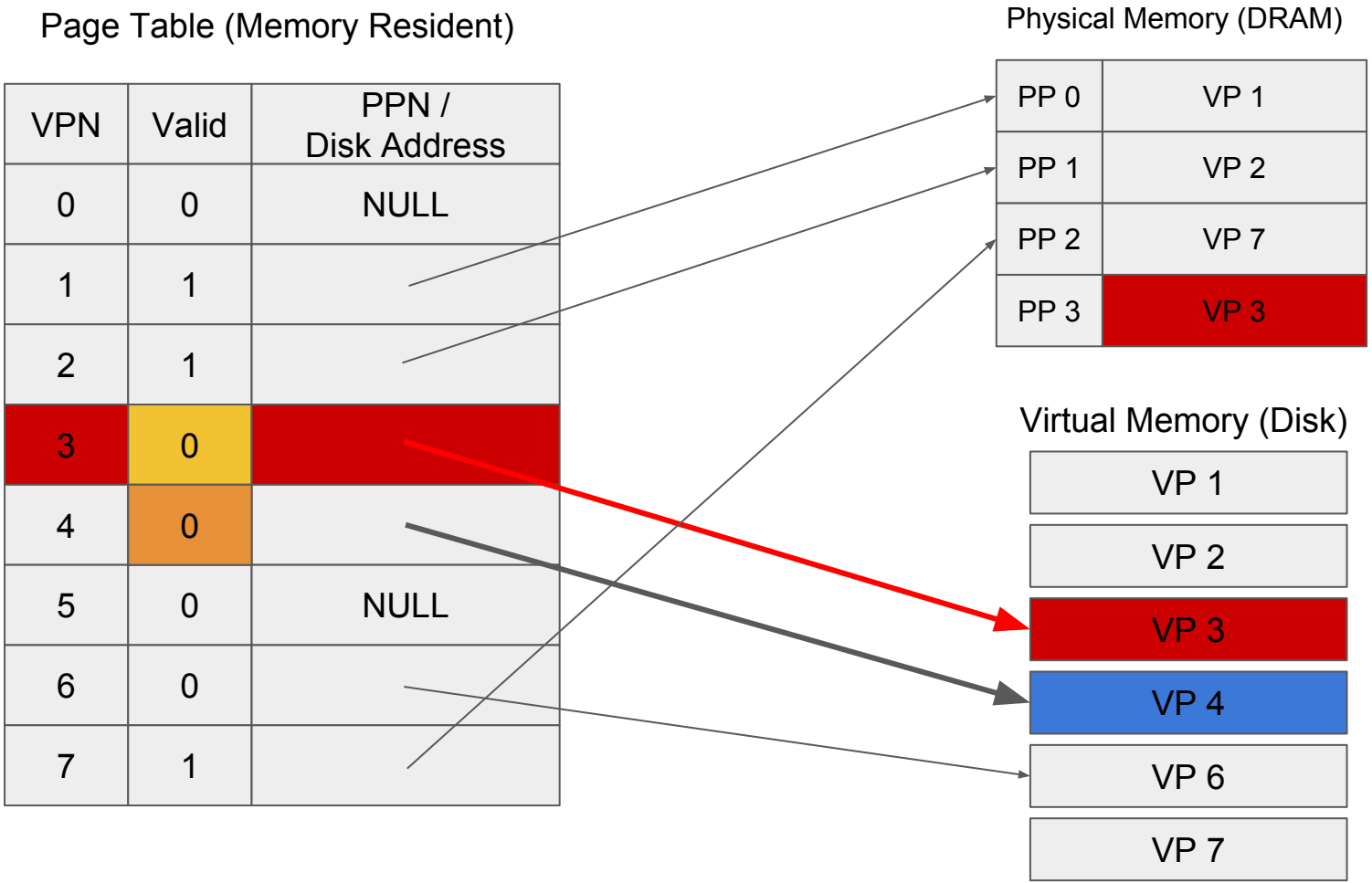

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
Victim Page
PP 3
VP 4
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

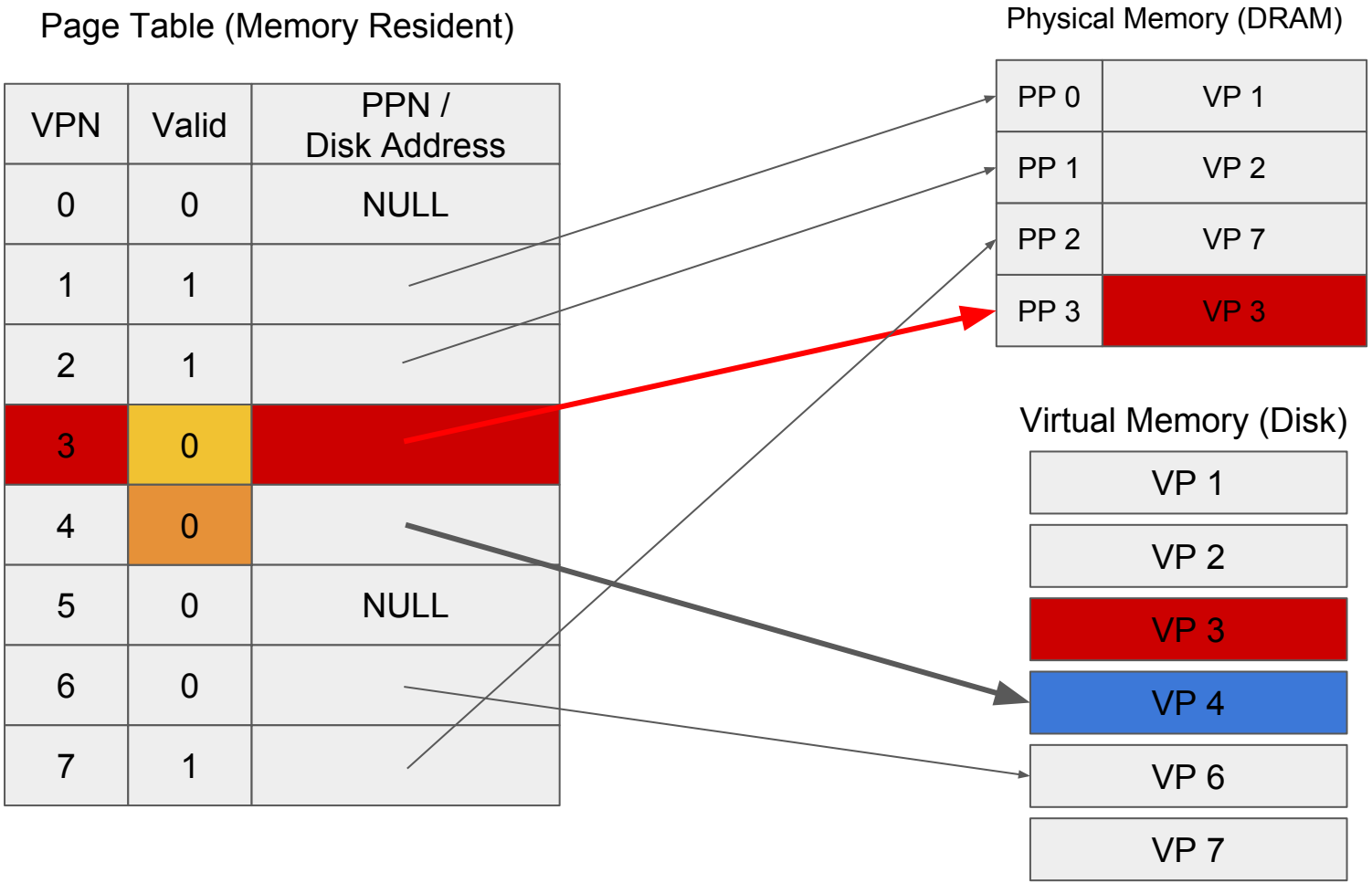

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

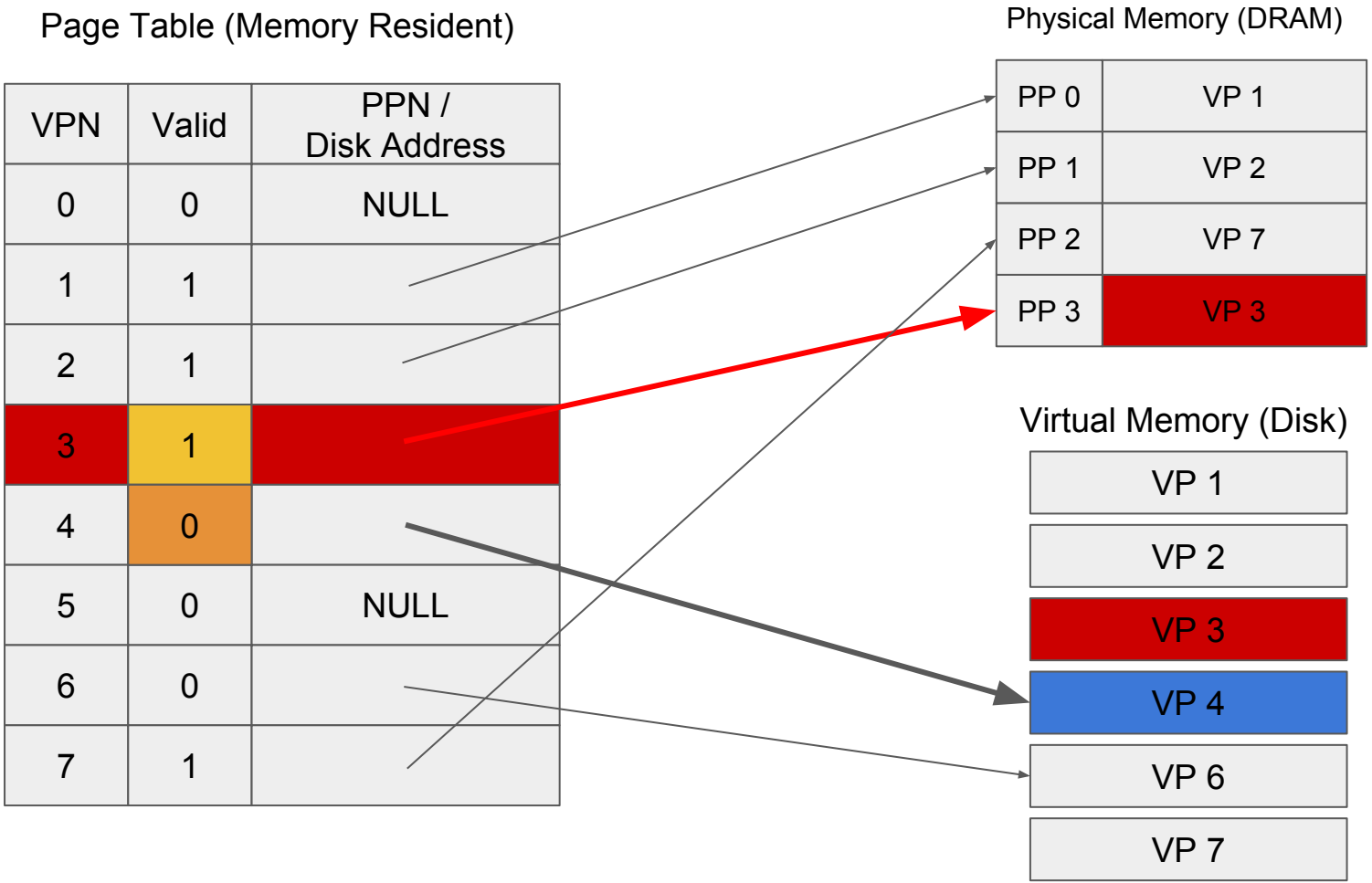

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7

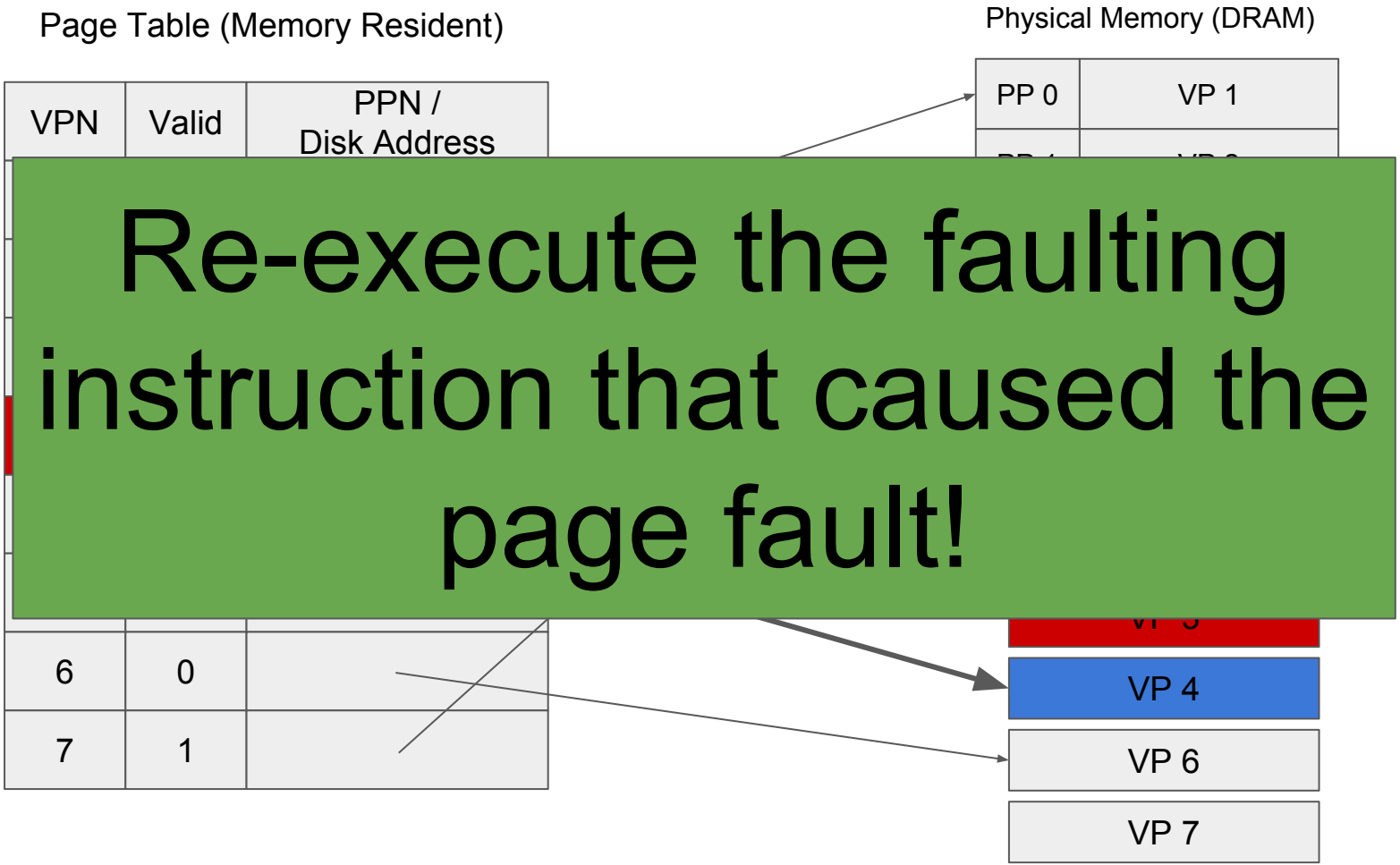

Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
1
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
0
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
0
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
0
4
0
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
0
0
NULL
1
1
2
1
3
1
4
0
5
0
NULL
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
PP 1
VP 2
PP 2
VP 7
PP 3
VP 3
Virtual Memory (Disk)
VP 1
VP 2
VP 3
VP 4
VP 6
VP 7


Page Table (Memory Resident)
VPN
Valid
PPN / Disk Address
6
0
7
1
Physical Memory (DRAM)
PP 0
VP 1
VP 4
VP 6
VP 7
Re-execute the faulting instruction that caused the page fault!

Thrashing

Memory Protection

Page Table of Process i

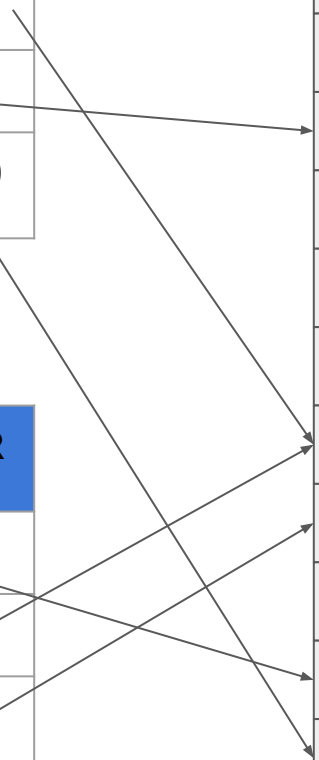
VPN	VALID	SUP	READ	WRITE	ADDR
0	1	no	yes	no	PP 6
1	1	no	yes	yes	PP 2
2	1	yes	yes	yes	PP 10

Page Table of Process j

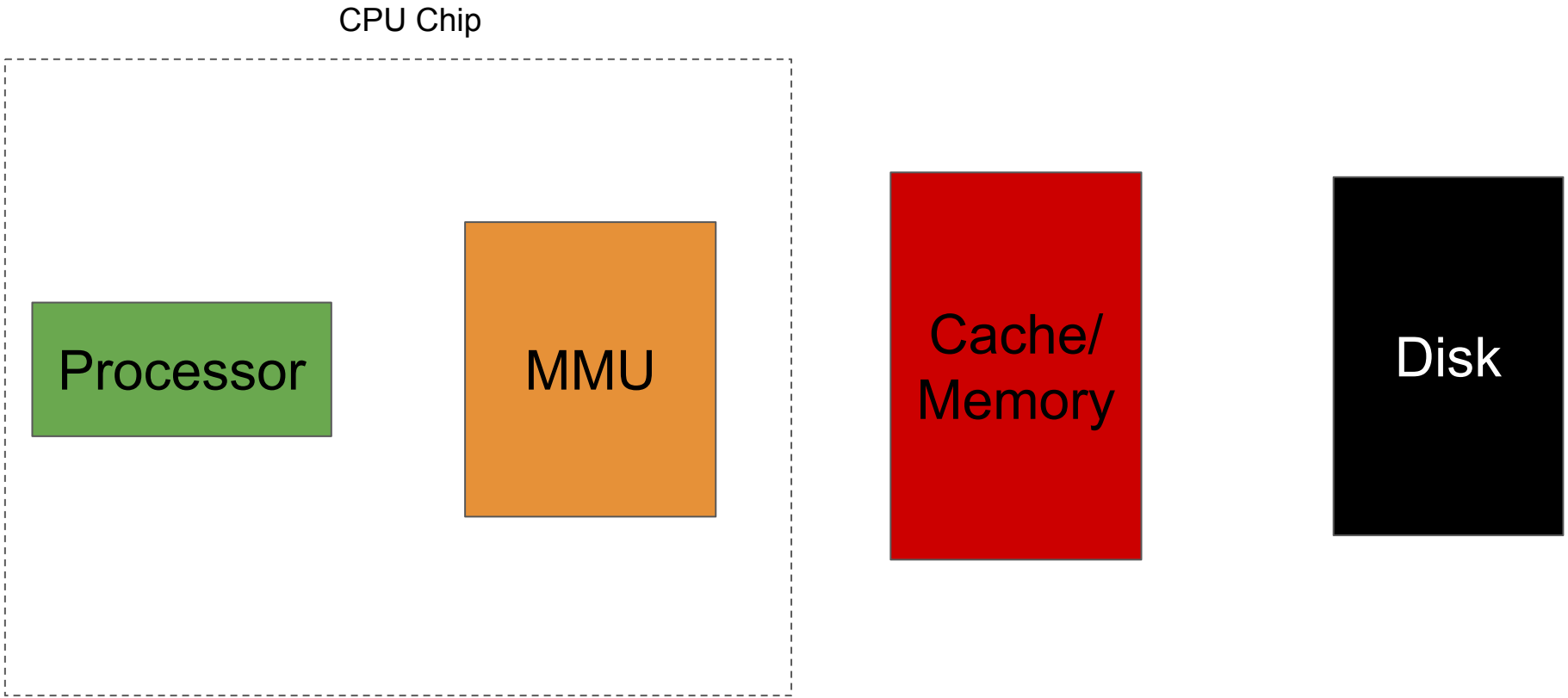
VPN	VALID	SUP	READ	WRITE	ADDR
0	1	no	yes	no	PP 9
1	1	yes	yes	yes	PP 6
2	1	no	yes	yes	PP 7

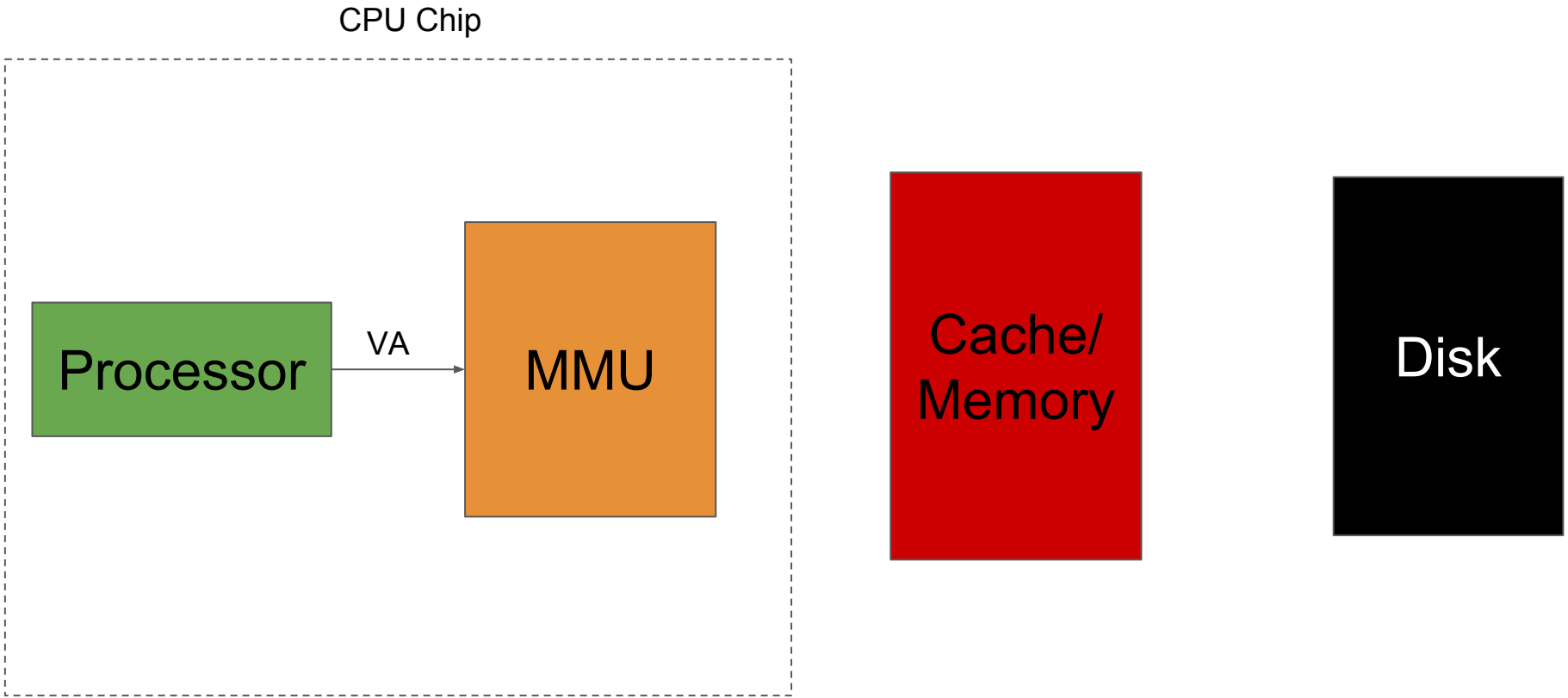
Physical Memory (DRAM)

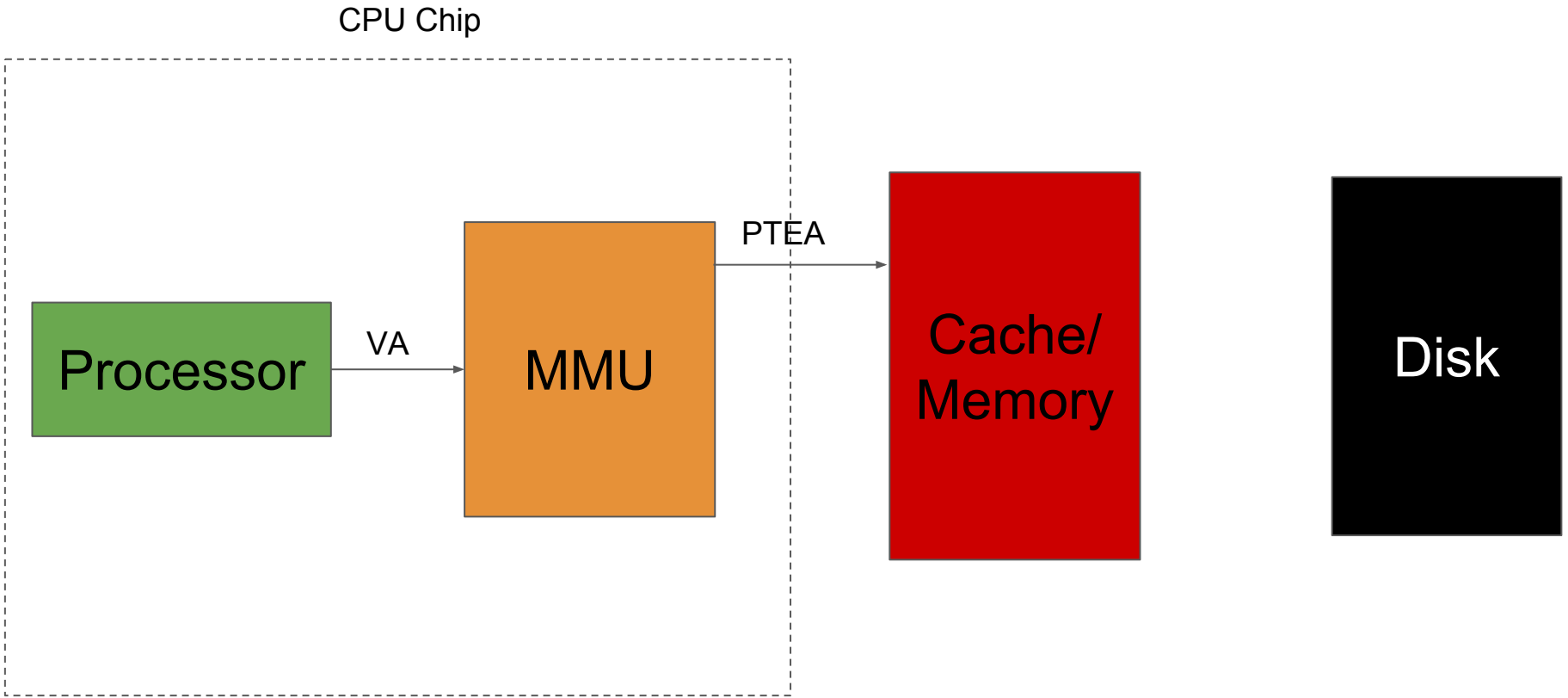
PPN	Contents
0	
1	
2	VP 1
3	
4	
5	
6	Shared page
7	VP 3
8	
9	VP 1
10	VP 3



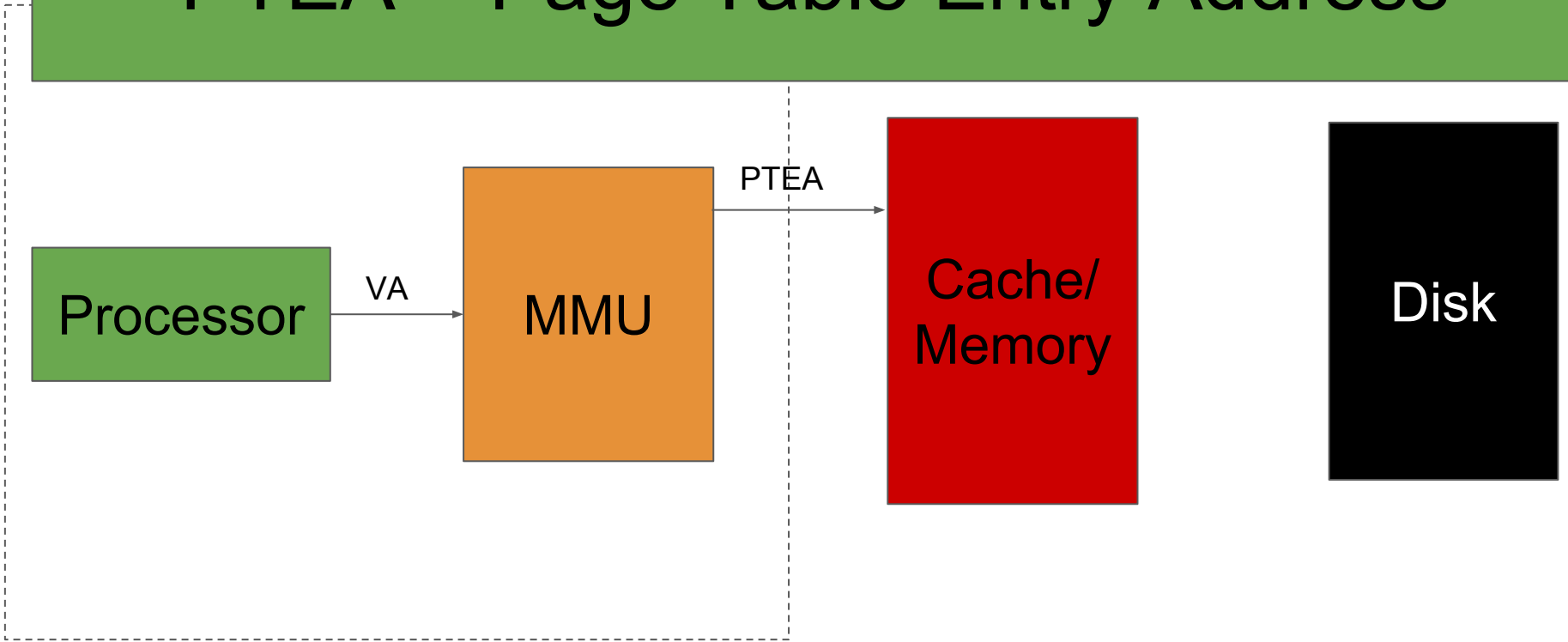
Steps in Page Hit


CPU Chip
Processor
MMU
Cache/
Memory
Disk

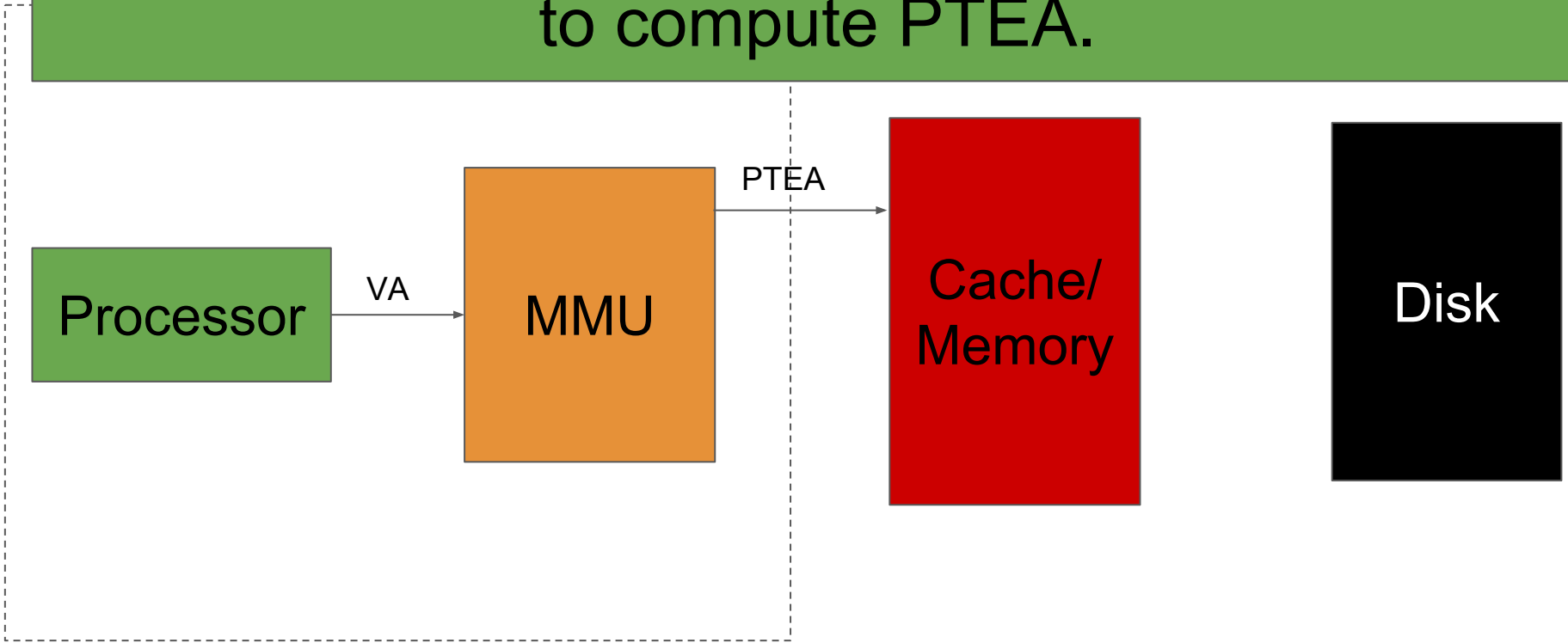

CPU Chip
Processor
VA
MMU
Cache/
Memory
Disk


CPU Chip
Processor
VA
MMU
PTEA
Cache/
Memory
Disk

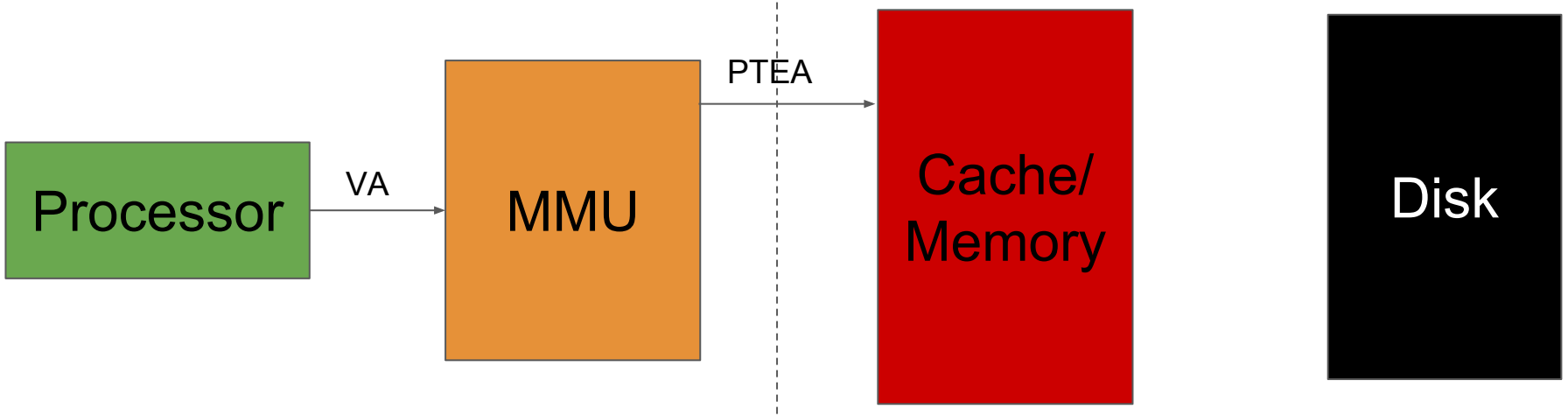
PTEA = Page Table Entry Address



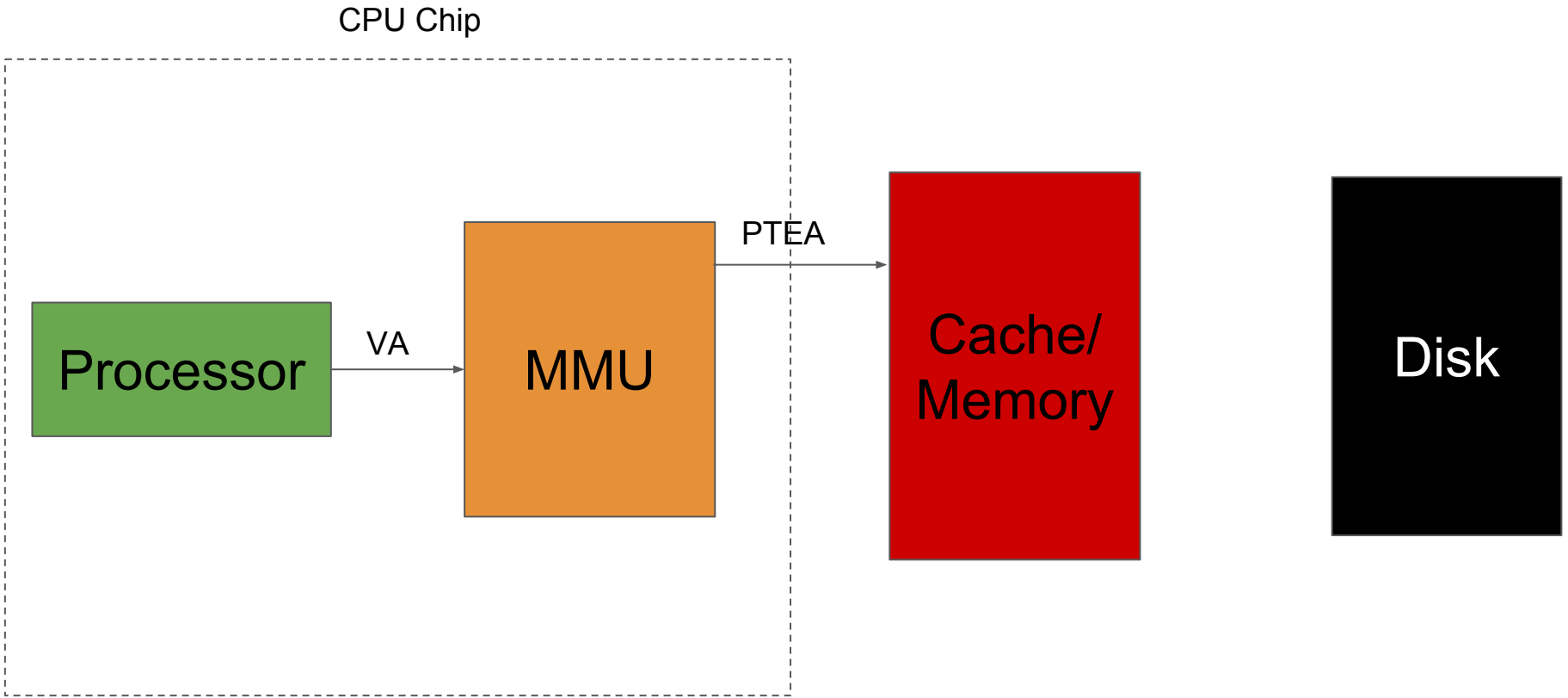
MMU uses Page Table Base Register (PTBR) to compute PTEA.

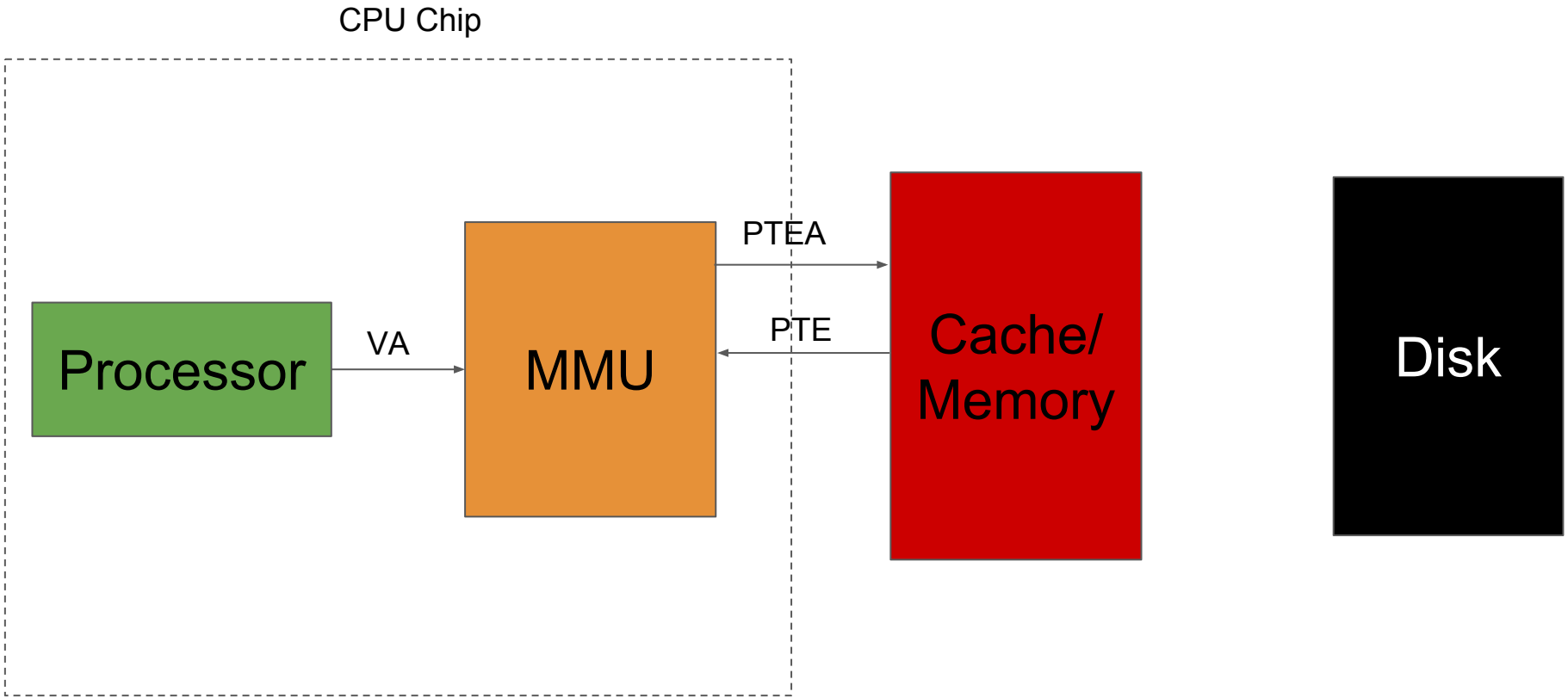


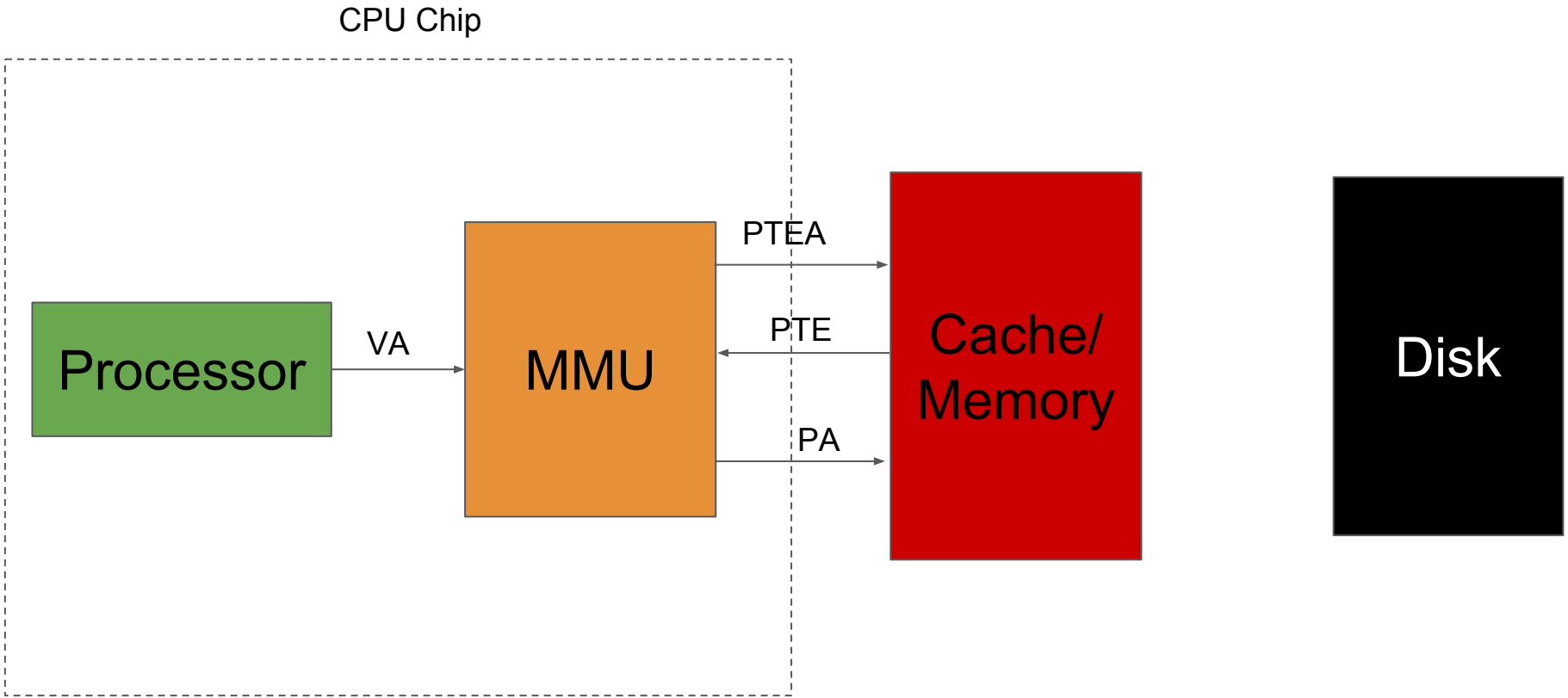
MMU uses Page Table Base Register (PTBR) to compute PTEA.

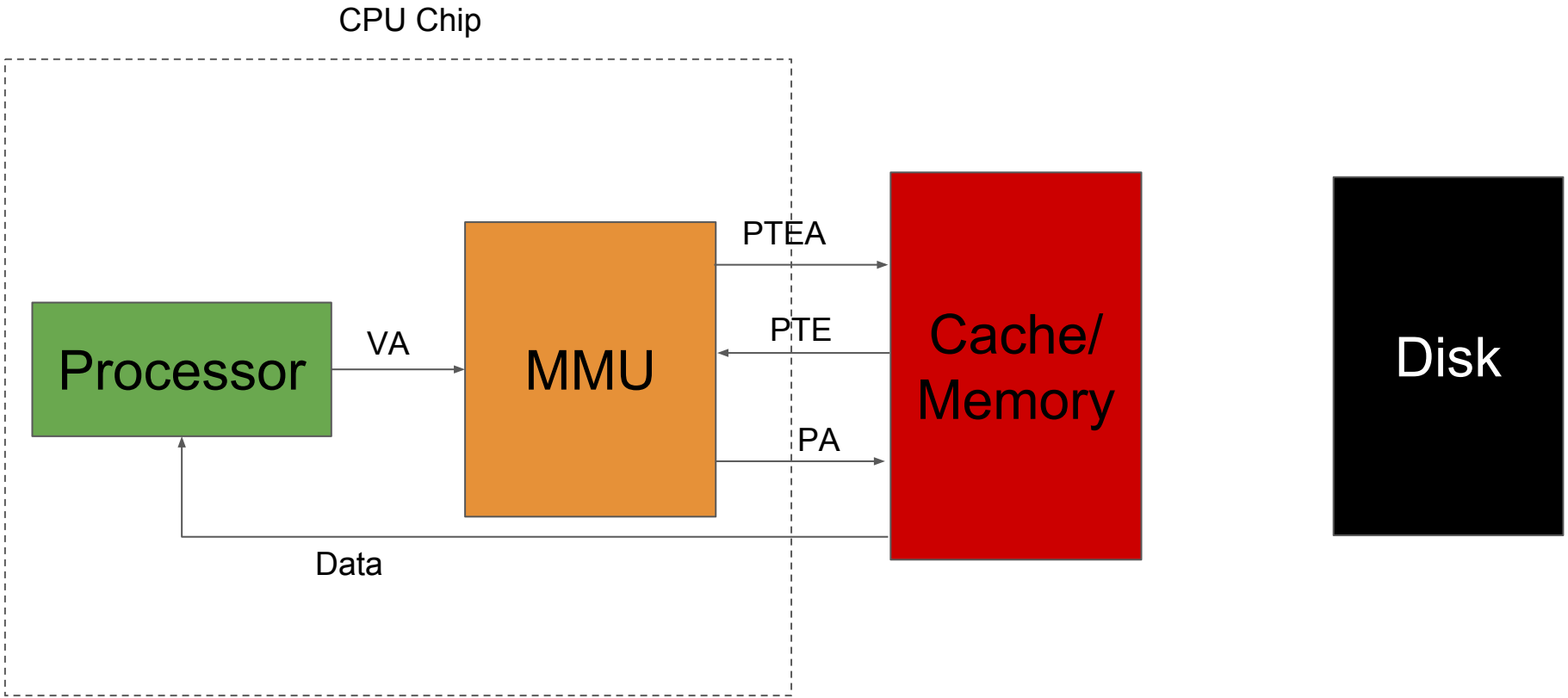


Page Table Base Register (PTBR) is a CPU register that stores the address of the Page Table!

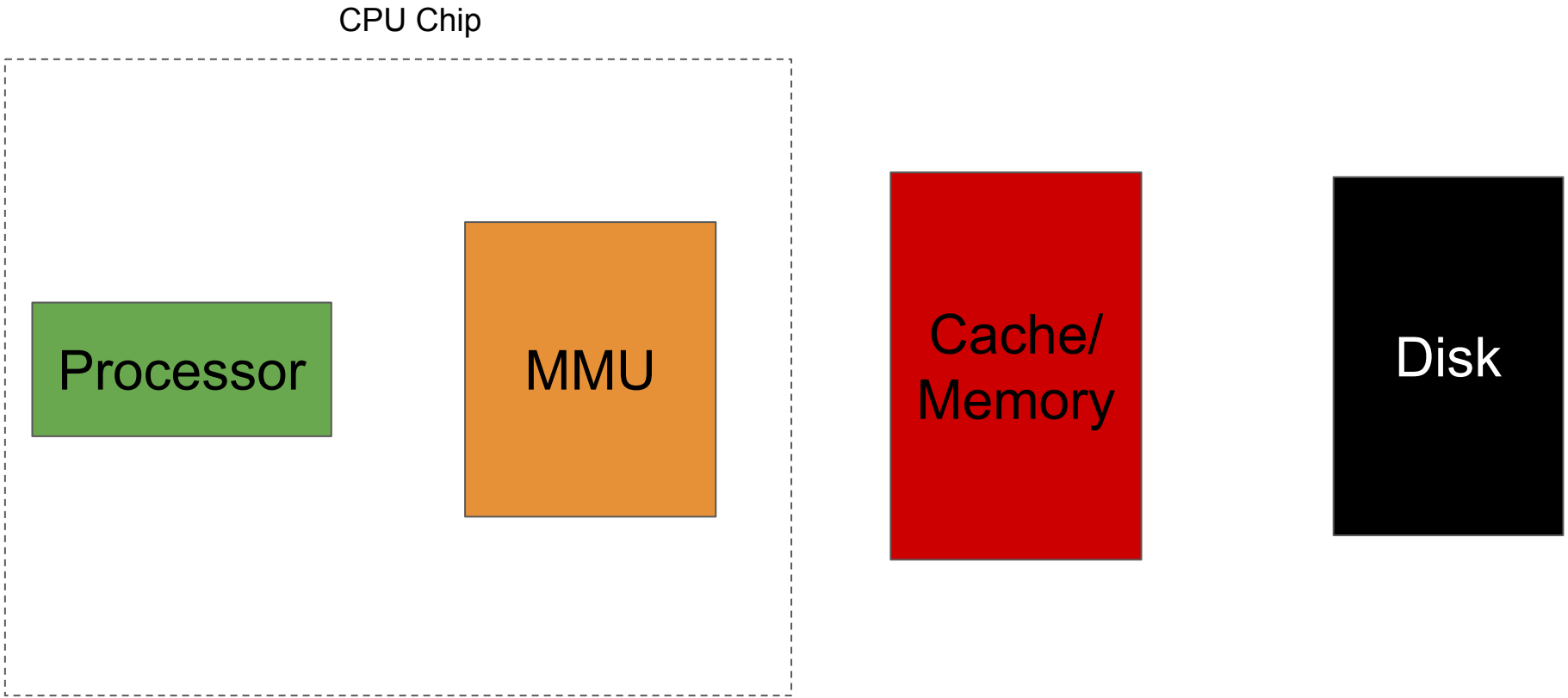

CPU Chip
Processor
VA
MMU
PTEA
Cache/
Memory
Disk

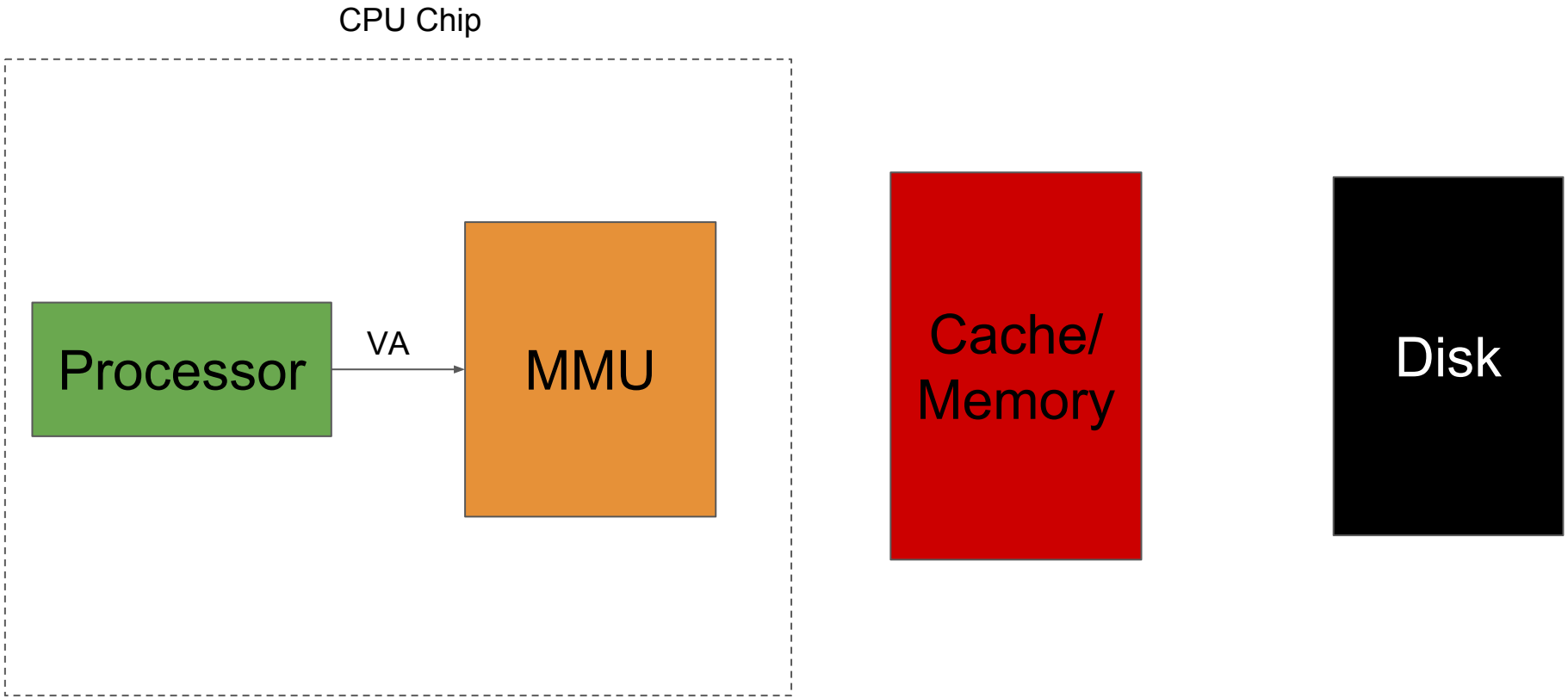

CPU Chip
Processor
VA
MMU
PTEA
PTE
Cache/
Memory
Disk

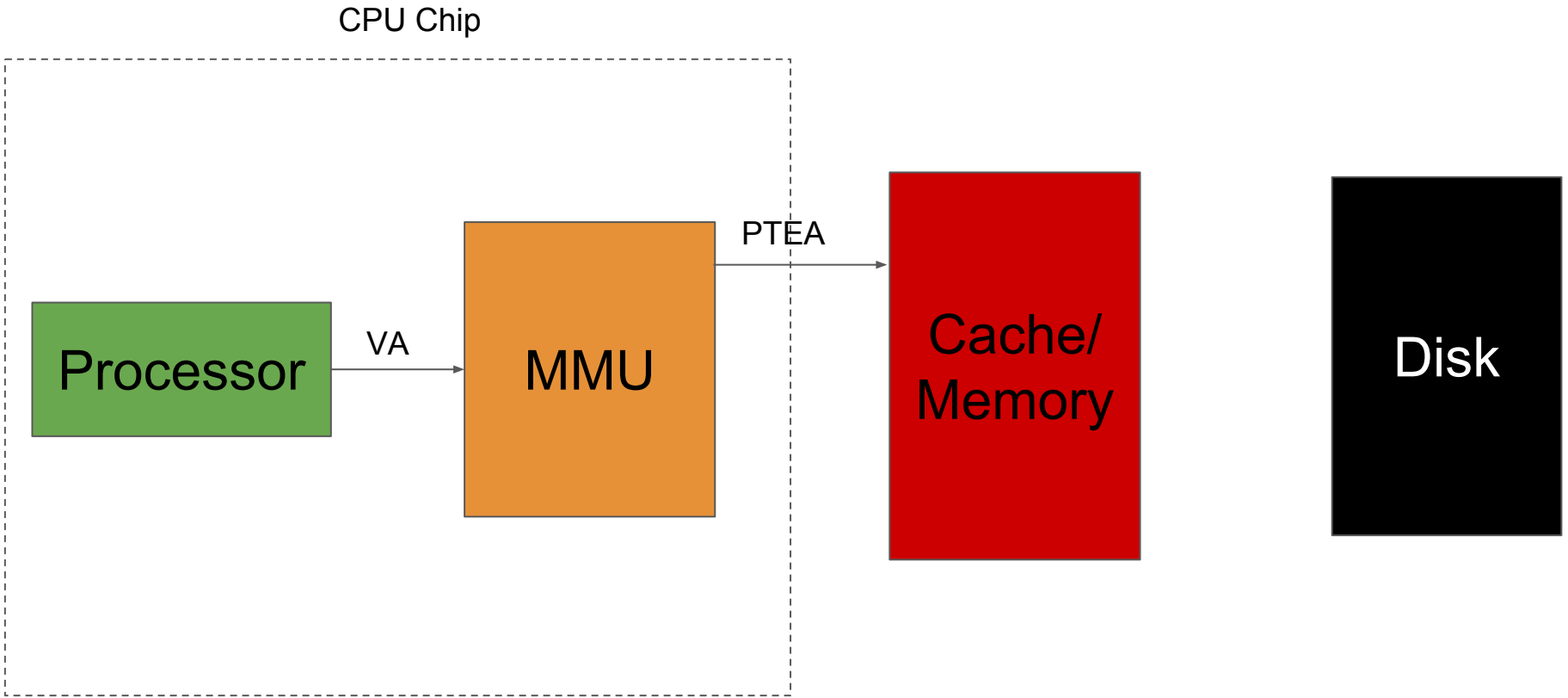

CPU Chip
Processor
VA
MMU
PTEA
PTE
PA
Cache/
Memory
Disk

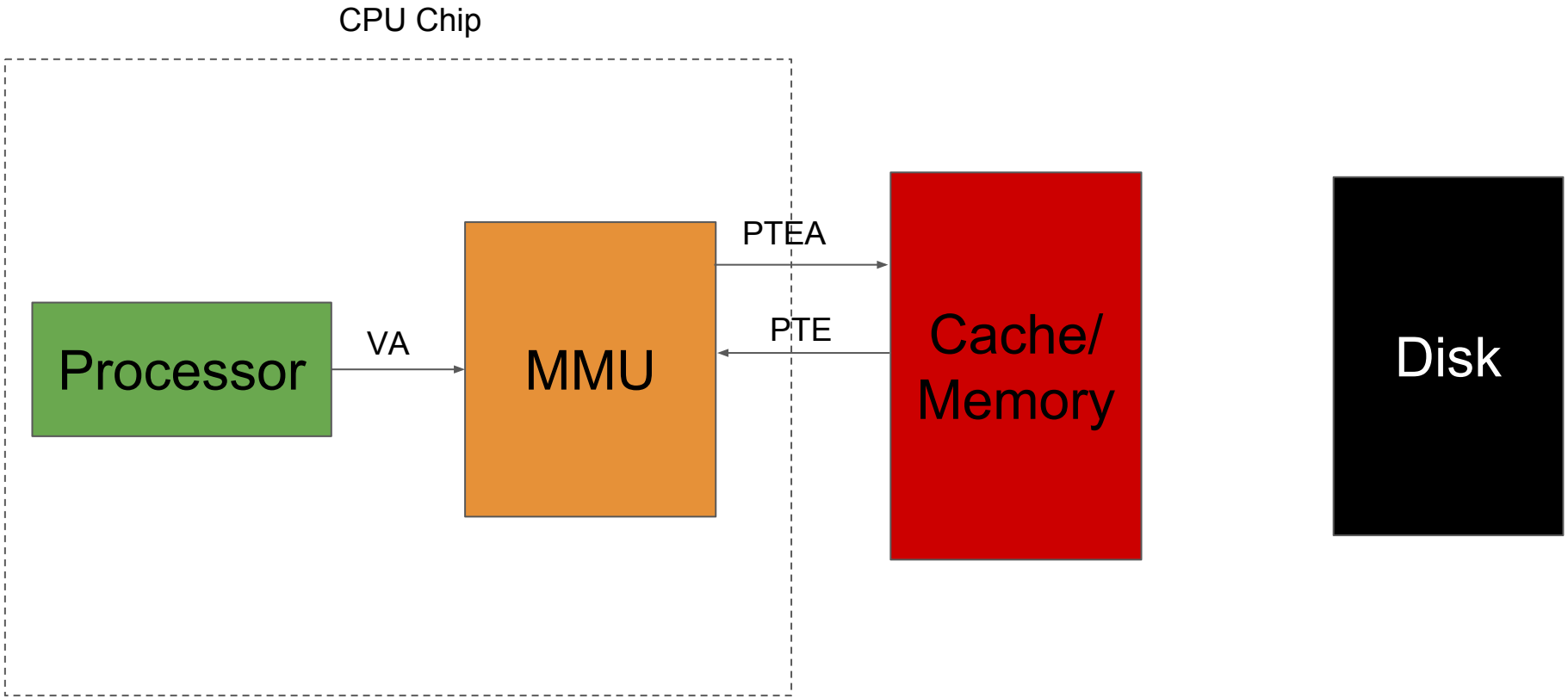

CPU Chip
Processor
VA
MMU
PTEA
PTE
PA
Cache/
Memory
Data
Disk

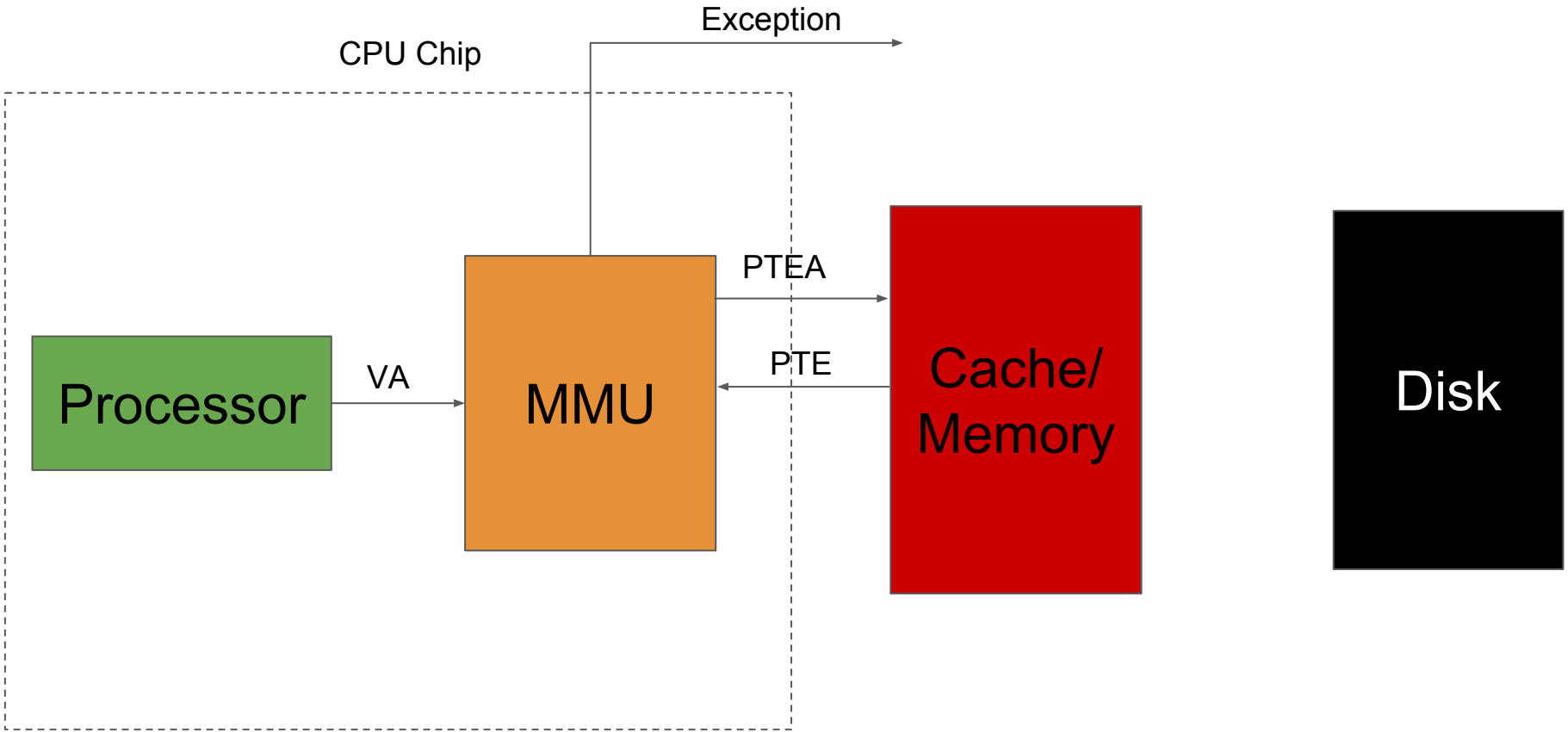
Steps in Page Fault

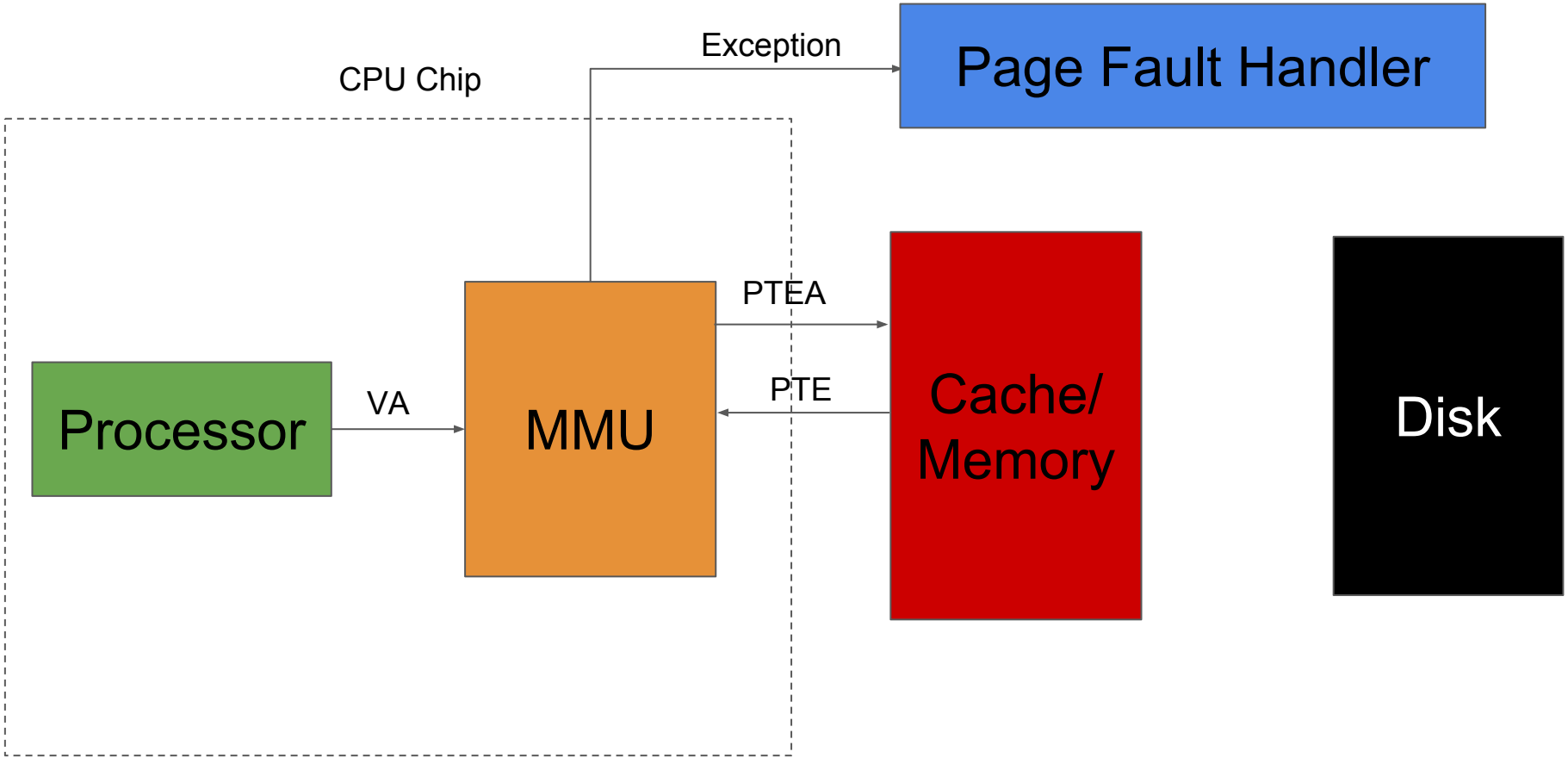

CPU Chip
Processor
MMU
Cache/
Memory
Disk

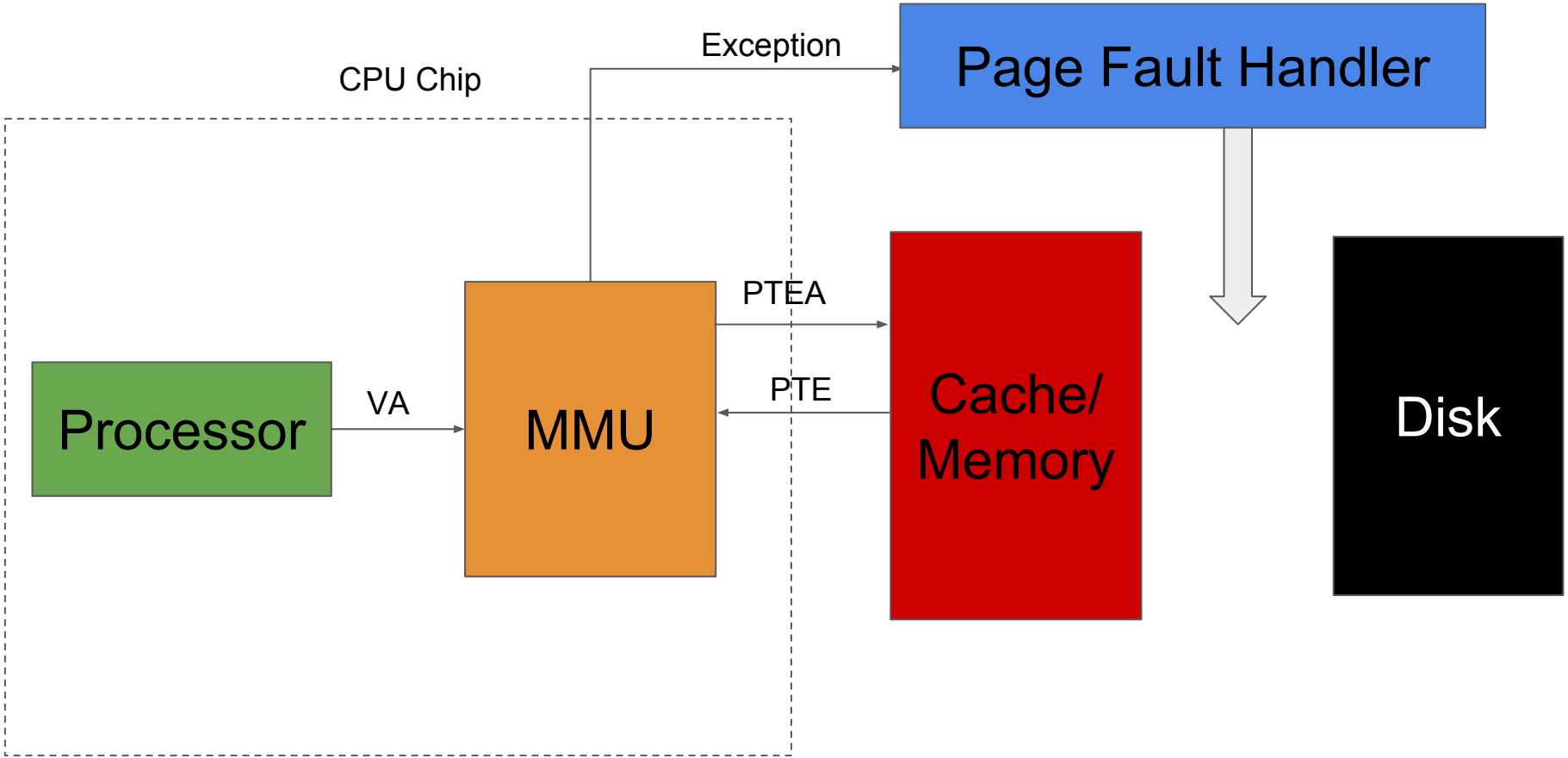

CPU Chip
Processor
VA
MMU
Cache/
Memory
Disk

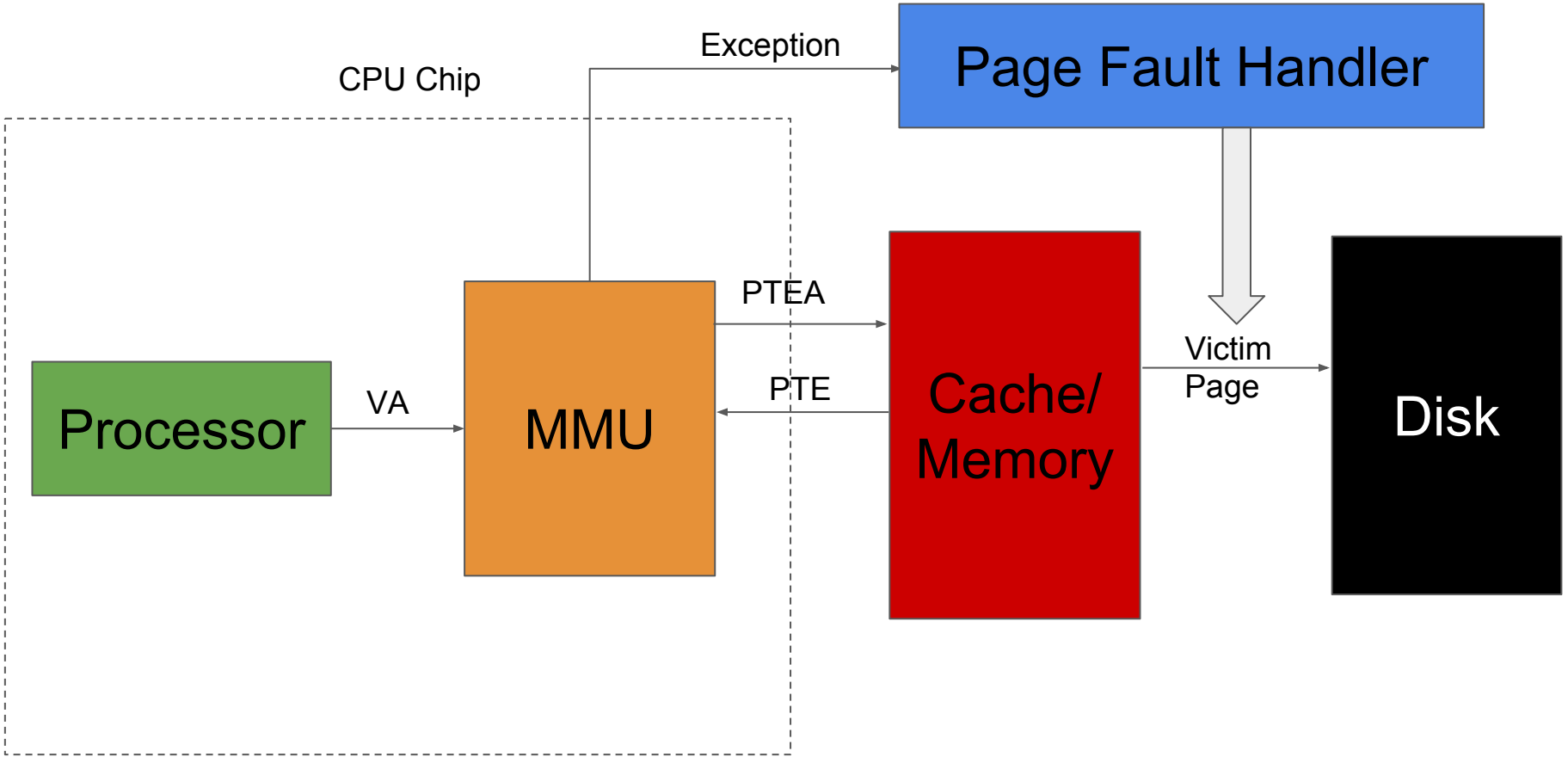

CPU Chip
Processor
VA
MMU
PTEA
Cache/
Memory
Disk

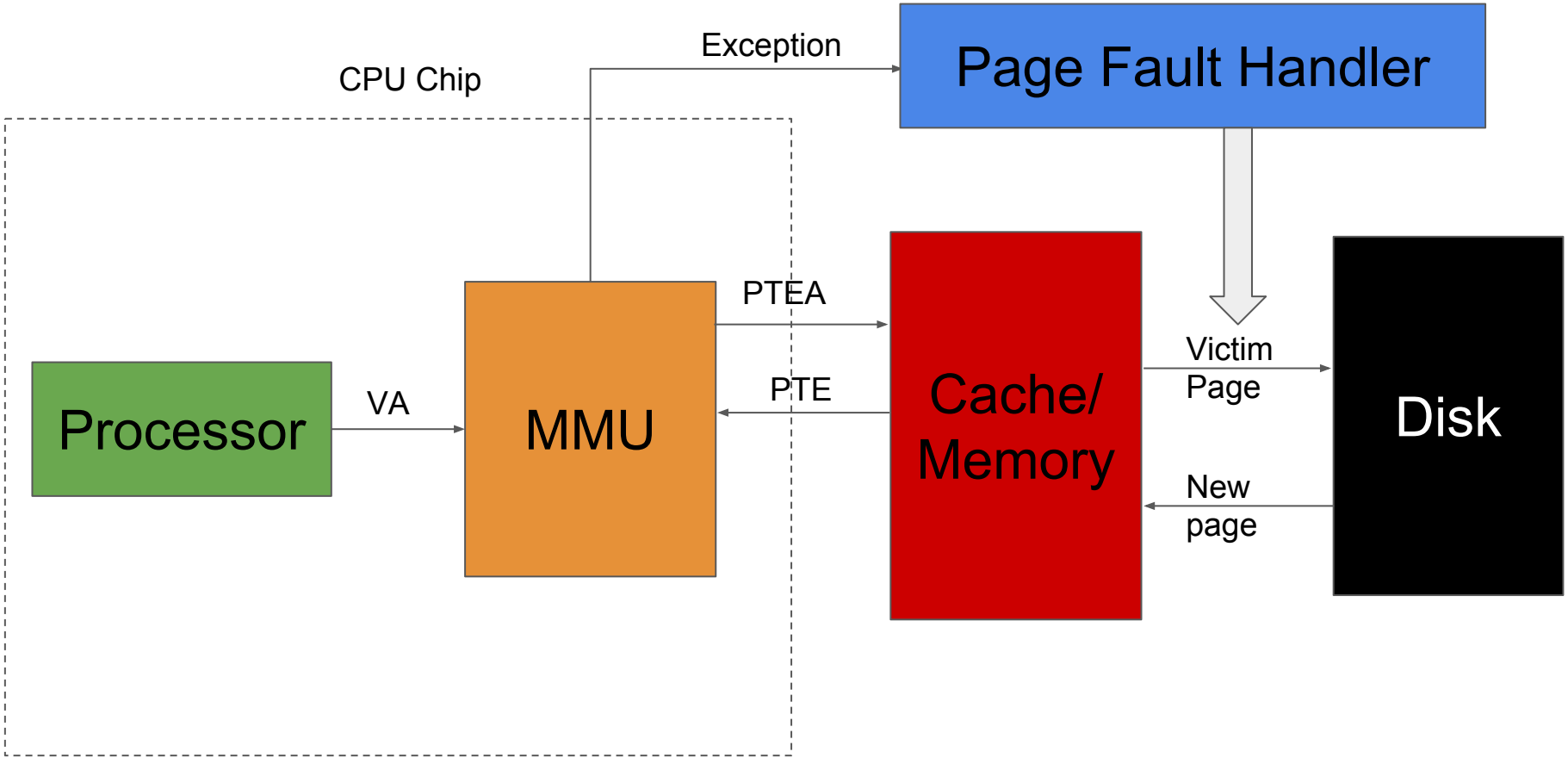

CPU Chip
Processor
VA
MMU
PTEA
PTE
Cache/
Memory
Disk

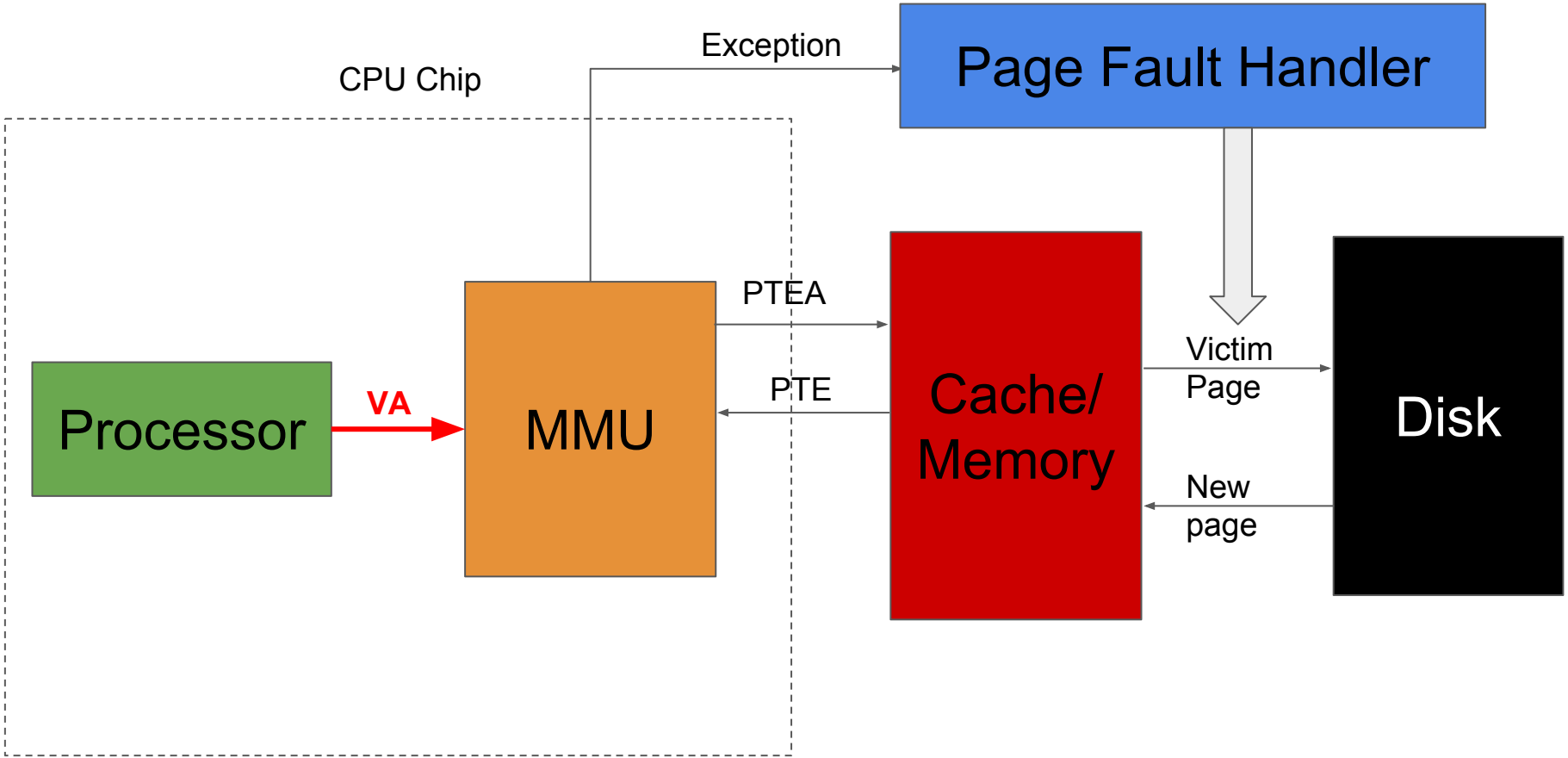

Exception
CPU Chip
PTEA
PTE
VA
Processor
MMU
Cache/
Memory
Disk

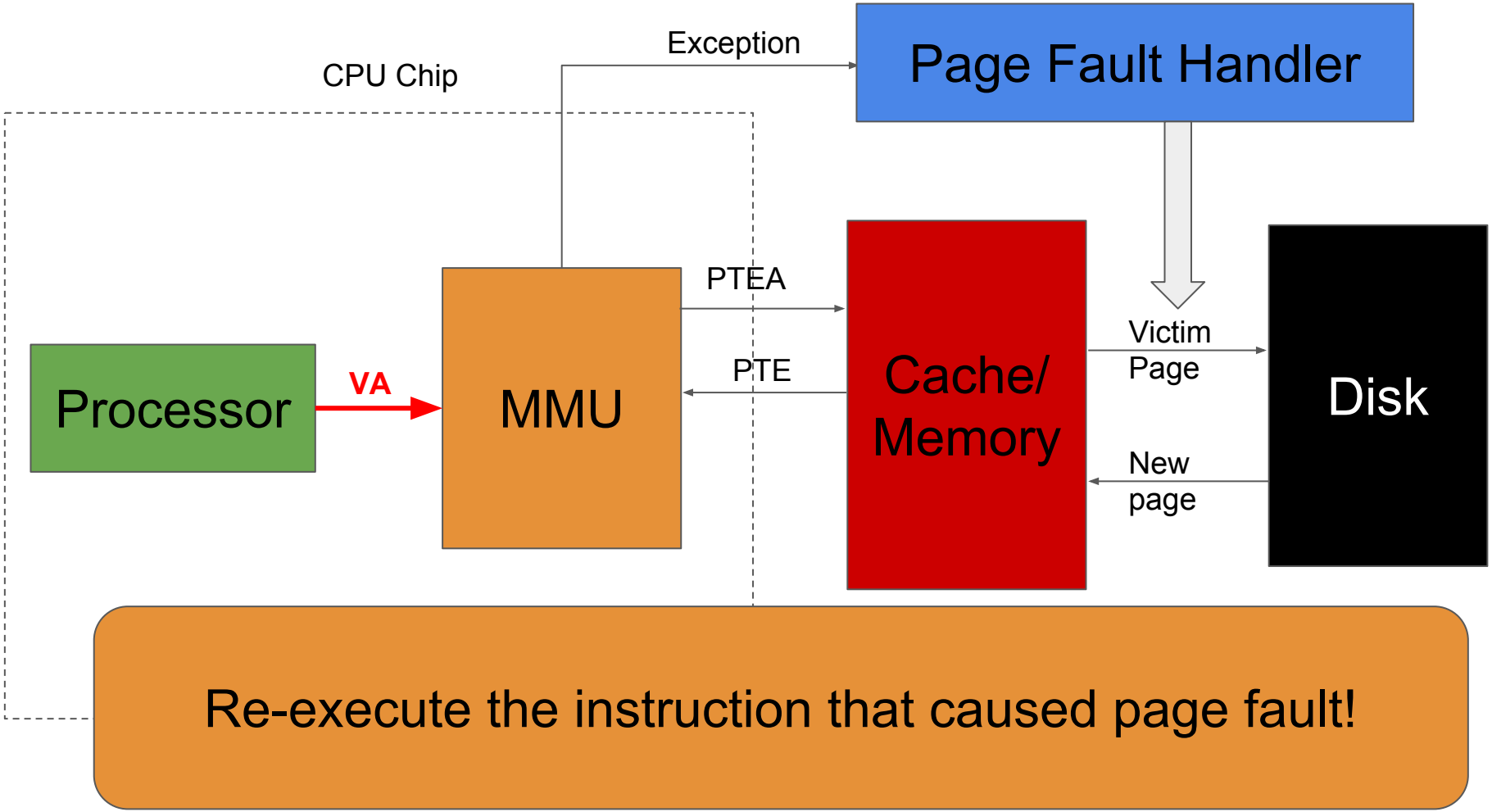

Exception
Page Fault Handler
CPU Chip
PTEA
PTE
Processor
VA
MMU
Cache/
Memory
Disk


Exception
Page Fault Handler
CPU Chip
PTEA
PTE
Processor
VA
MMU
Cache/
Memory
Disk


Exception
Page Fault Handler
CPU Chip
PTEA
Processor
VA
MMU
PTE
Cache/
Memory
Victim
Page
Disk


Exception
Page Fault Handler
CPU Chip
PTEA
Processor
VA
MMU
PTE
Cache/
Memory
Victim
Page
Disk
New
page


Exception
Page Fault Handler
CPU Chip
PTEA
PTE
Processor
VA
MMU
Cache/
Memory
Victim
Page
New
page
Disk

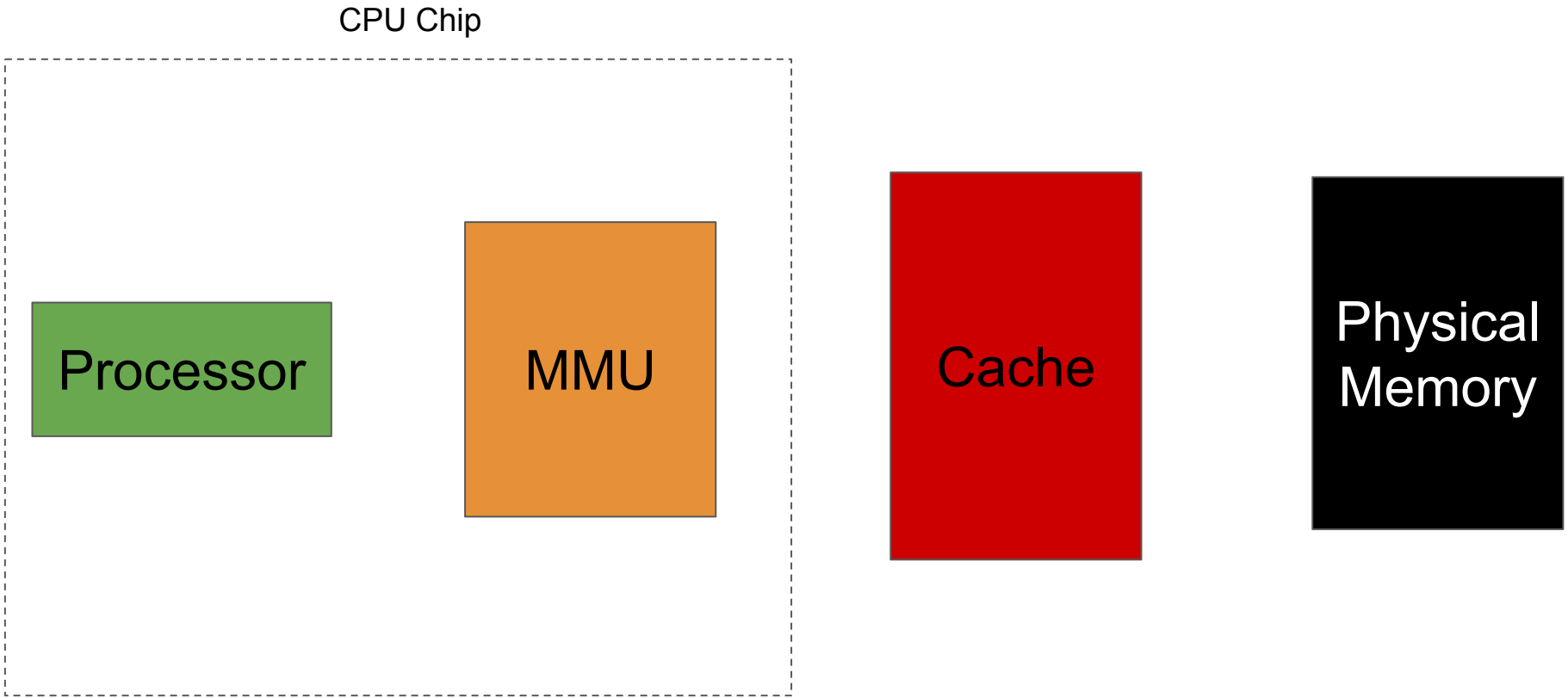

Exception
Page Fault Handler
CPU Chip
PTEA
PTE
Processor
VA
MMU
Cache/
Memory
Victim
Page
New
page
Disk
Re-execute the instruction that caused page fault!

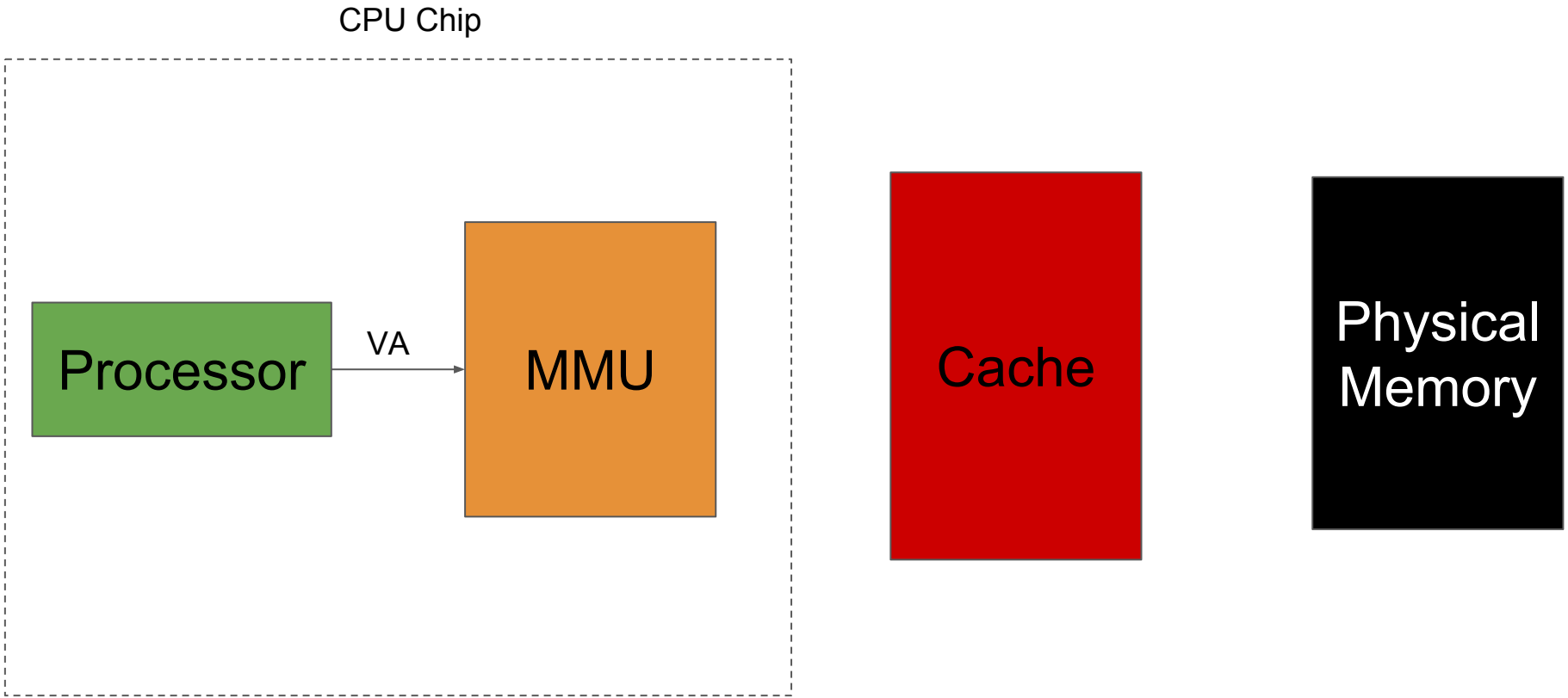
VM with Caches

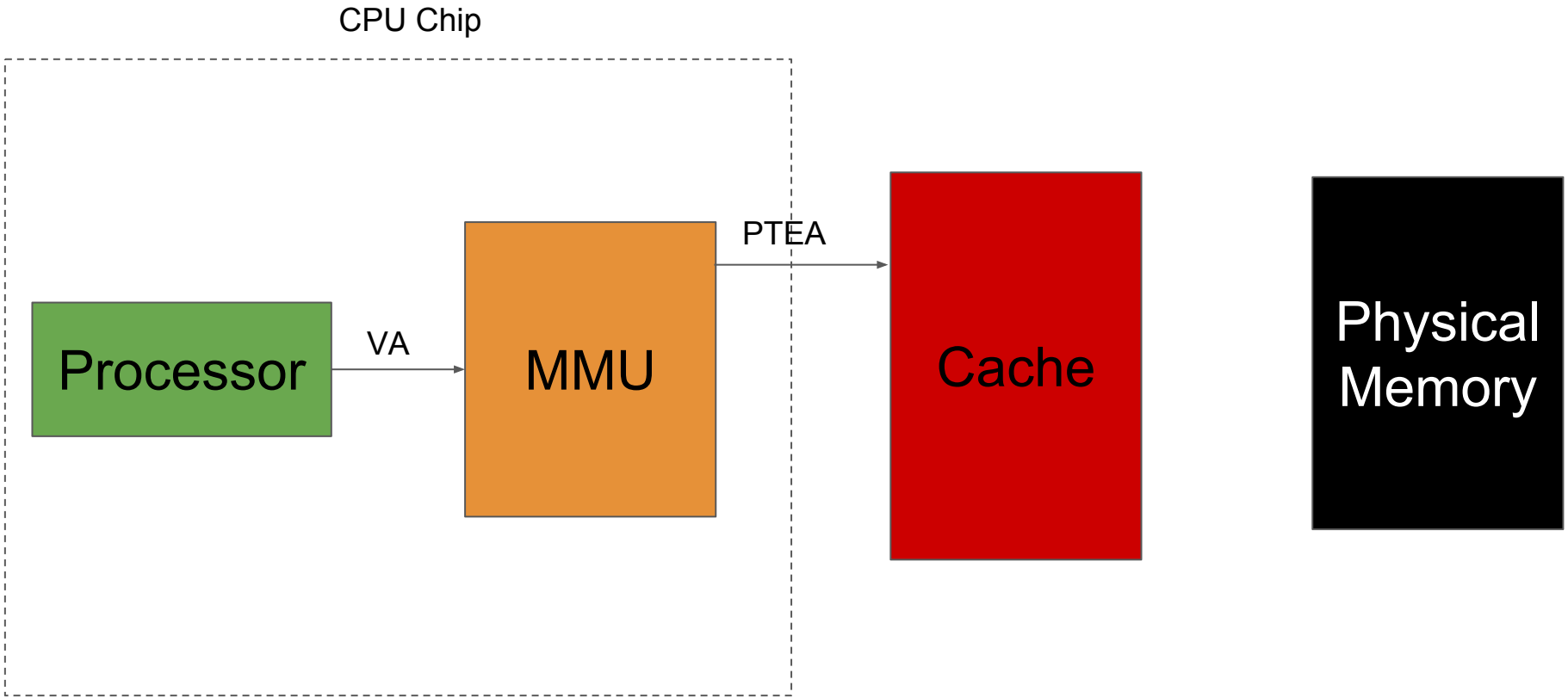
Scenario #1

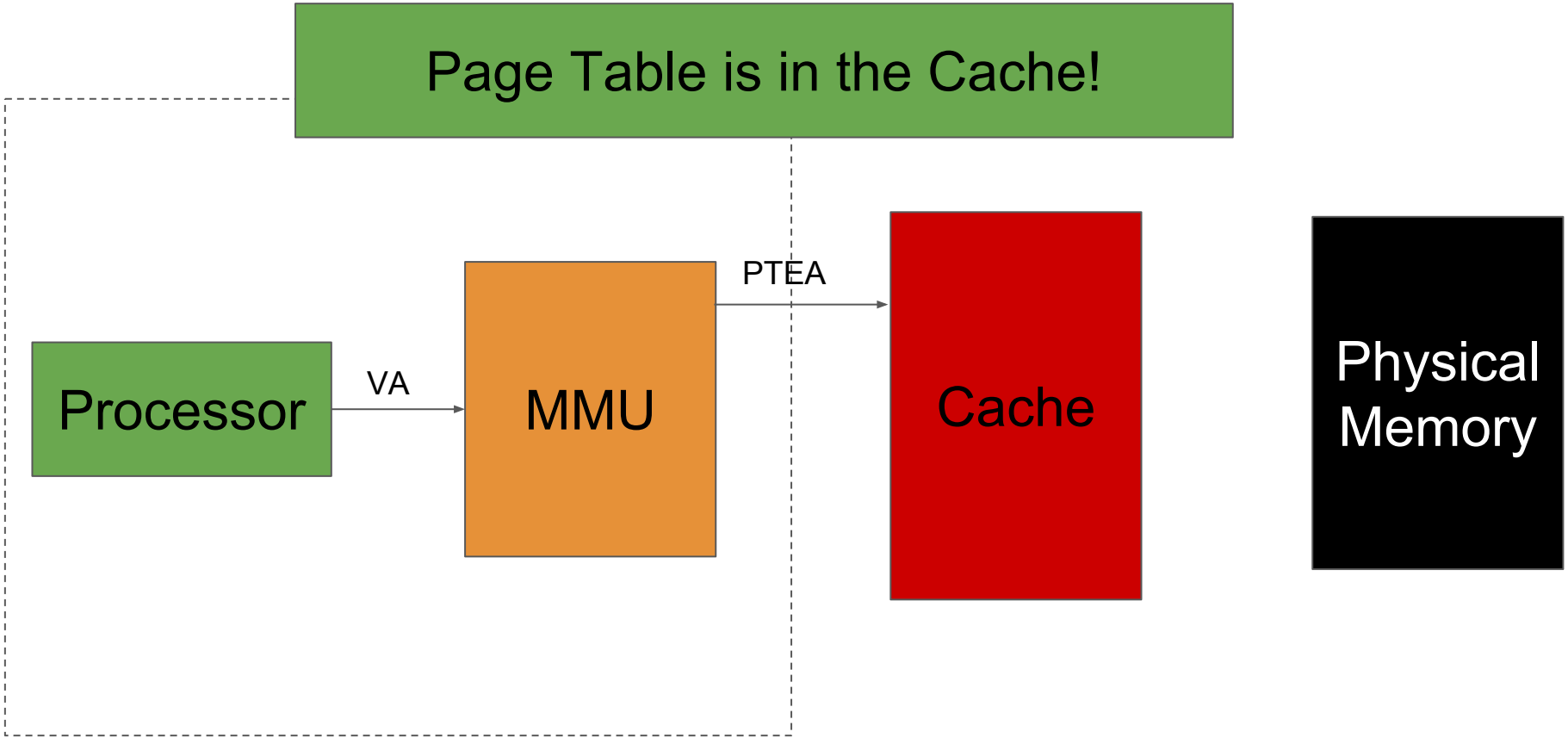
Page Table is in the Cache

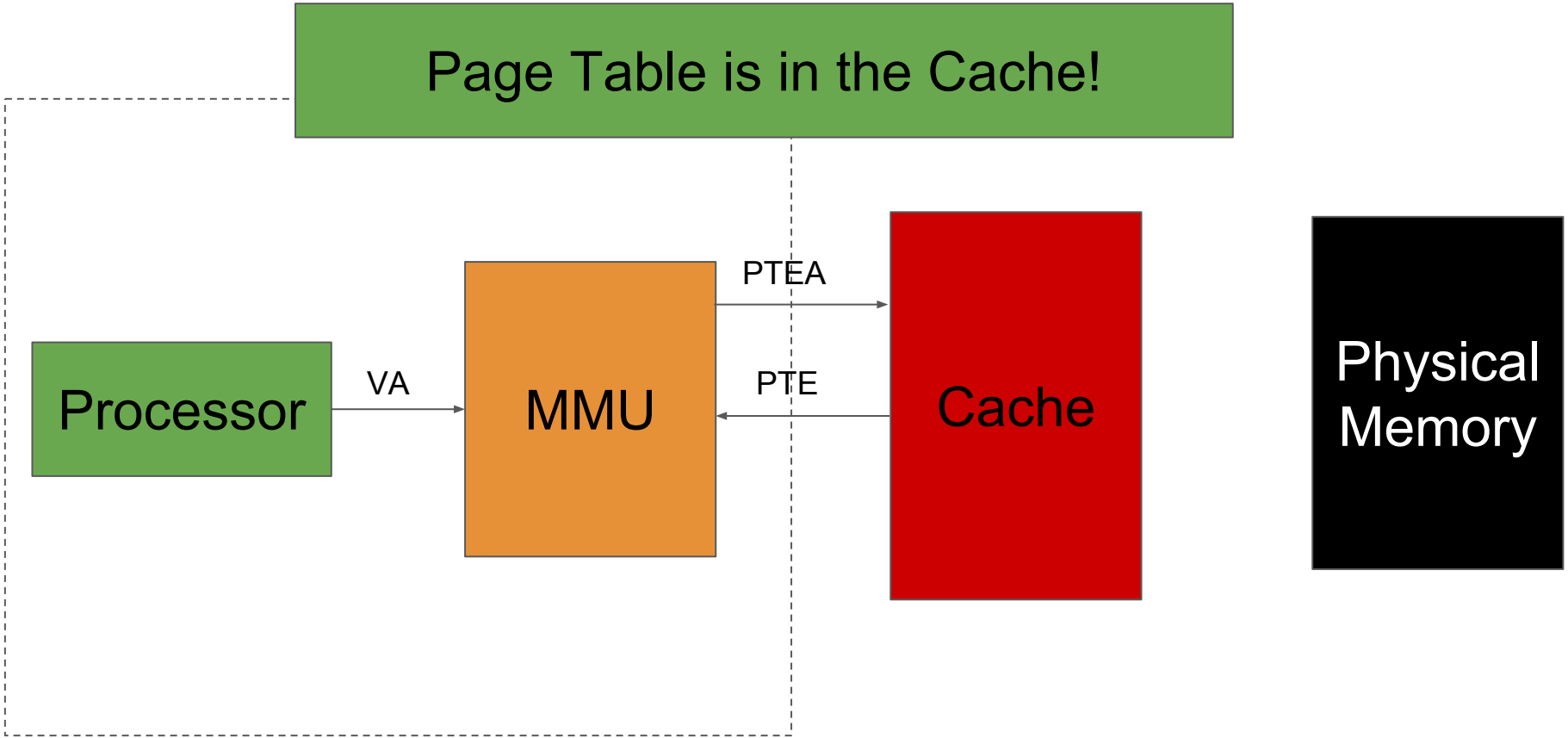
Physical Address is in the Cache

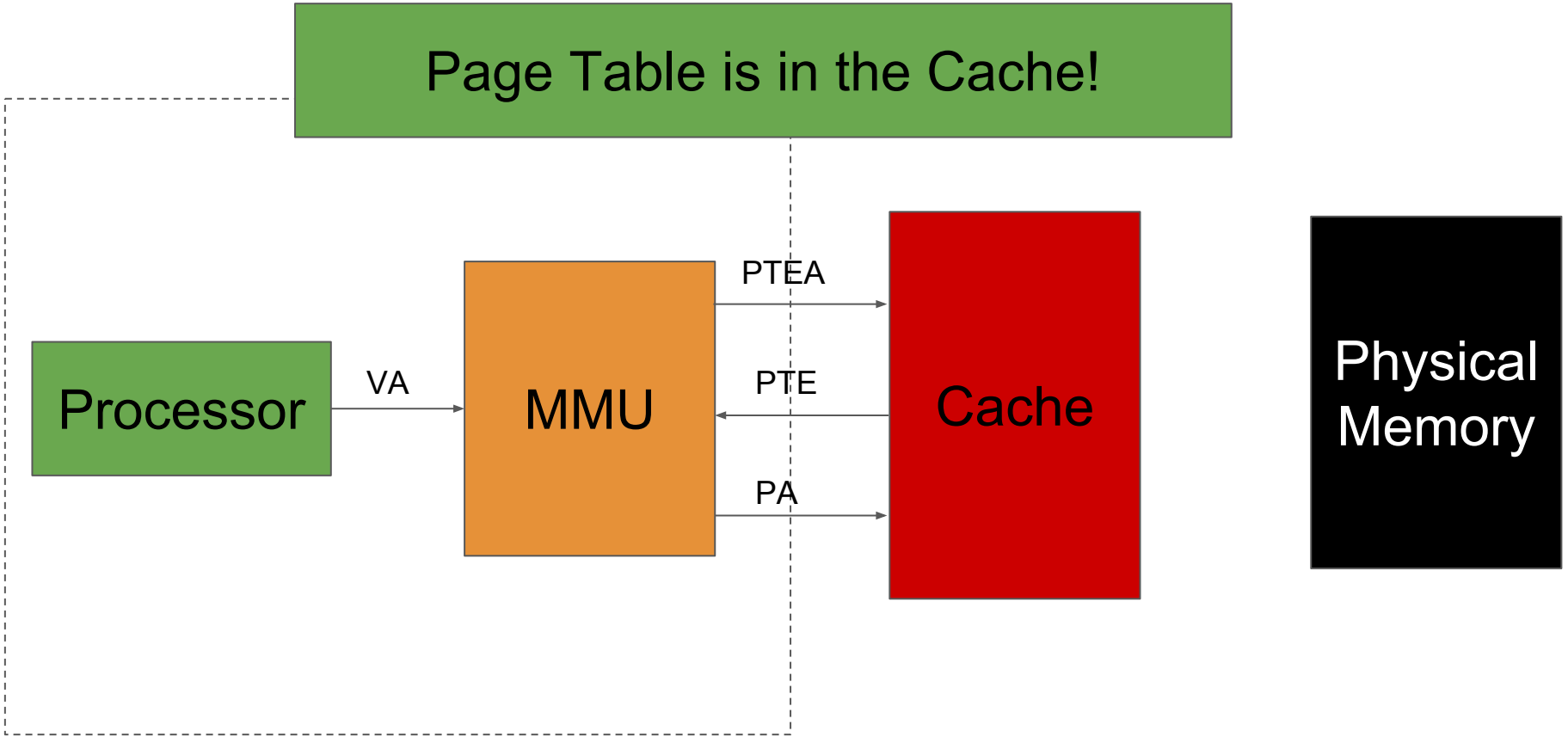

CPU Chip
Processor
MMU
Cache
Physical Memory

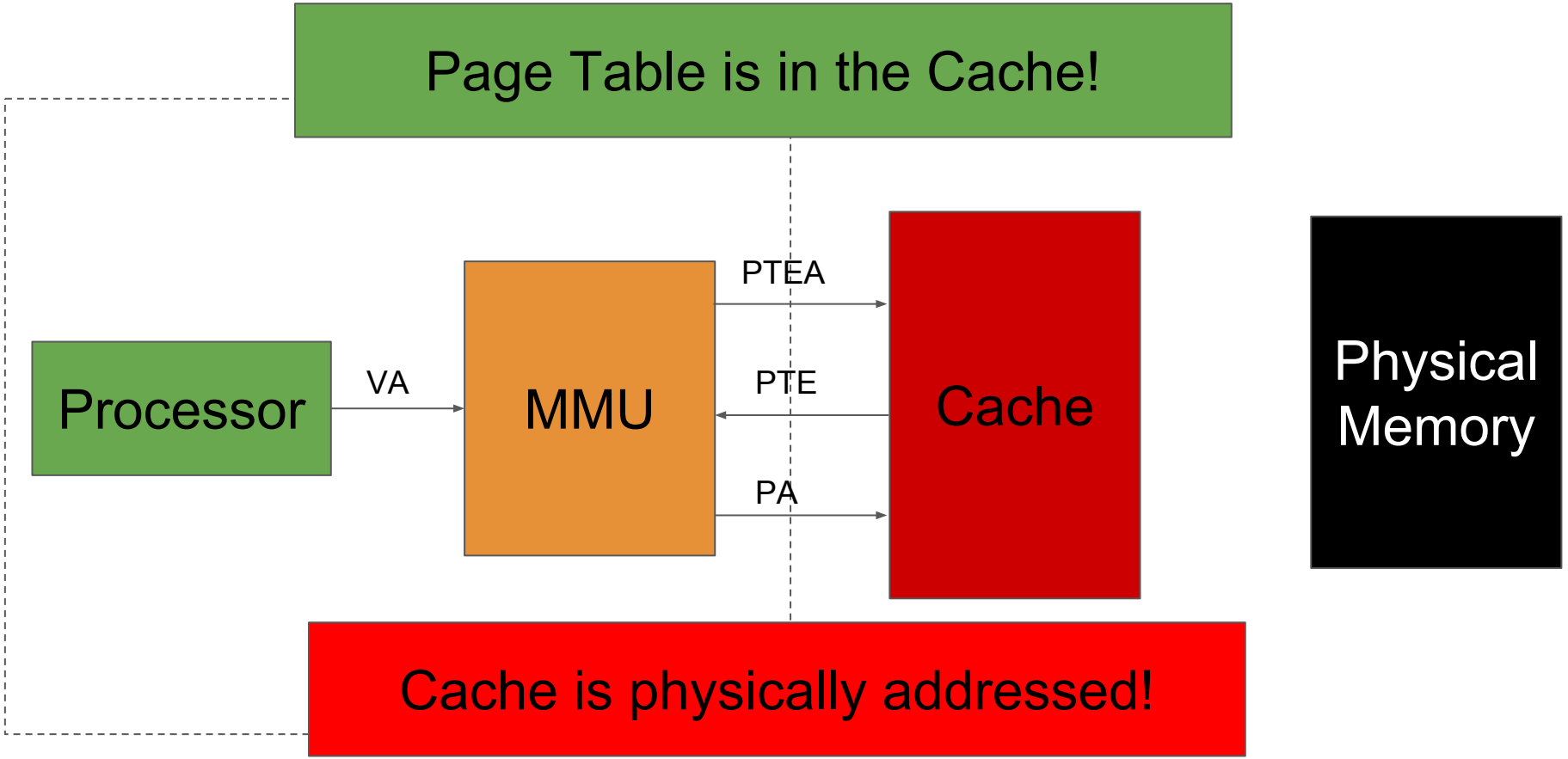

CPU Chip
Processor
VA
MMU
Cache
Physical Memory

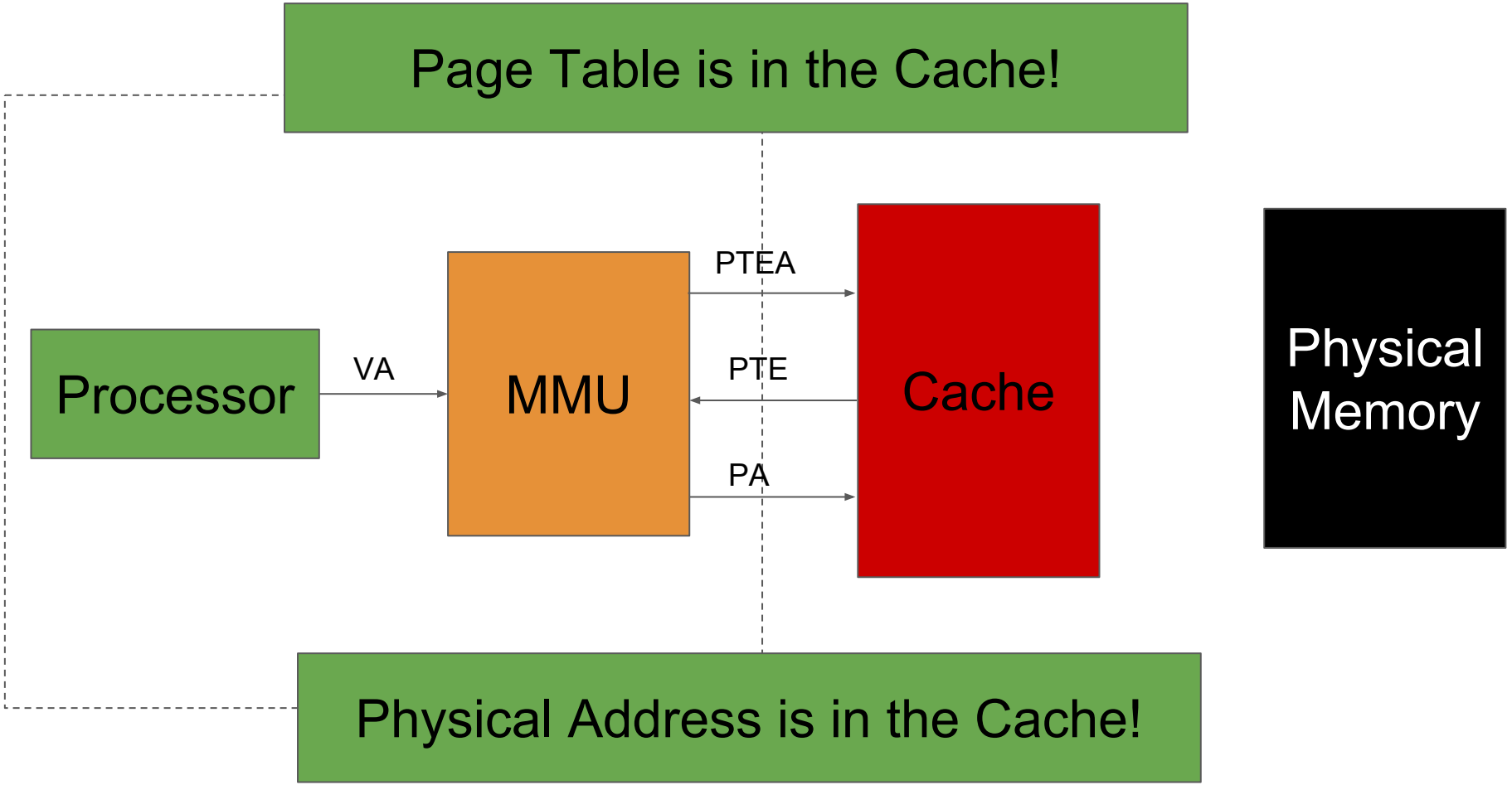

CPU Chip
Processor
VA
MMU
PTEA
Cache
Physical Memory

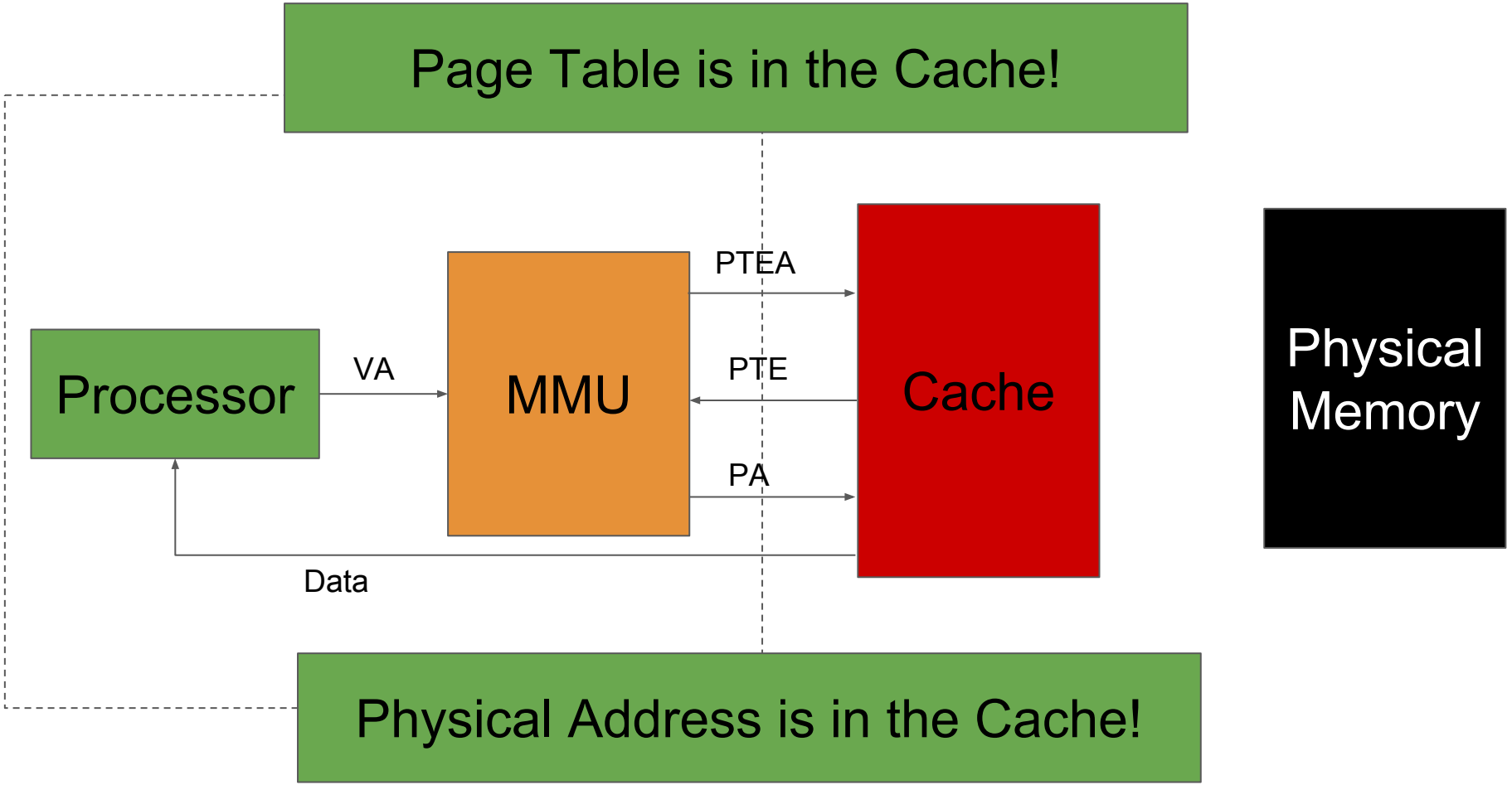

Page Table is in the Cache!
Processor
VA
MMU
PTEA
Cache
Physical Memory


Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
Cache
Physical Memory


Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
Physical Memory


Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
Physical Memory
Cache is physically addressed!

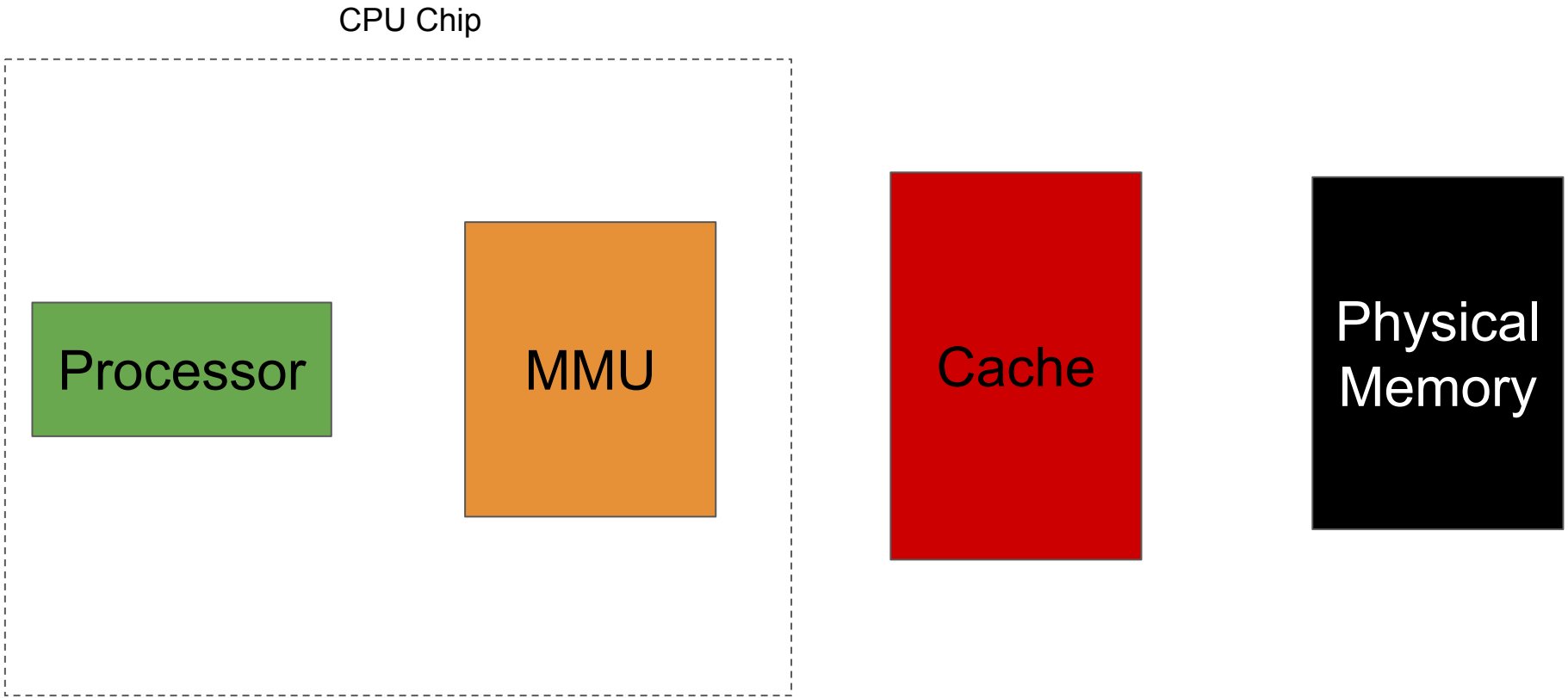

Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
Physical Memory
Physical Address is in the Cache!

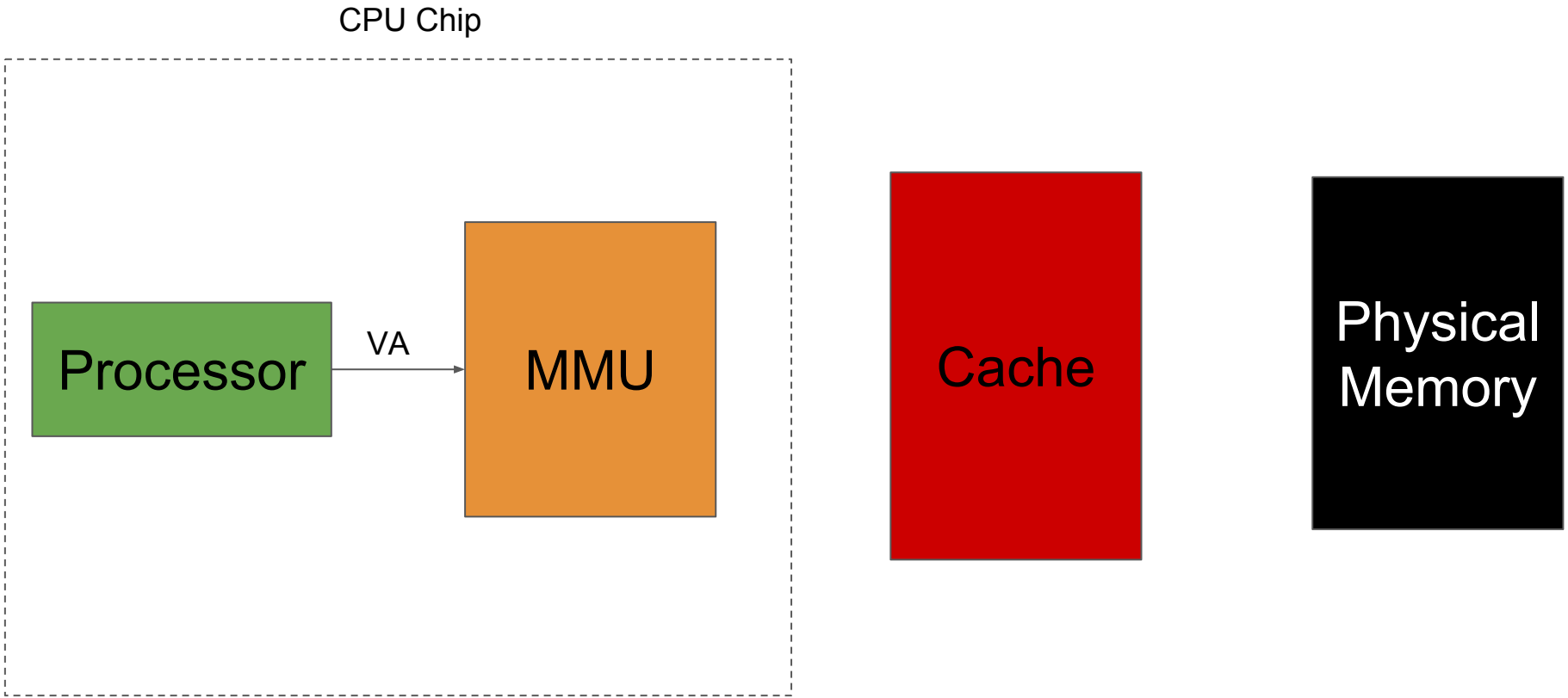

Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
Data
Physical Memory
Physical Address is in the Cache!

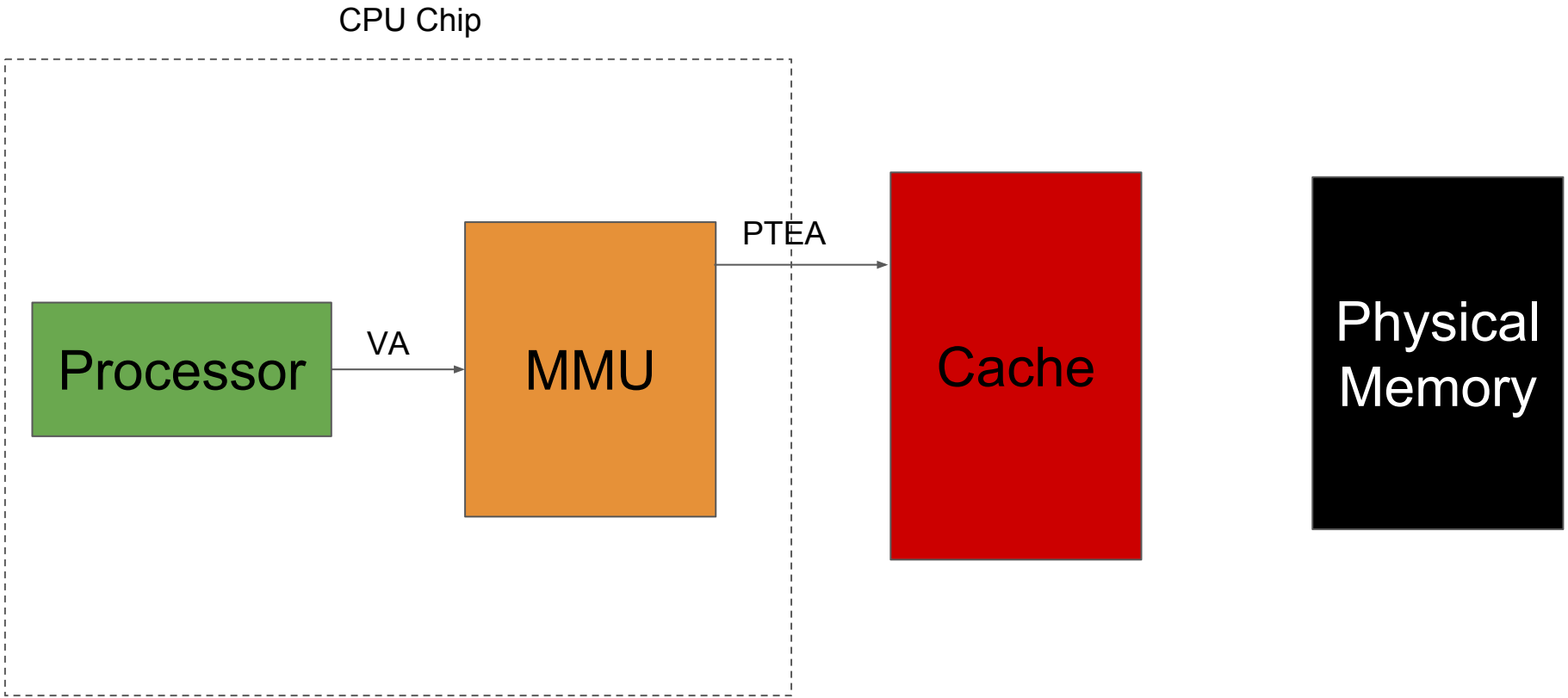
Scenario #2

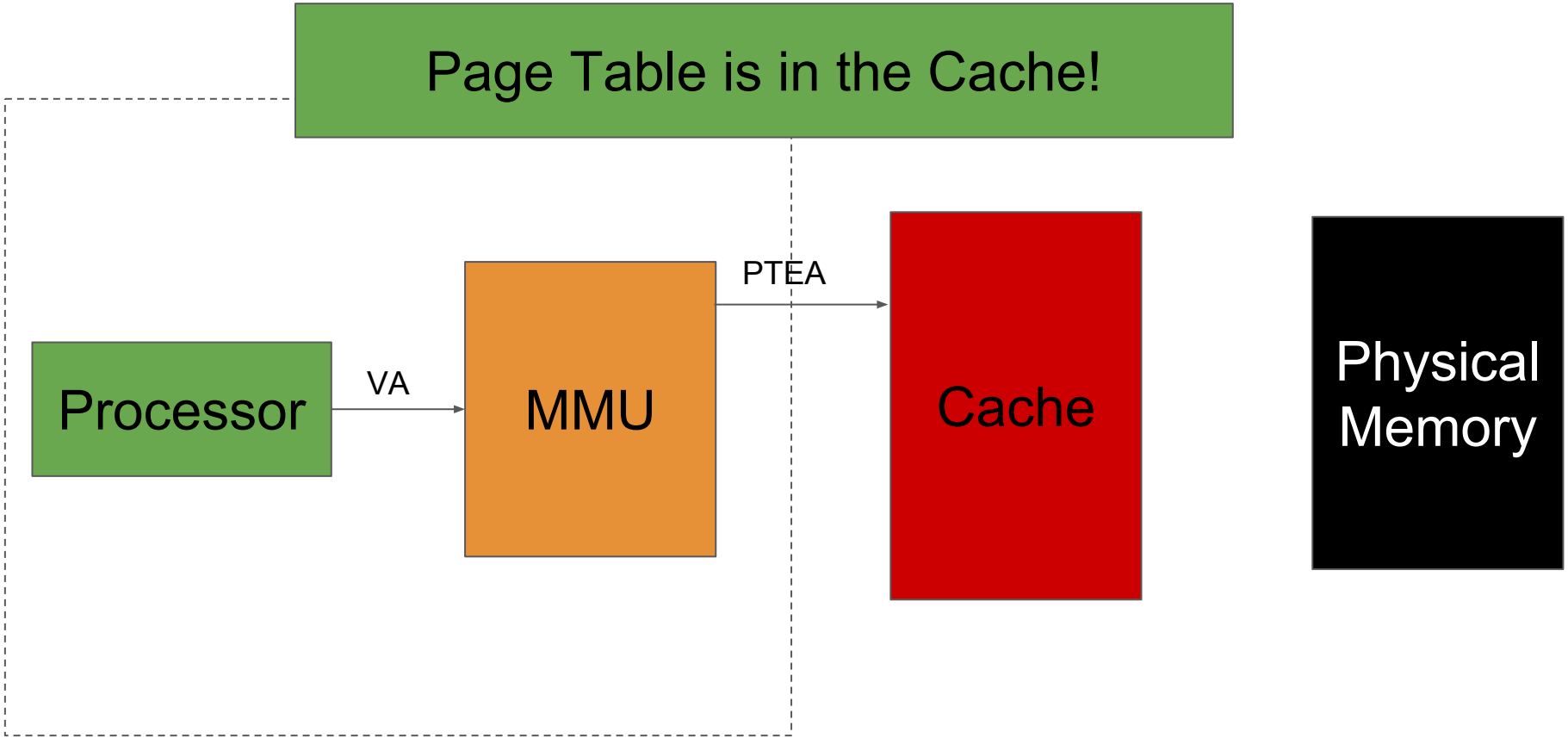
Page Table is in the Cache

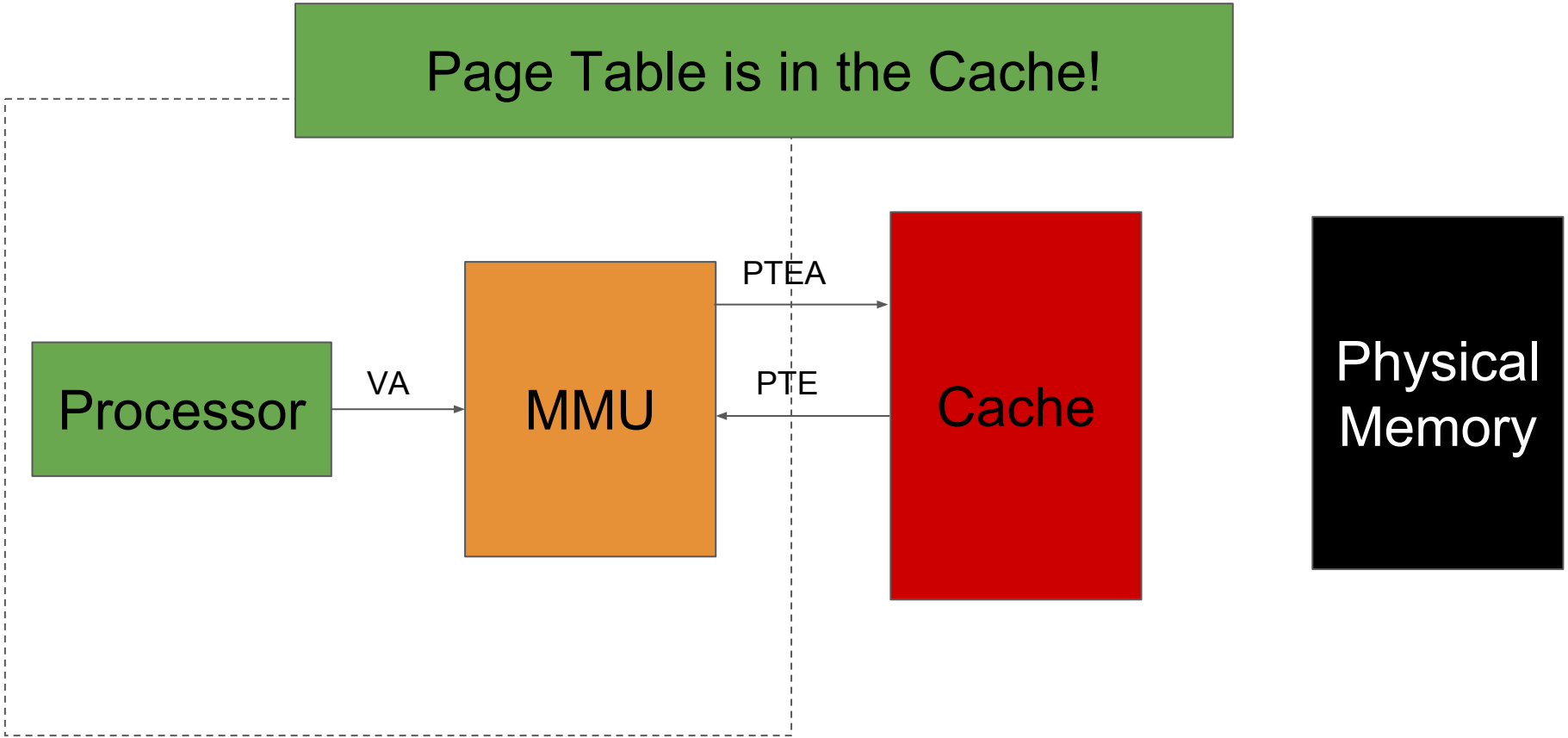
Physical Address is NOT in the Cache

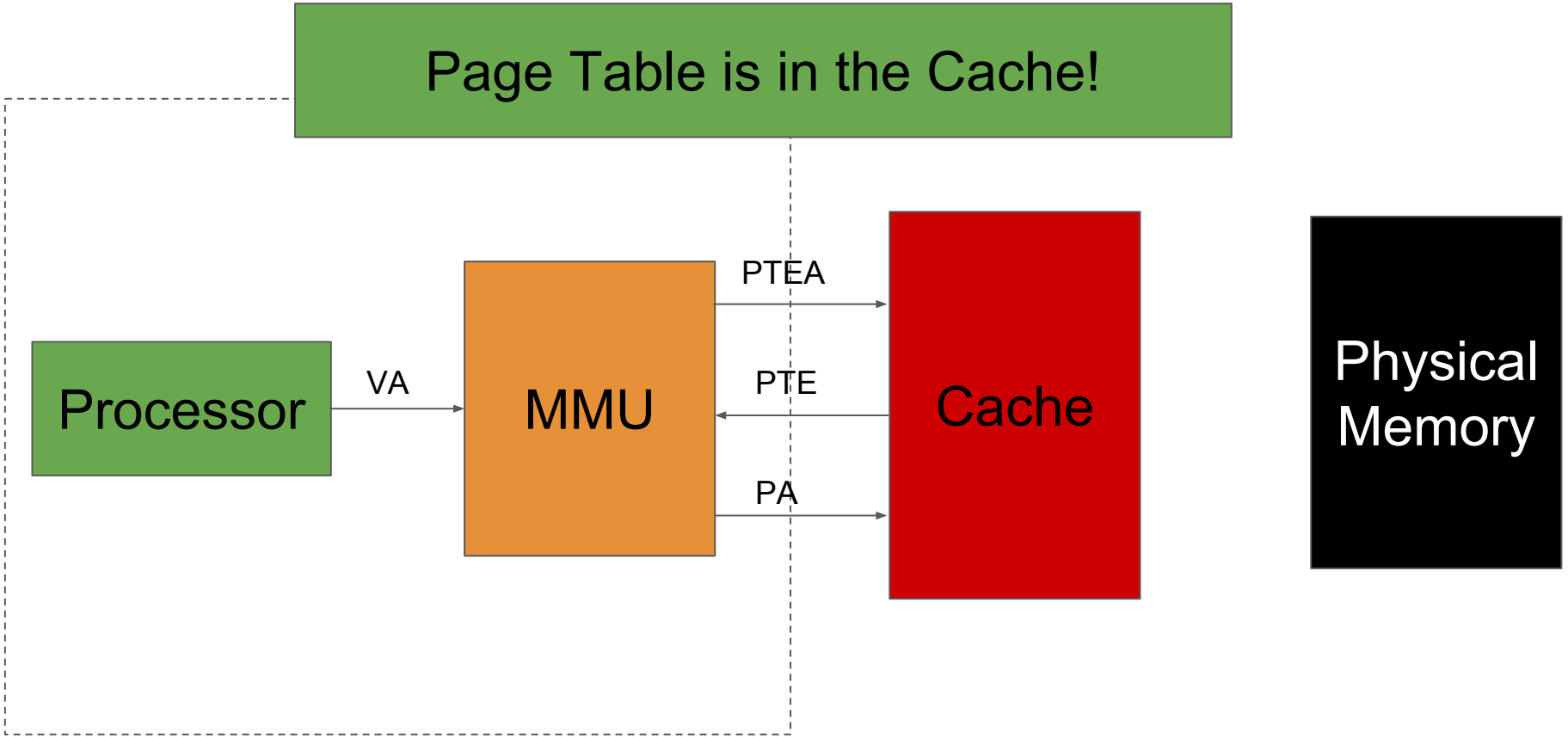

CPU Chip
Processor
MMU
Cache
Physical Memory

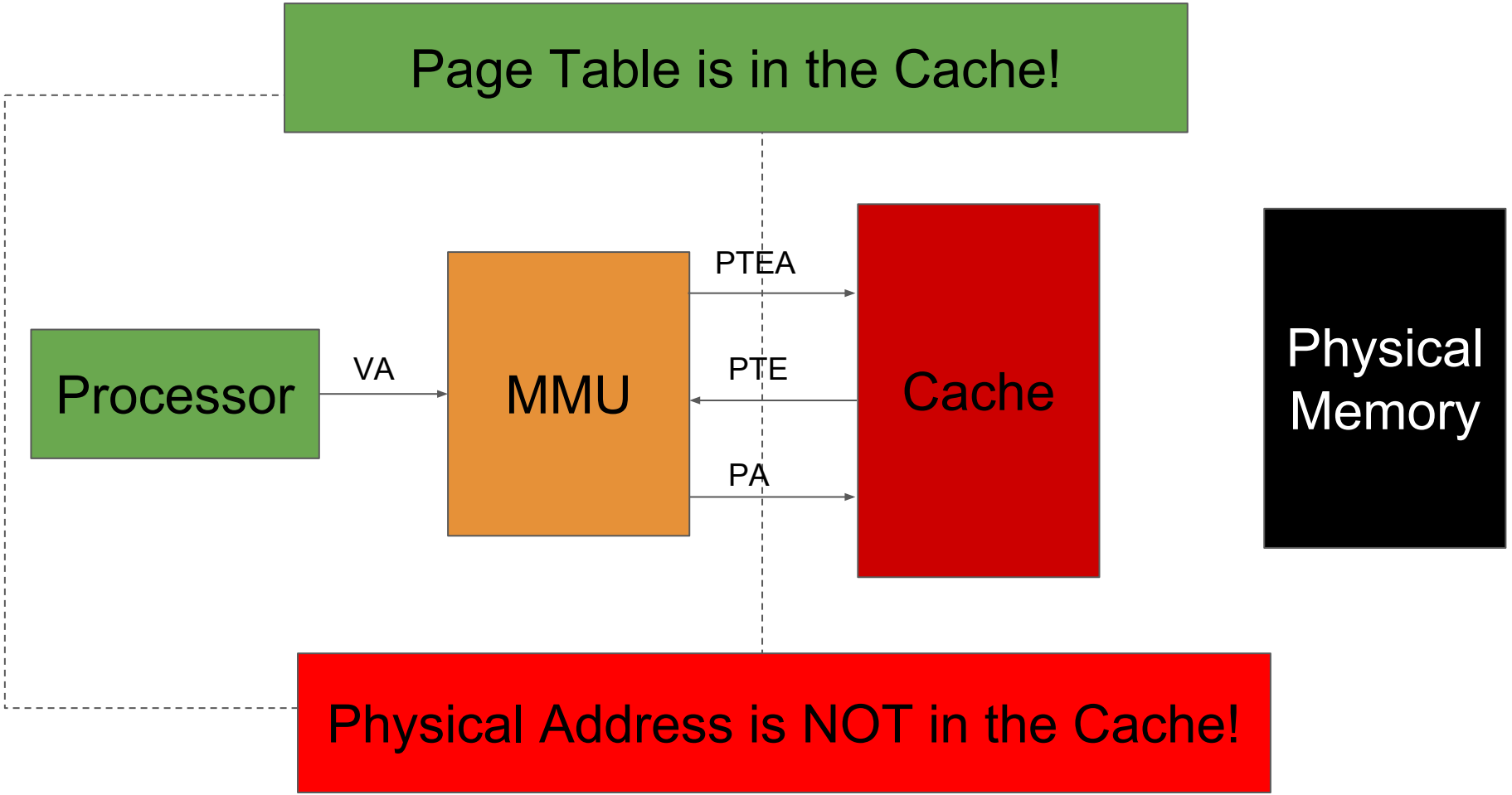

CPU Chip
Processor
VA
MMU
Cache
Physical Memory

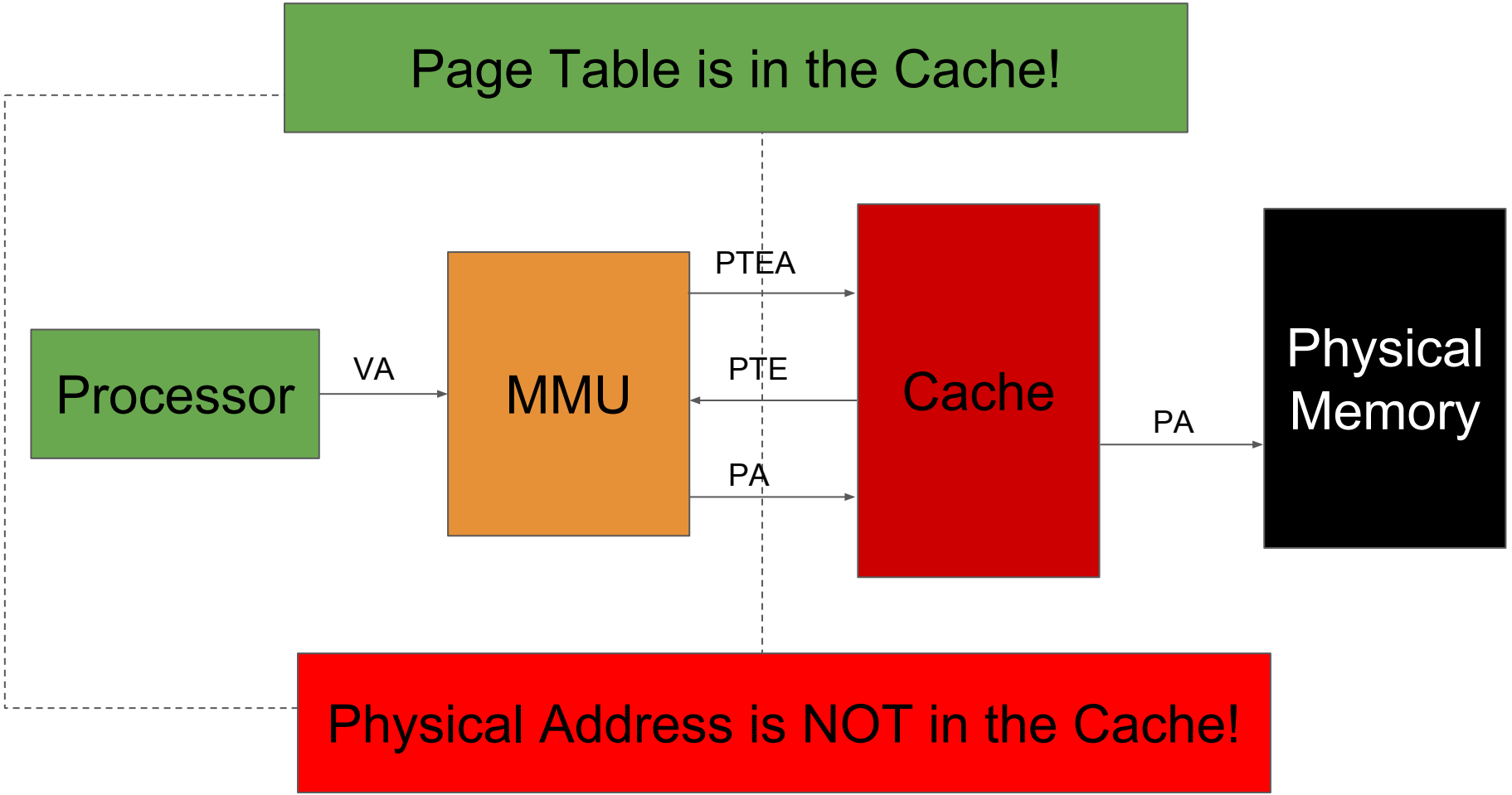

CPU Chip
Processor
VA
MMU
PTEA
Cache
Physical Memory

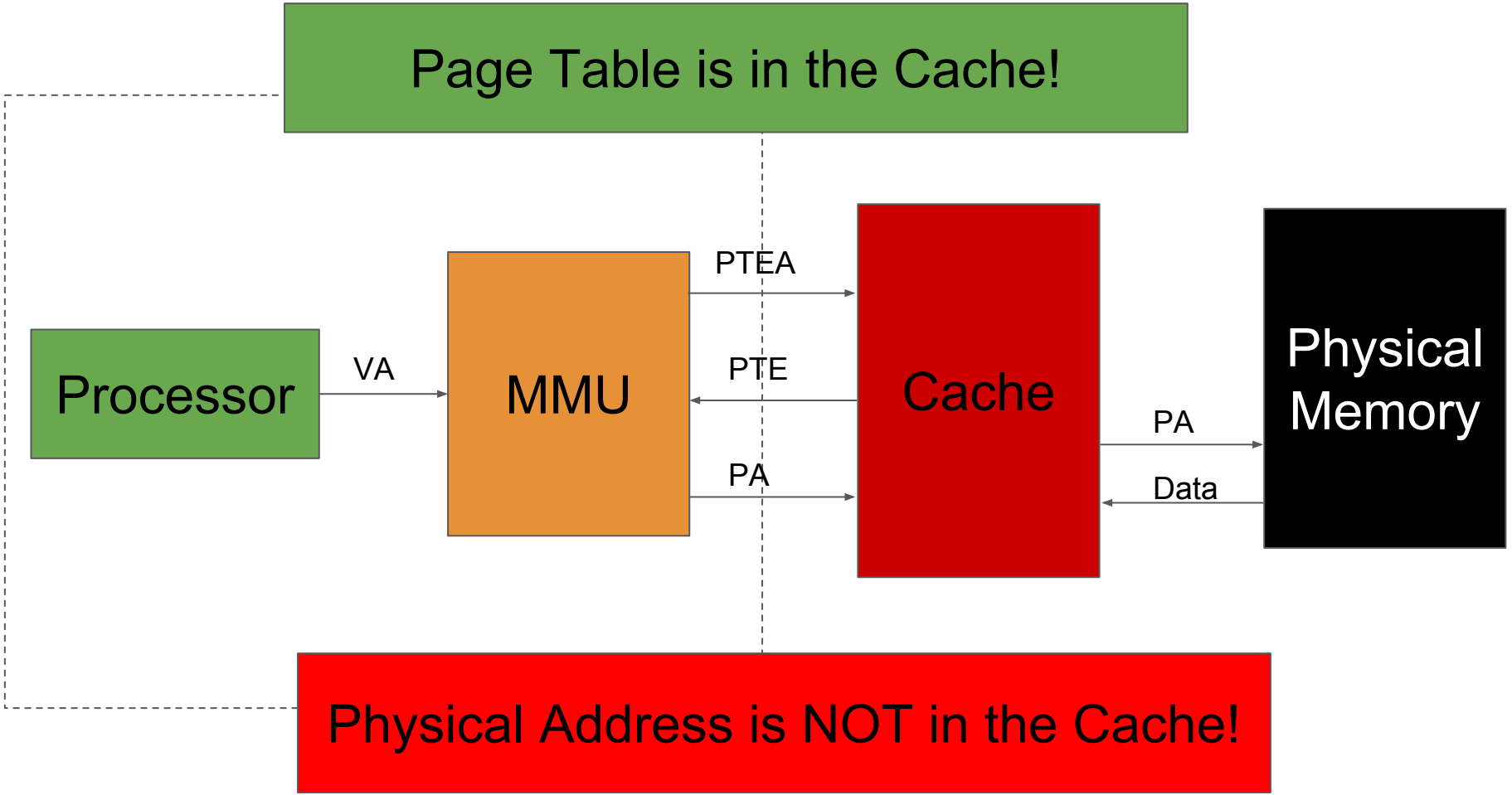

Page Table is in the Cache!
Processor
VA
MMU
PTEA
Cache
Physical Memory

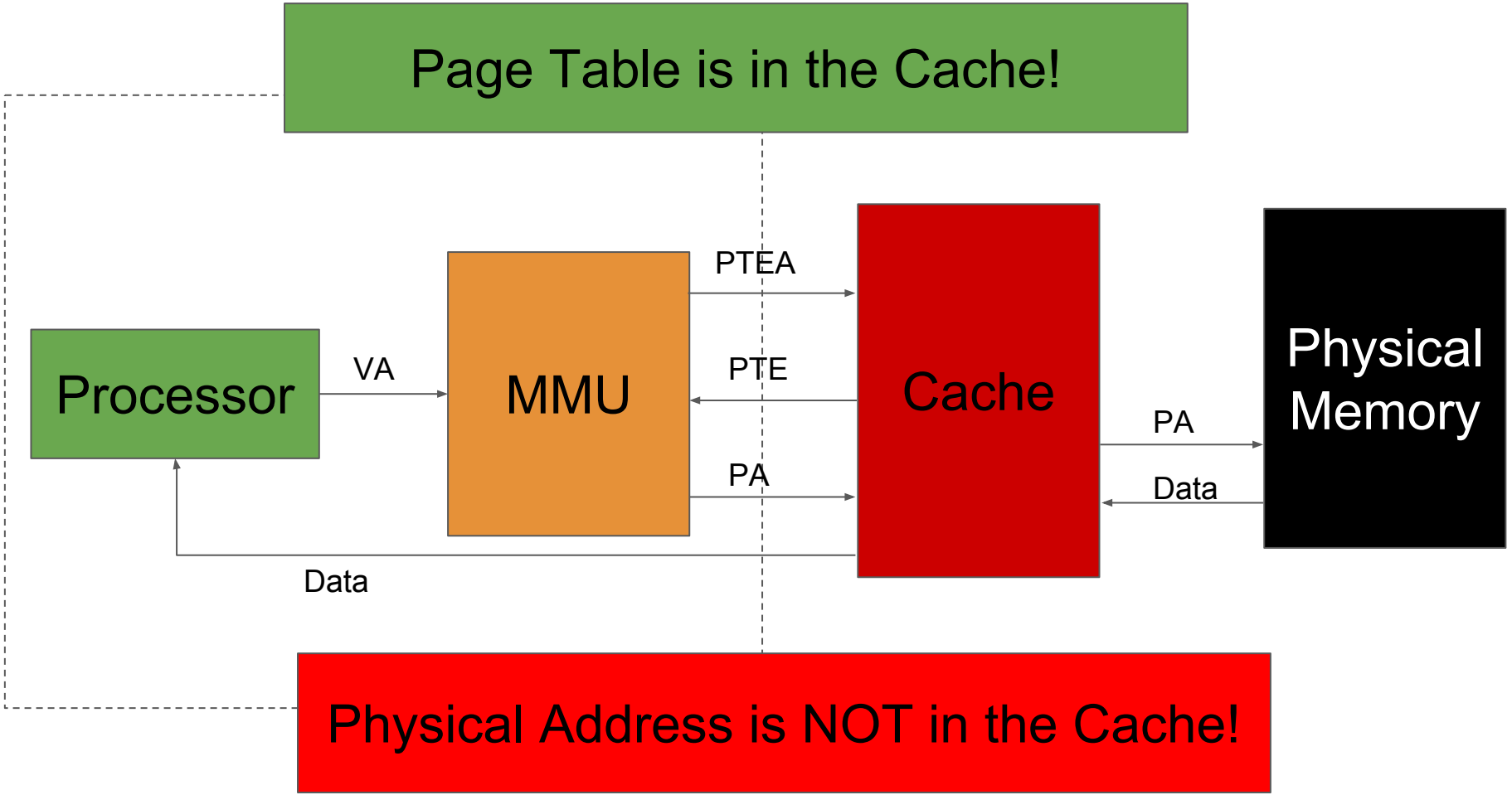

Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
Cache
Physical Memory


Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
Physical Memory


Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
Physical Memory
Physical Address is NOT in the Cache!


Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PA
Physical Memory
Physical Address is NOT in the Cache!

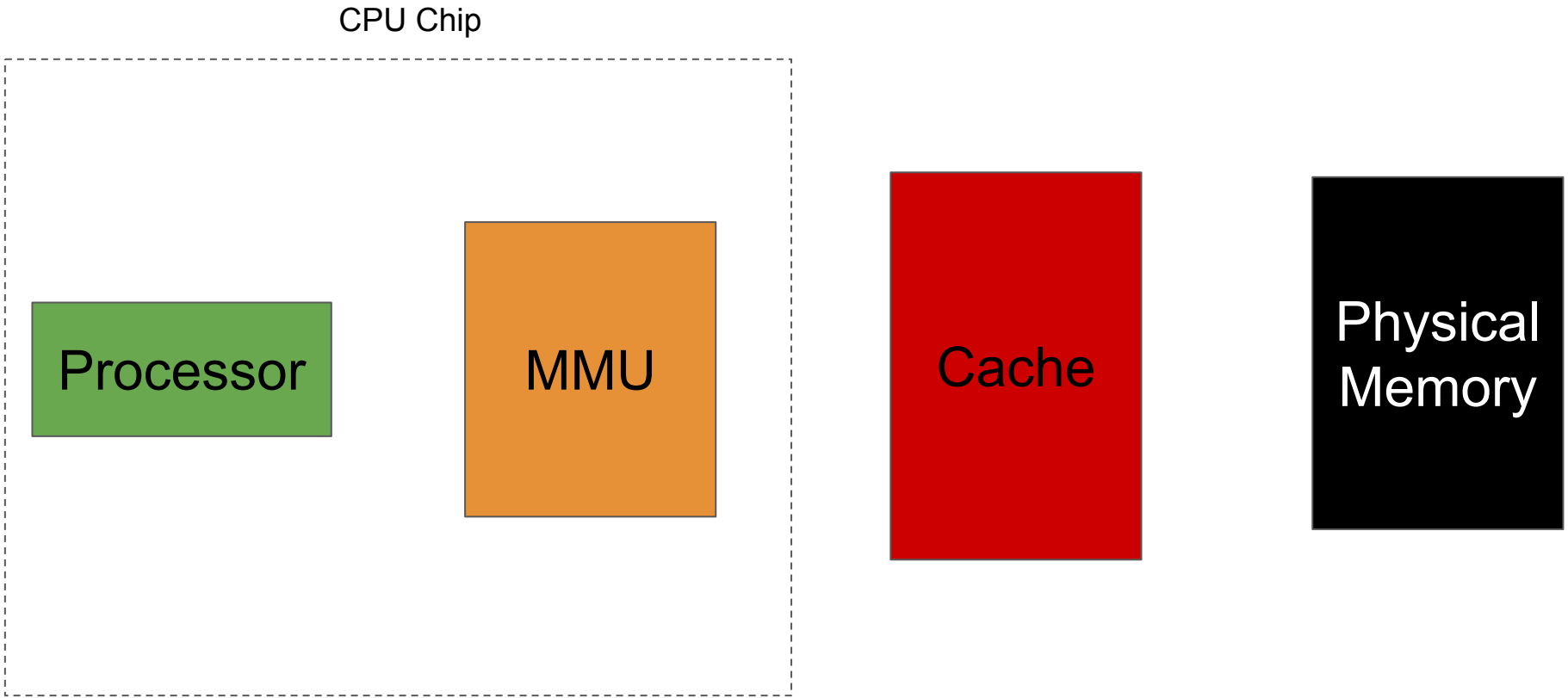

Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PA
Data
Physical Memory
Physical Address is NOT in the Cache!

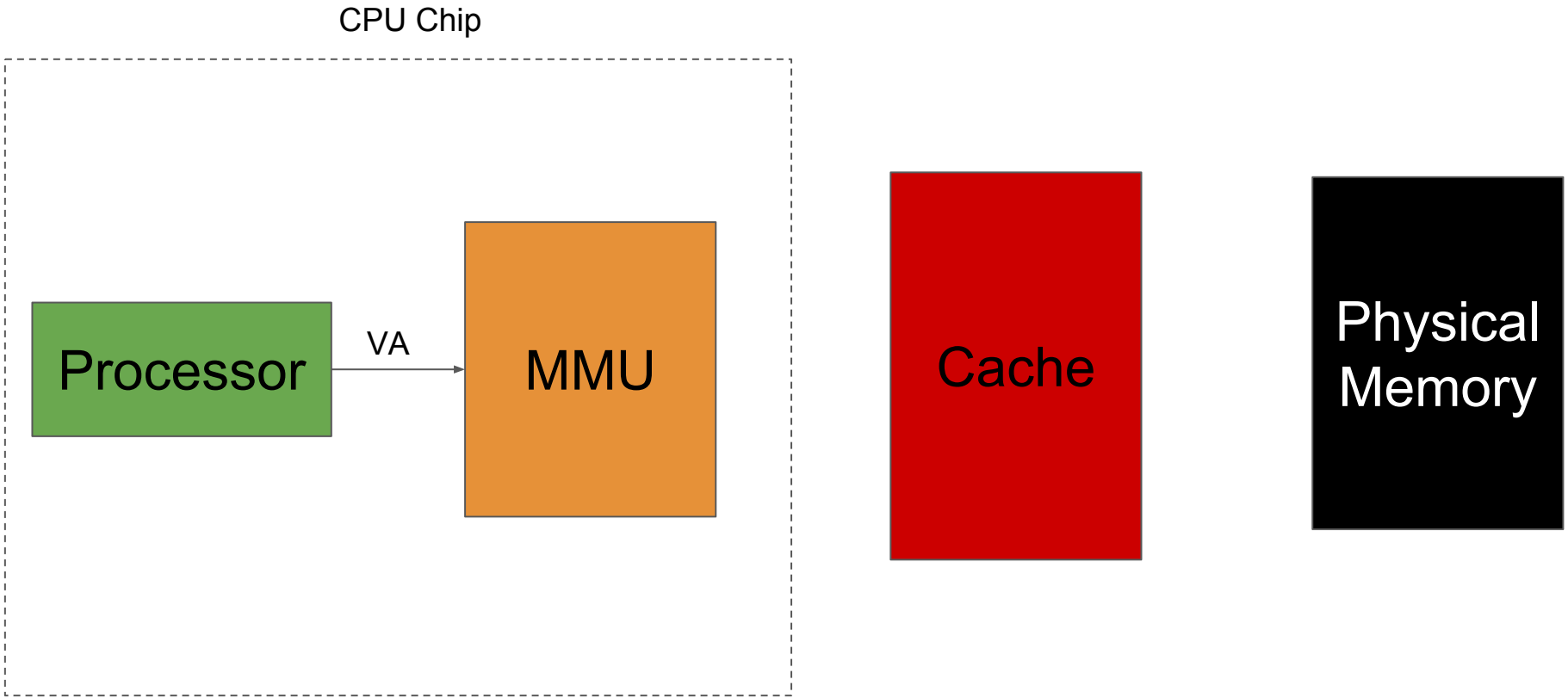

Page Table is in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PA
Data
Physical Memory
Data
Physical Address is NOT in the Cache!

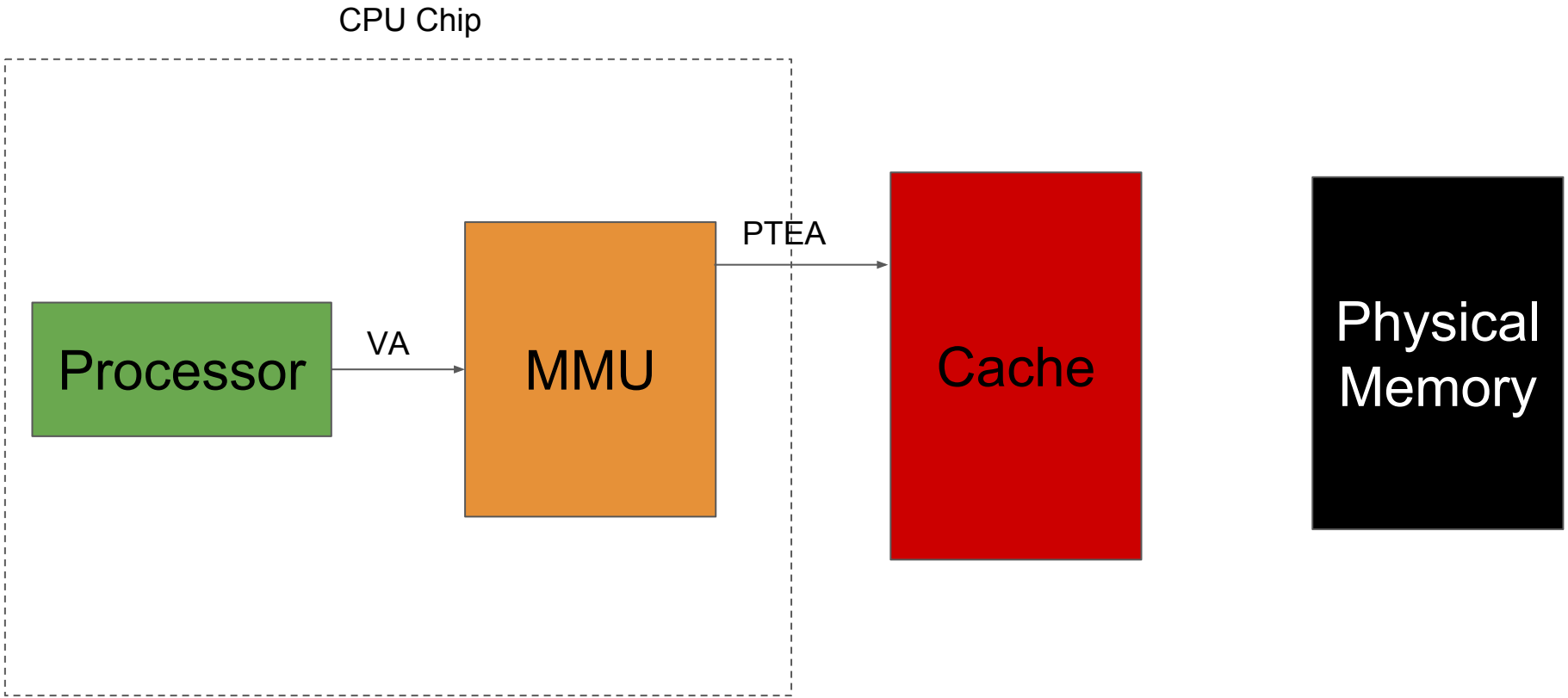
Scenario #3

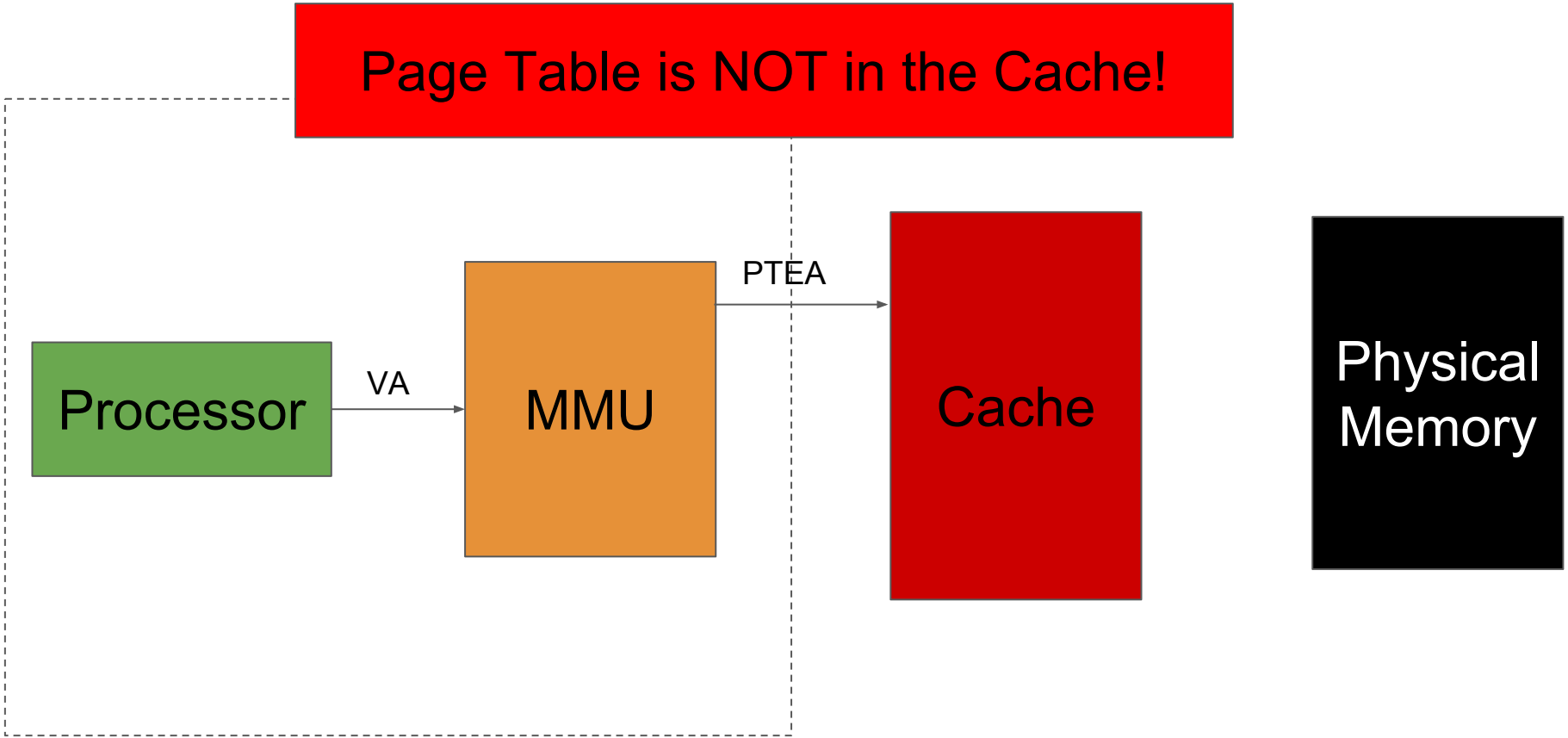
Page Table is NOT in the Cache

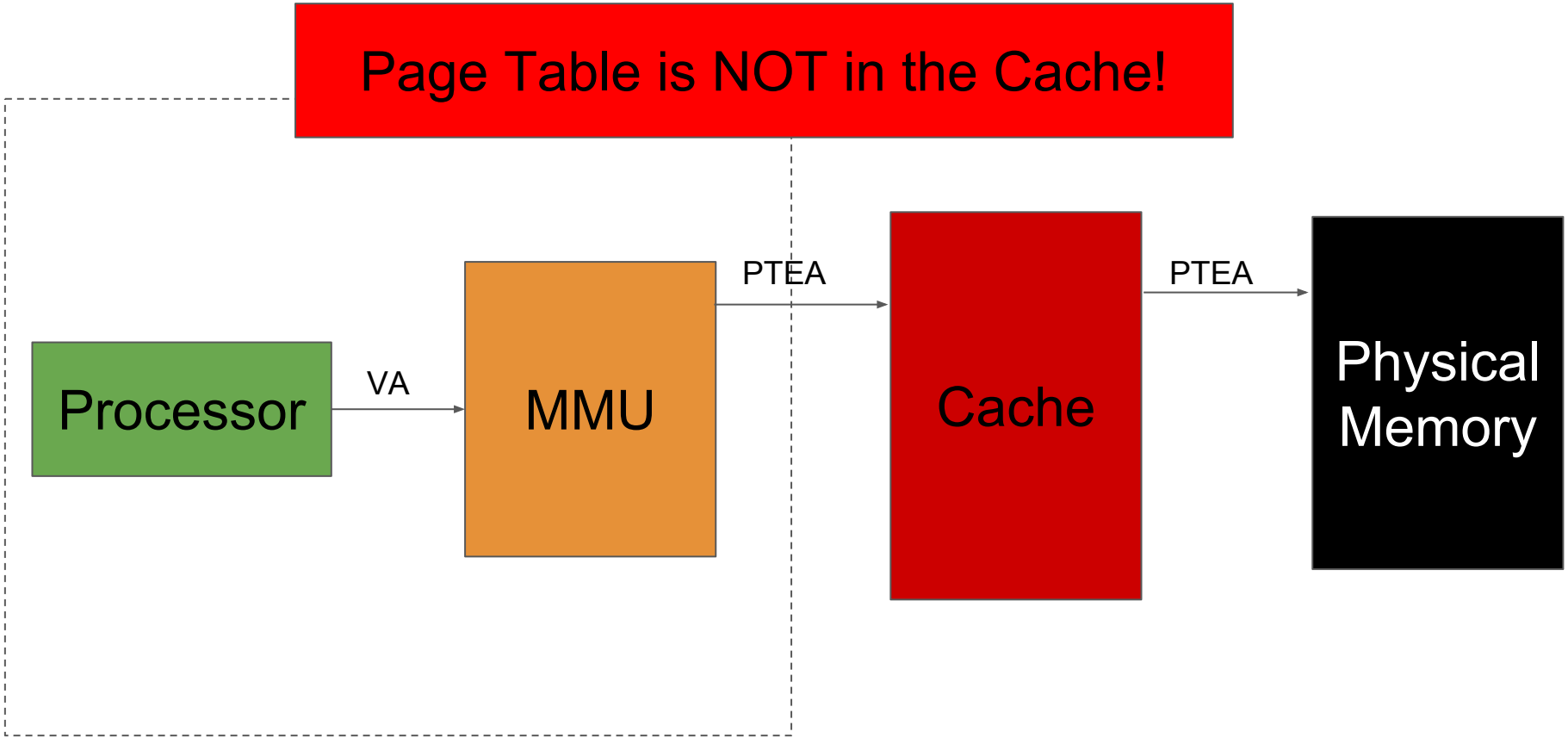
Physical Address is NOT in the Cache

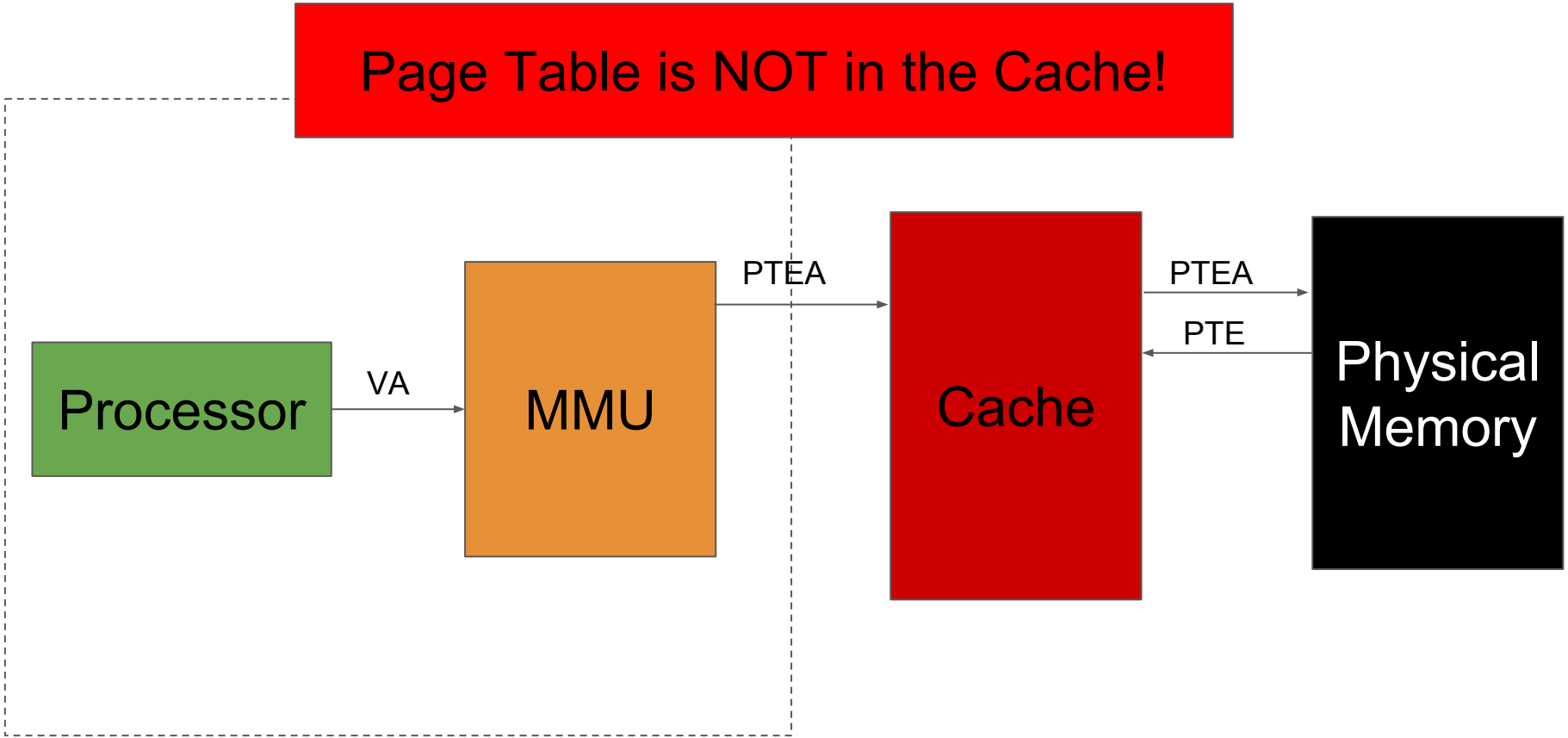

CPU Chip
Processor
MMU
Cache
Physical Memory

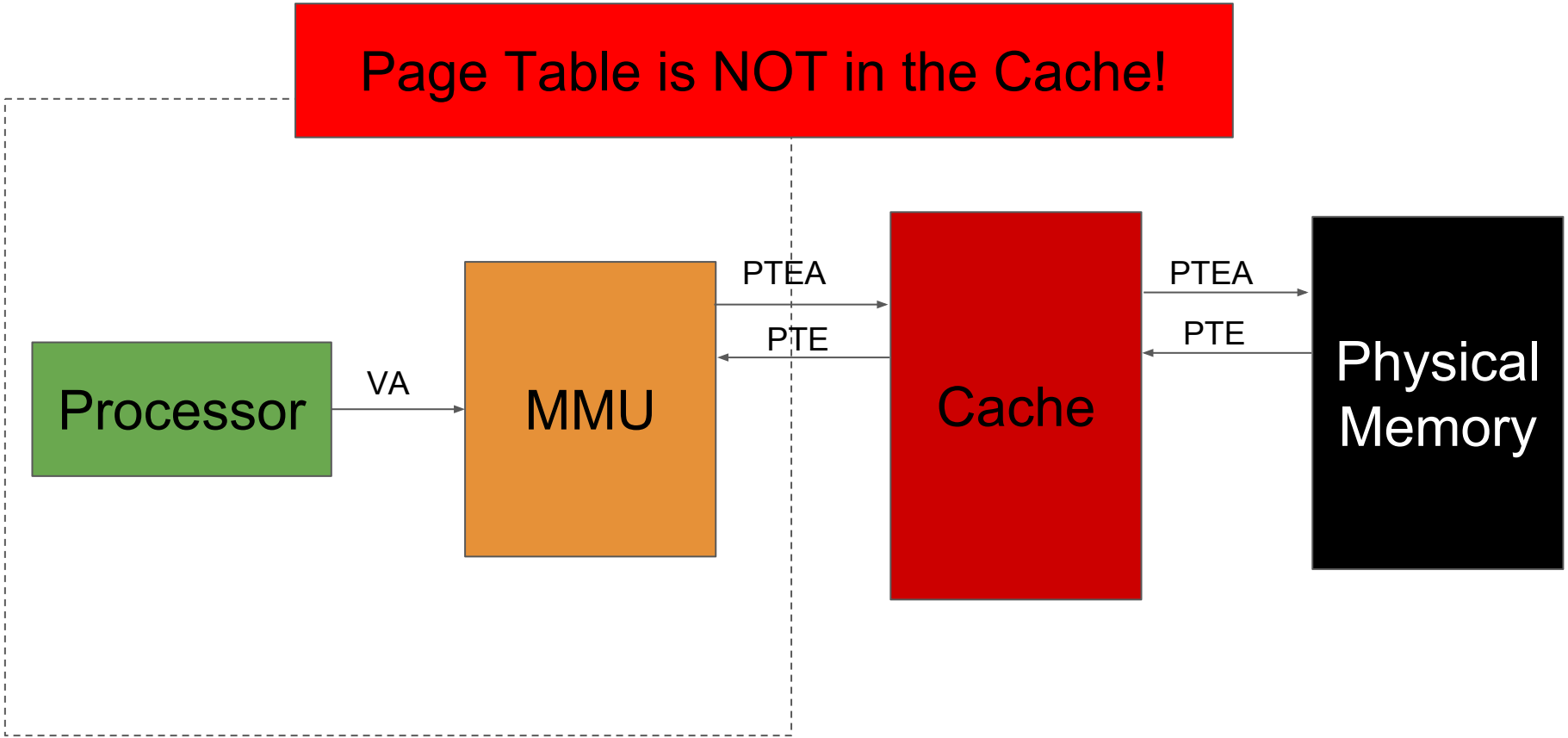

CPU Chip
Processor
VA
MMU
Cache
Physical Memory

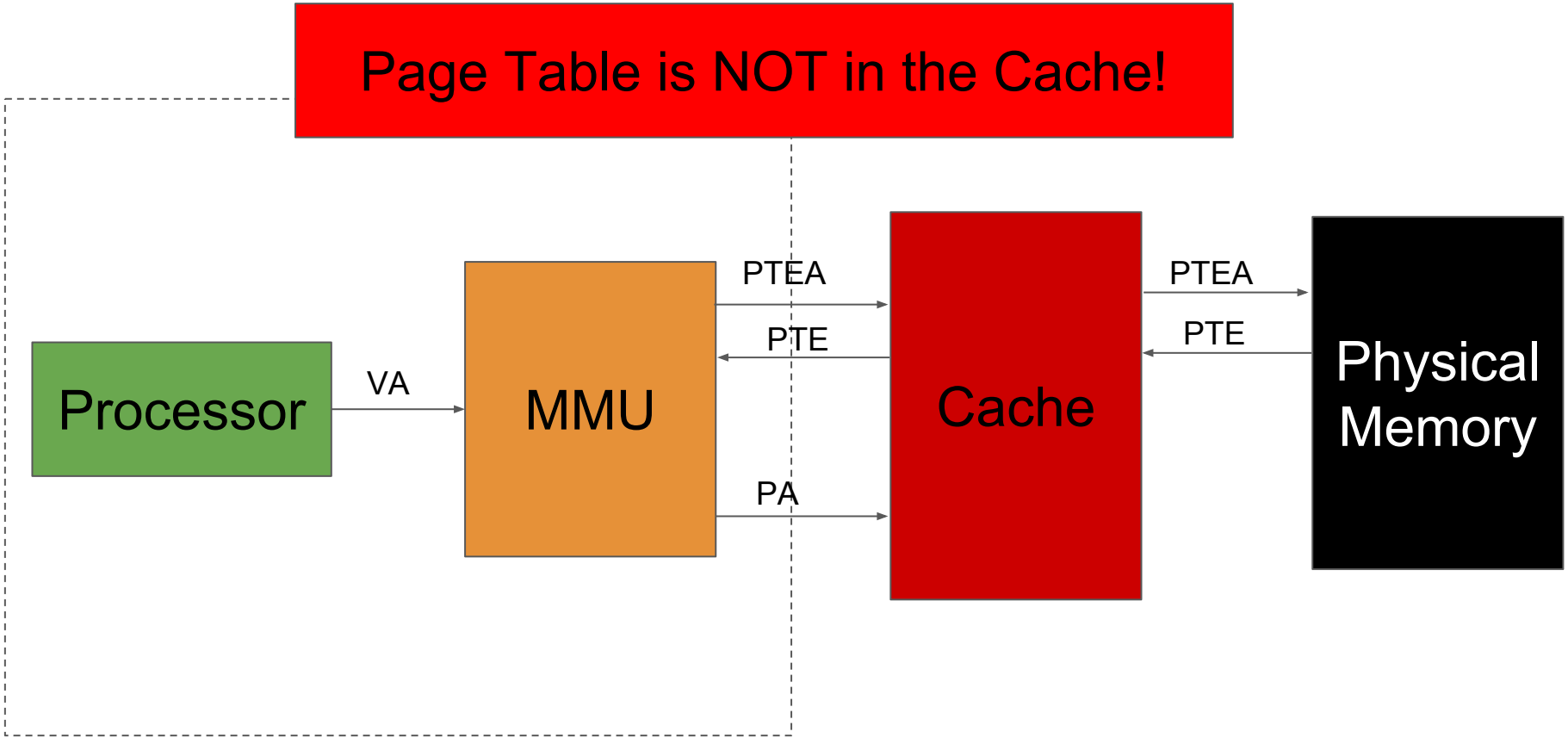

CPU Chip
Processor
VA
MMU
PTEA
Cache
Physical Memory

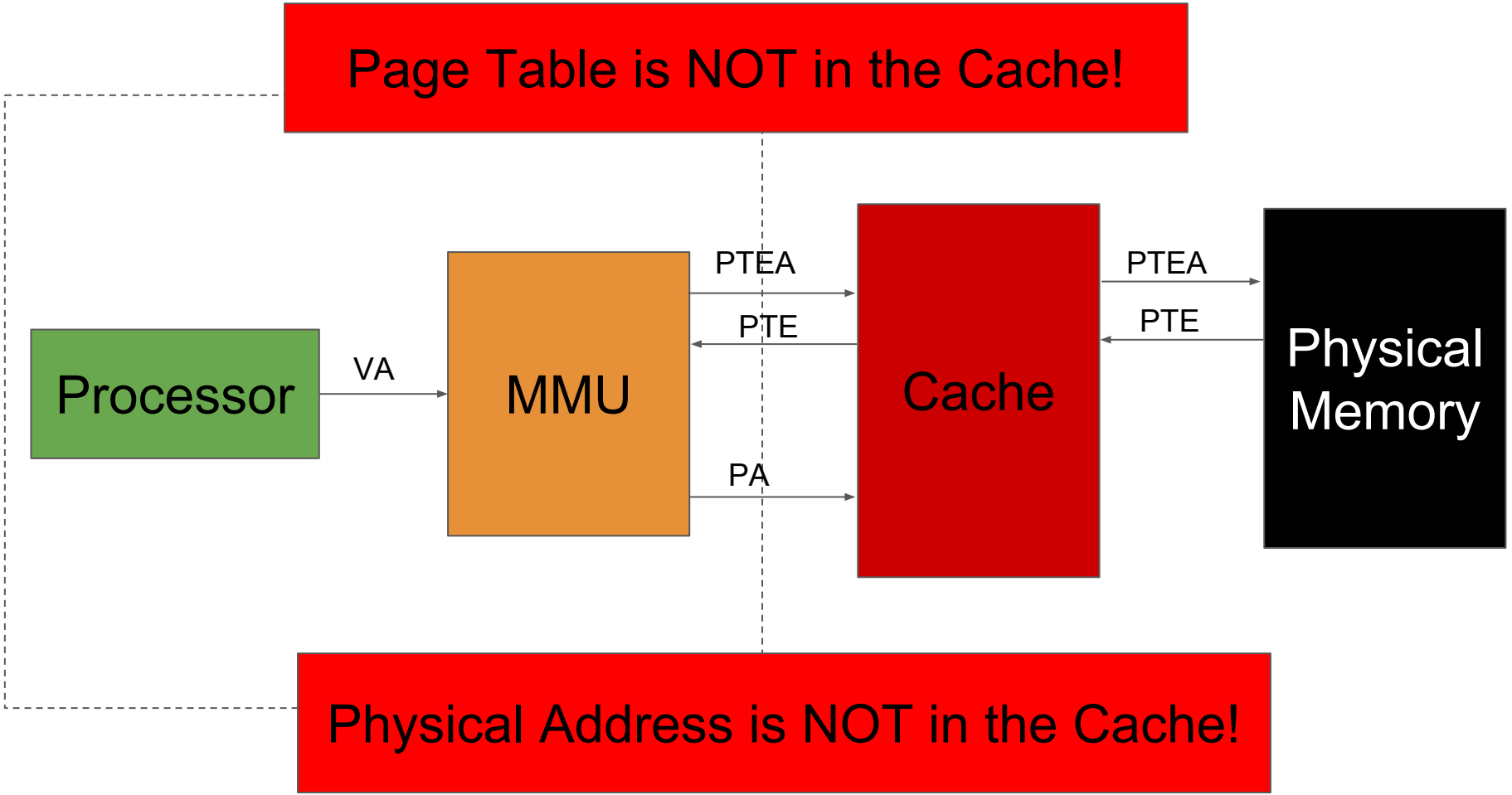

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
Cache
Physical Memory

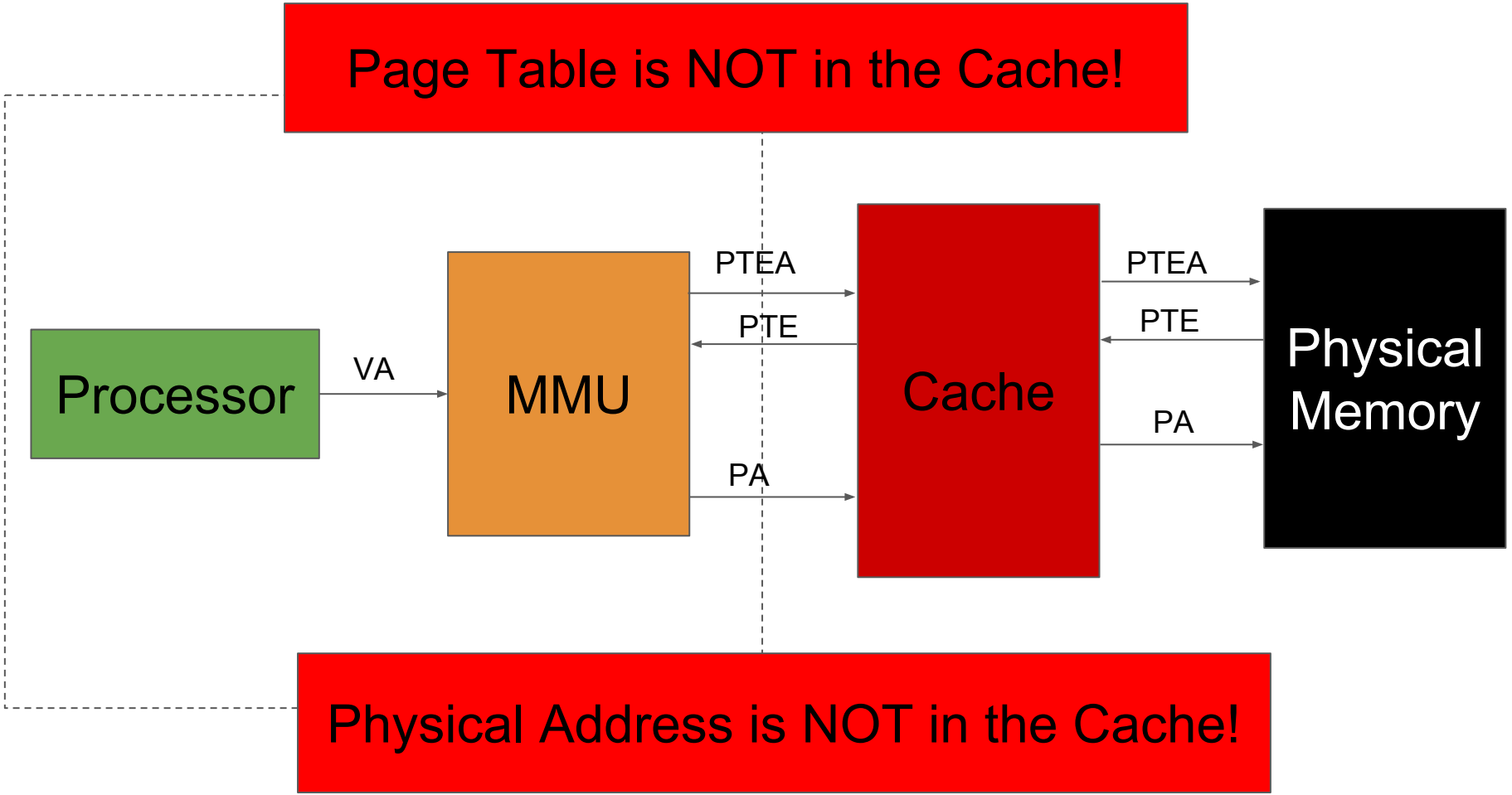

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
Cache
PTEA
Physical Memory

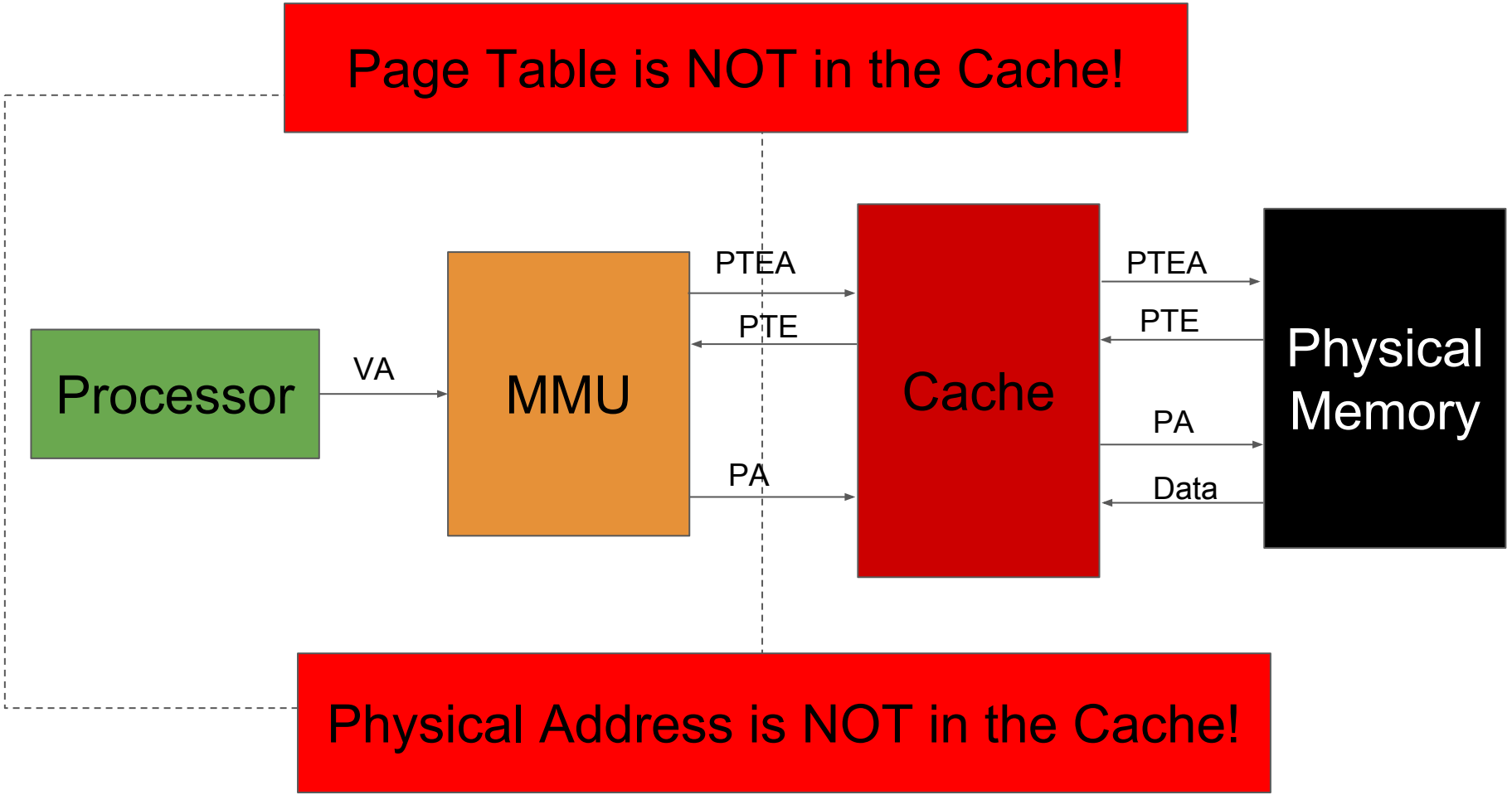

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
Cache
PTEA
PTE
Physical Memory

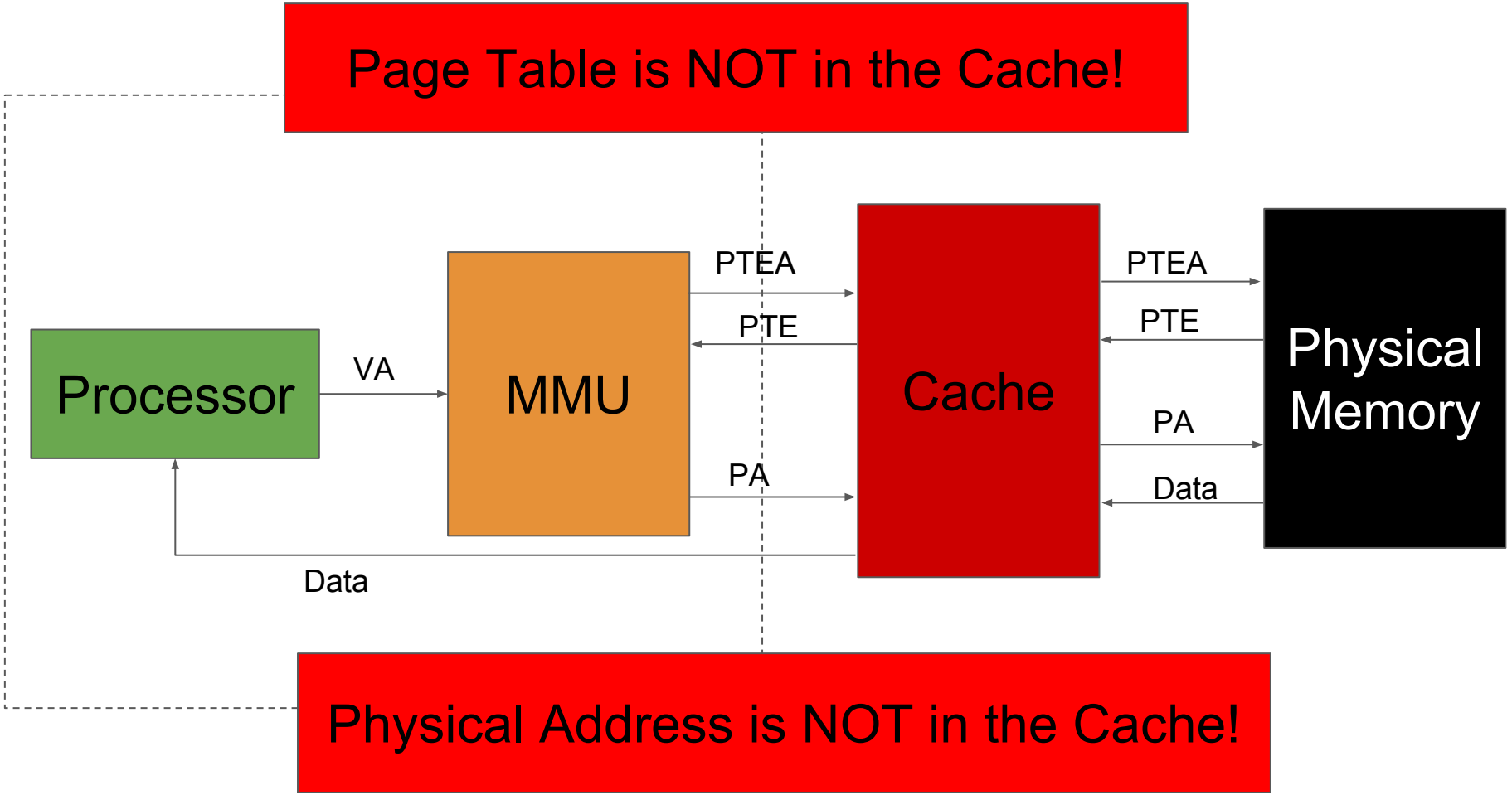

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
PTE
Cache
PTEA
PTE
Physical Memory


Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PTEA
PTE
Physical Memory

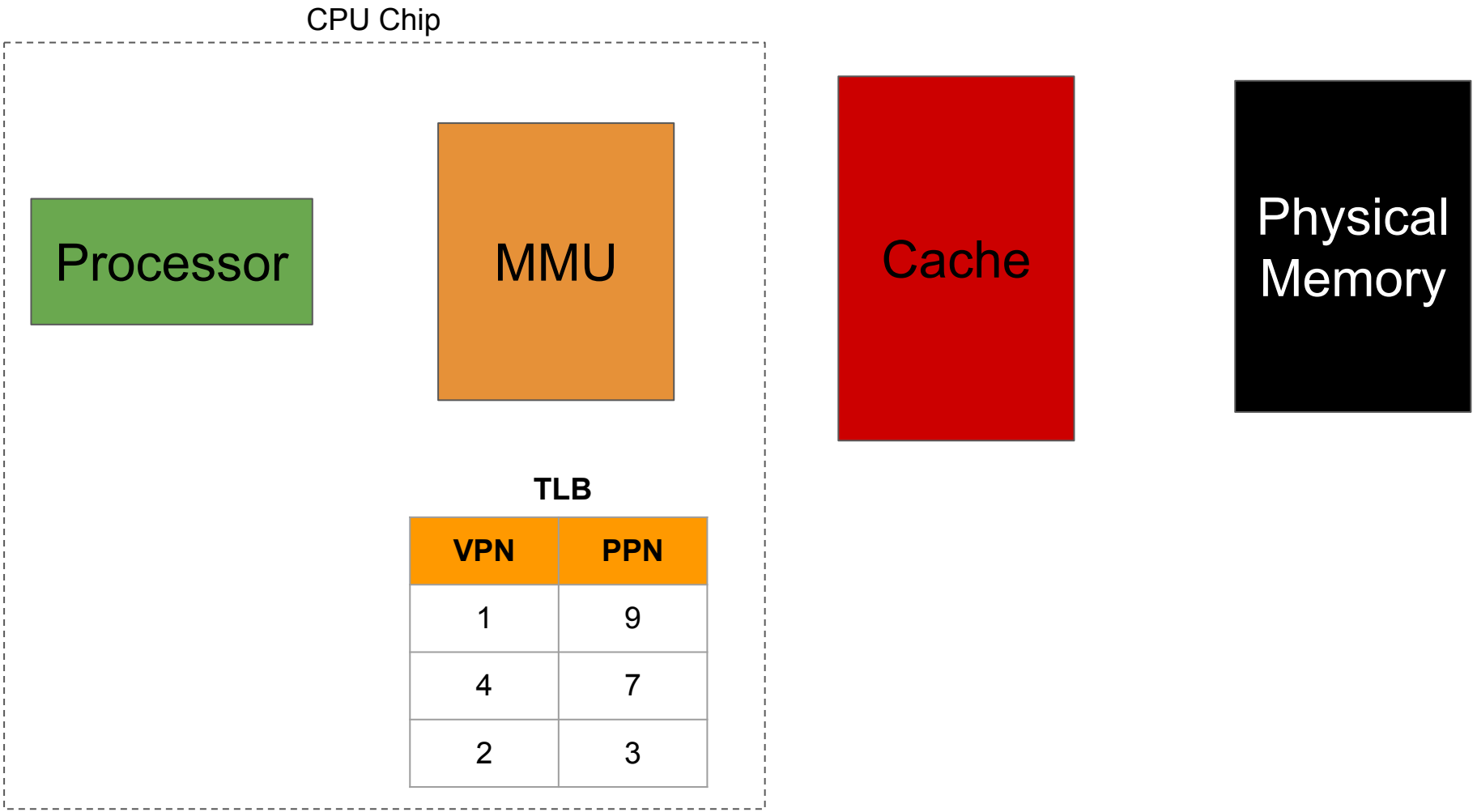

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PTEA
PTE
Physical Memory
Physical Address is NOT in the Cache!


Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PTEA
PTE
PA
Physical Memory
Physical Address is NOT in the Cache!

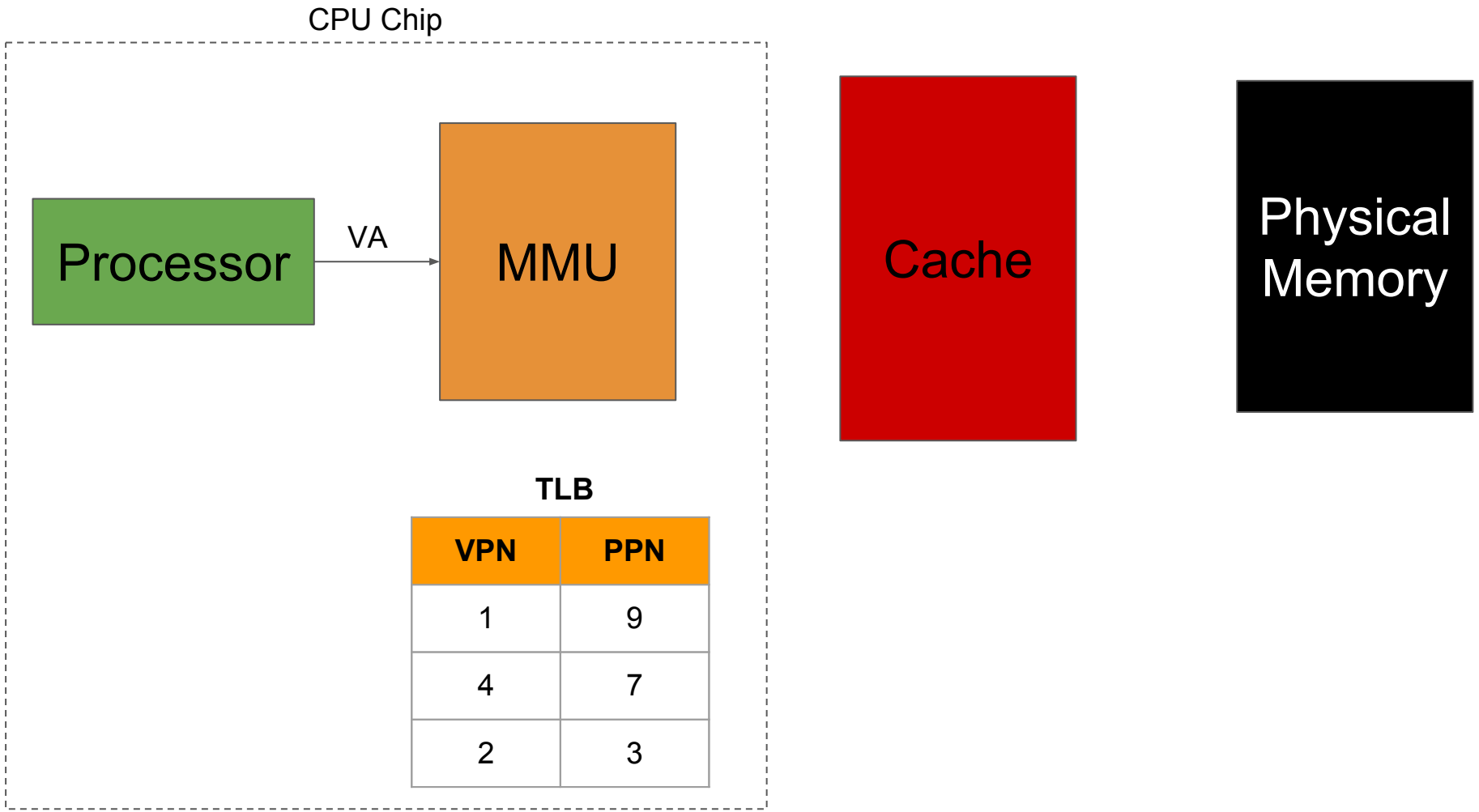

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Cache
PTEA
PTE
PA
Data
Physical Memory
Physical Address is NOT in the Cache!

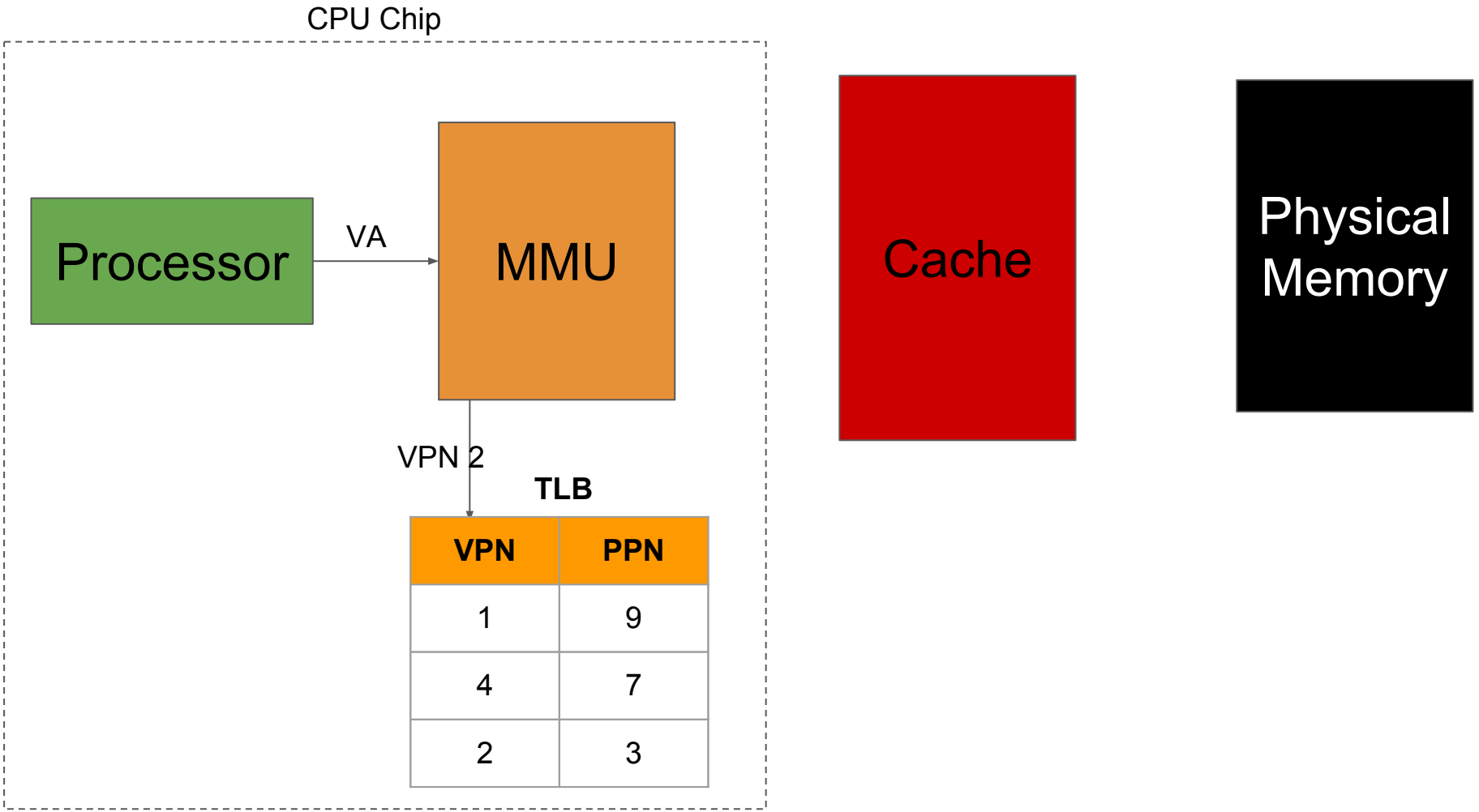

Page Table is NOT in the Cache!
Processor
VA
MMU
PTEA
PTE
PA
Data
Cache
PTEA
PTE
PA
Data
Physical Memory
Physical Address is NOT in the Cache!

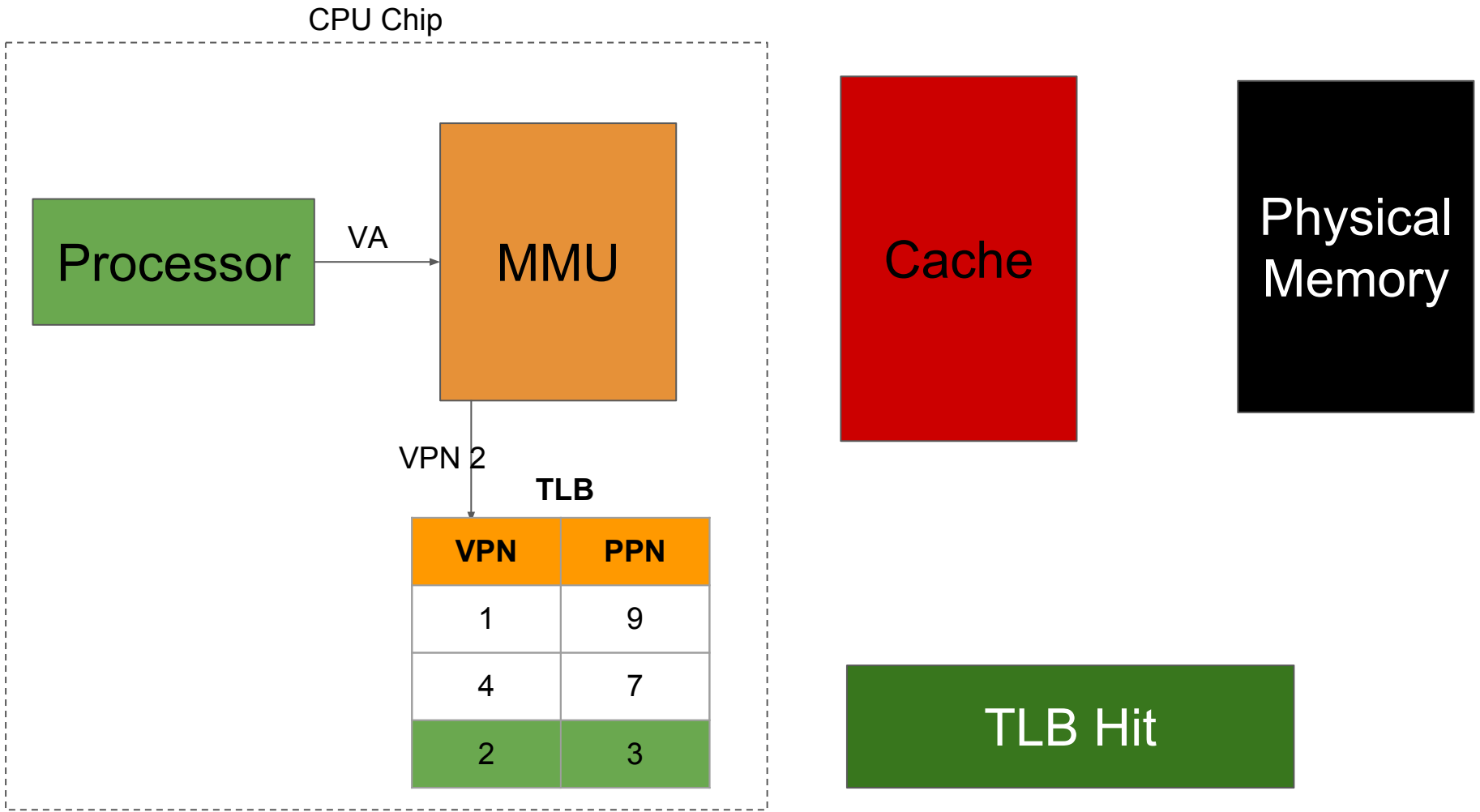
Translation Lookaside Buffer(TLB)

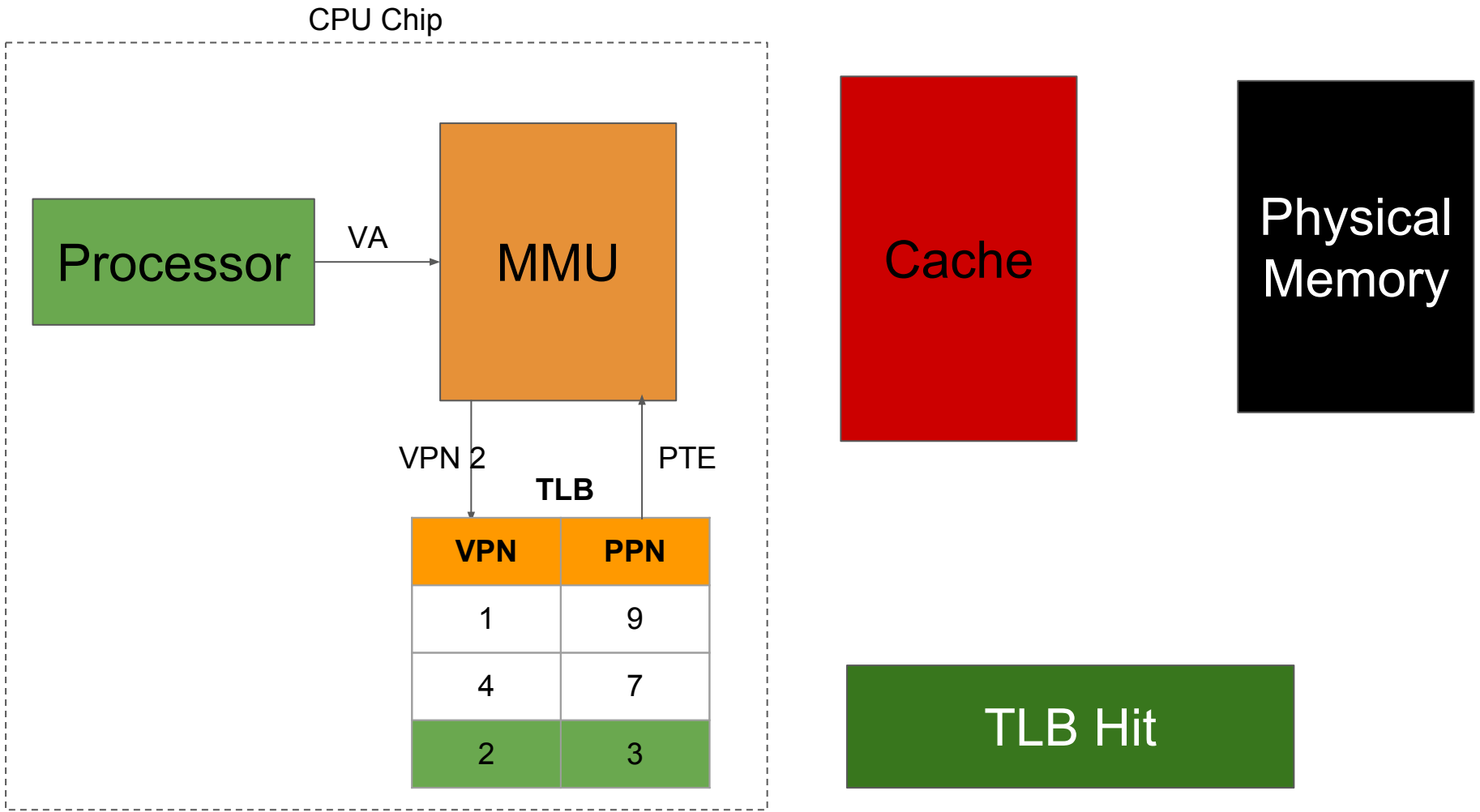

CPU Chip
Processor
MMU
Cache
Physical Memory
TLB
VPN
PPN
1
9
4
7
2
3

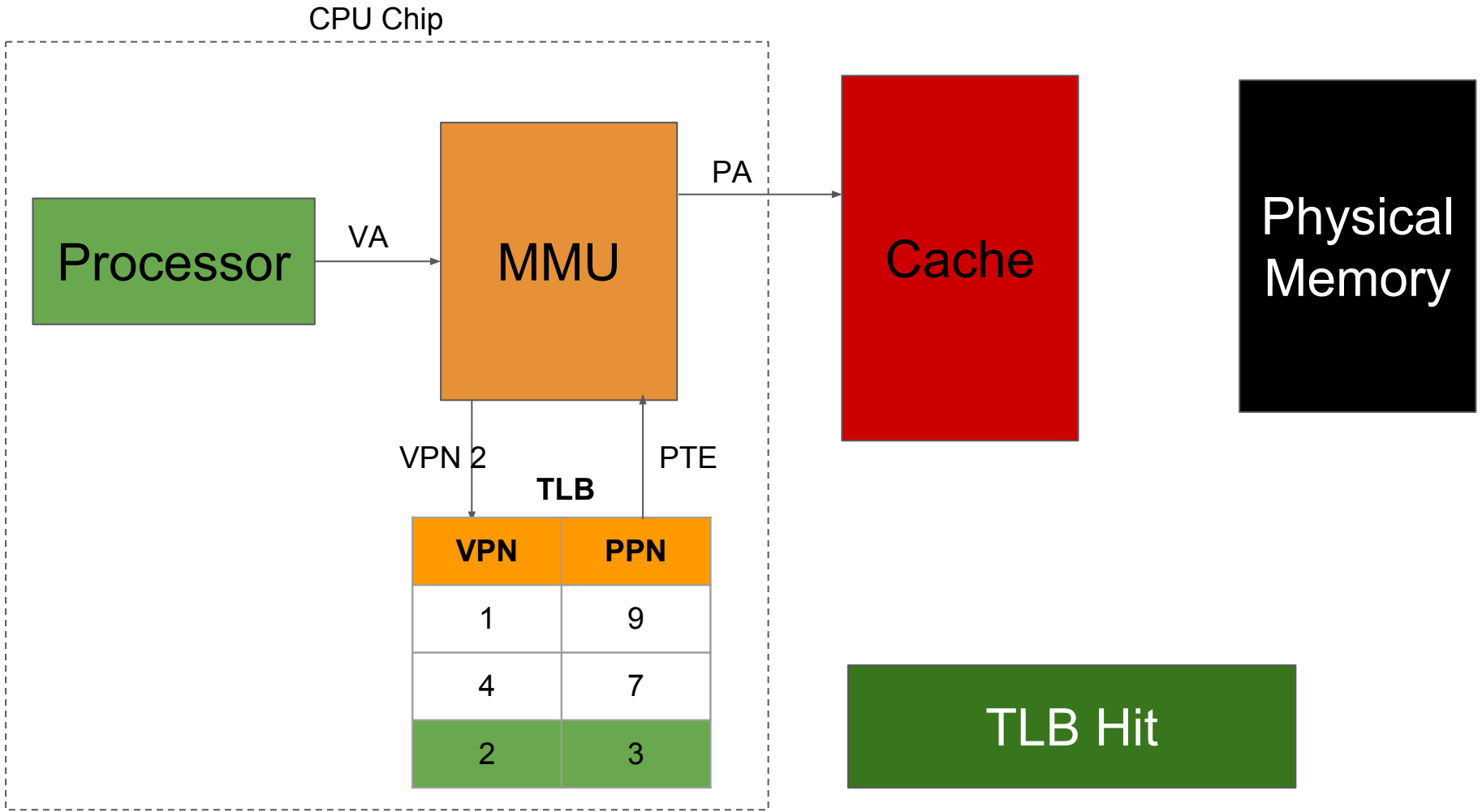
TLB Hit

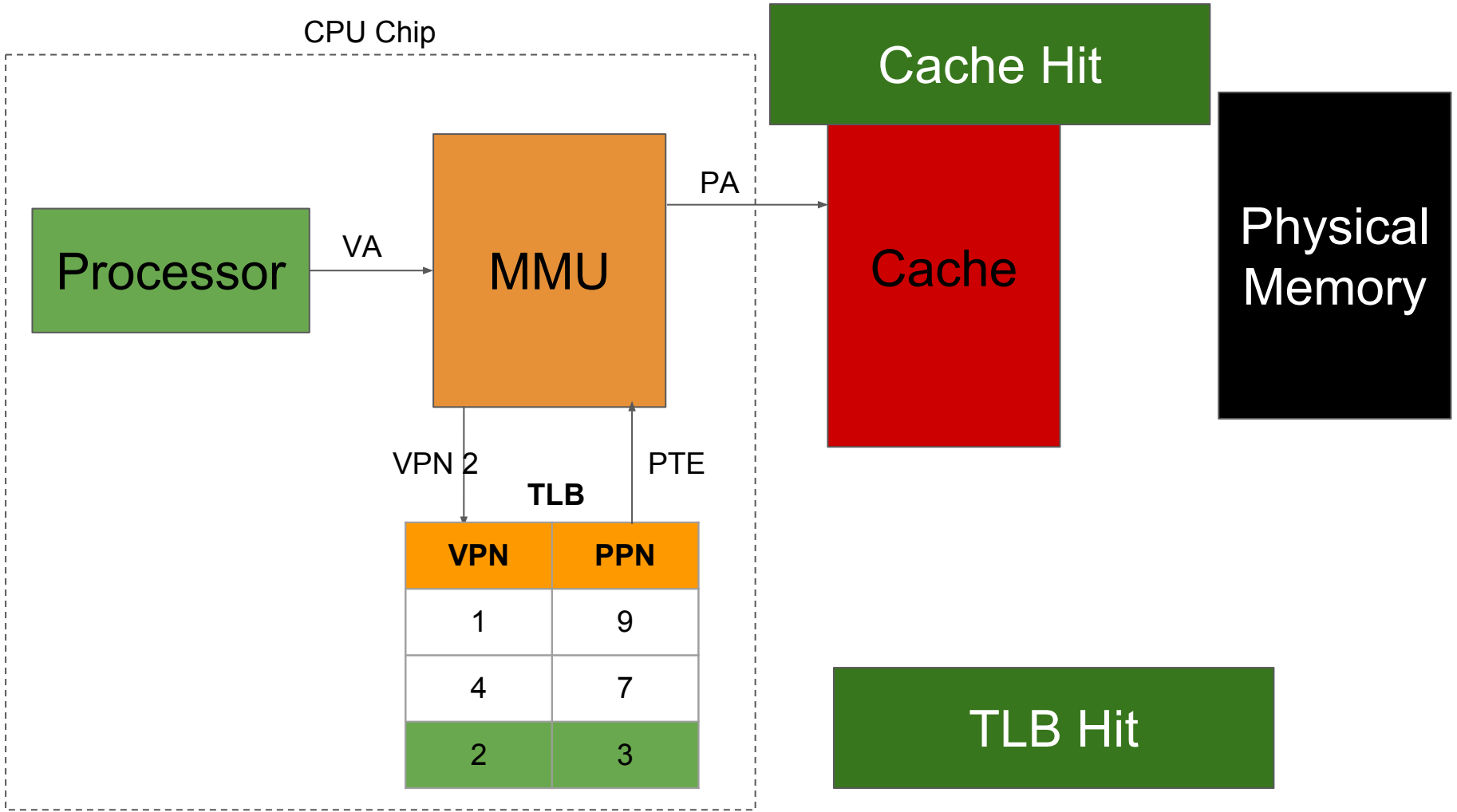

CPU Chip
Processor
VA
MMU
Cache
Physical Memory
TLB
VPN
PPN
1
9
4
7
2
3

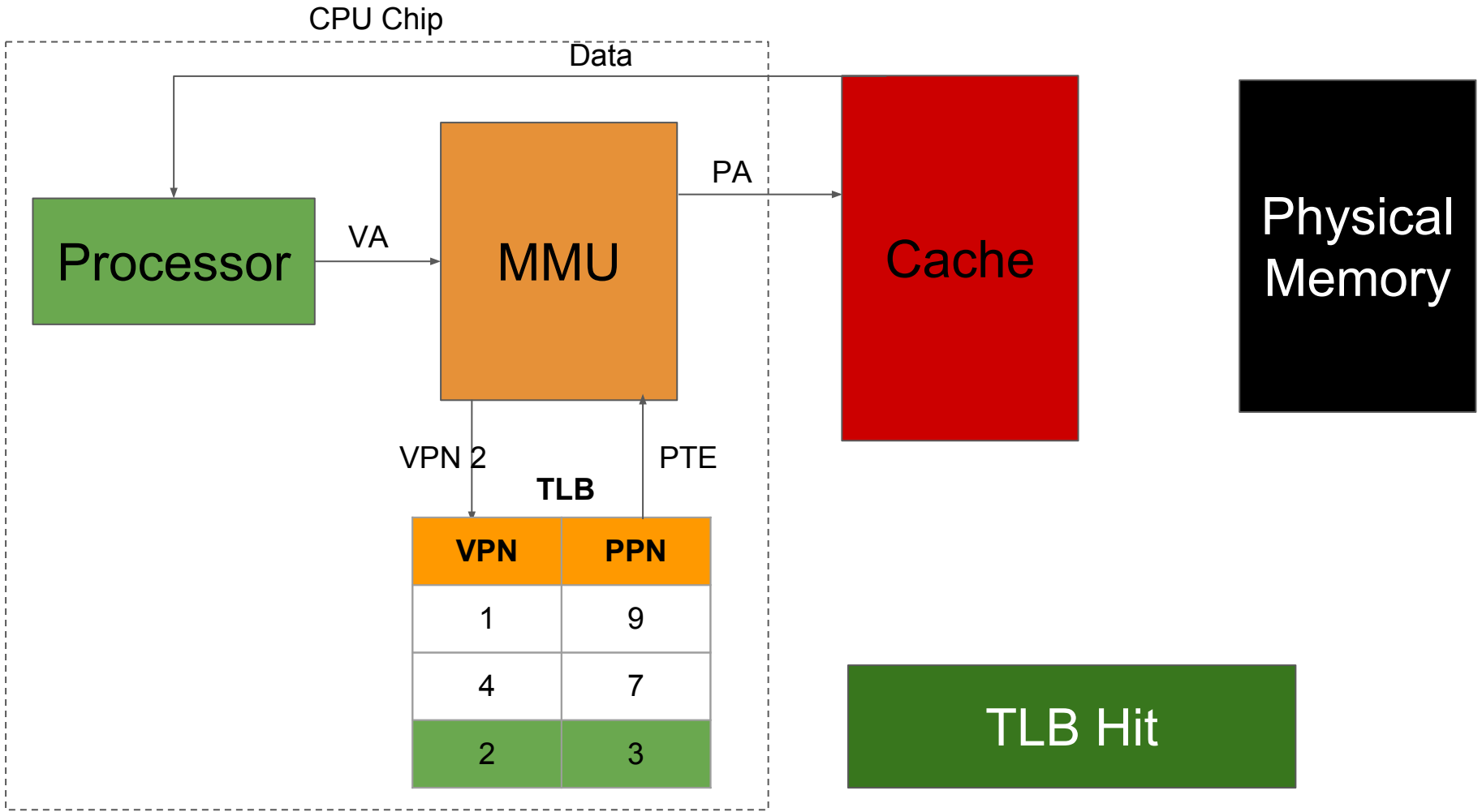

CPU Chip
Processor
VA
MMU
VPN 2
TLB
VPN
PPN
1
9
4
7
2
3
Cache
Physical Memory


CPU Chip
Processor
VA
MMU
VPN 2
TLB
VPN
PPN
1
9
4
7
2
3
Cache
Physical Memory
TLB Hit

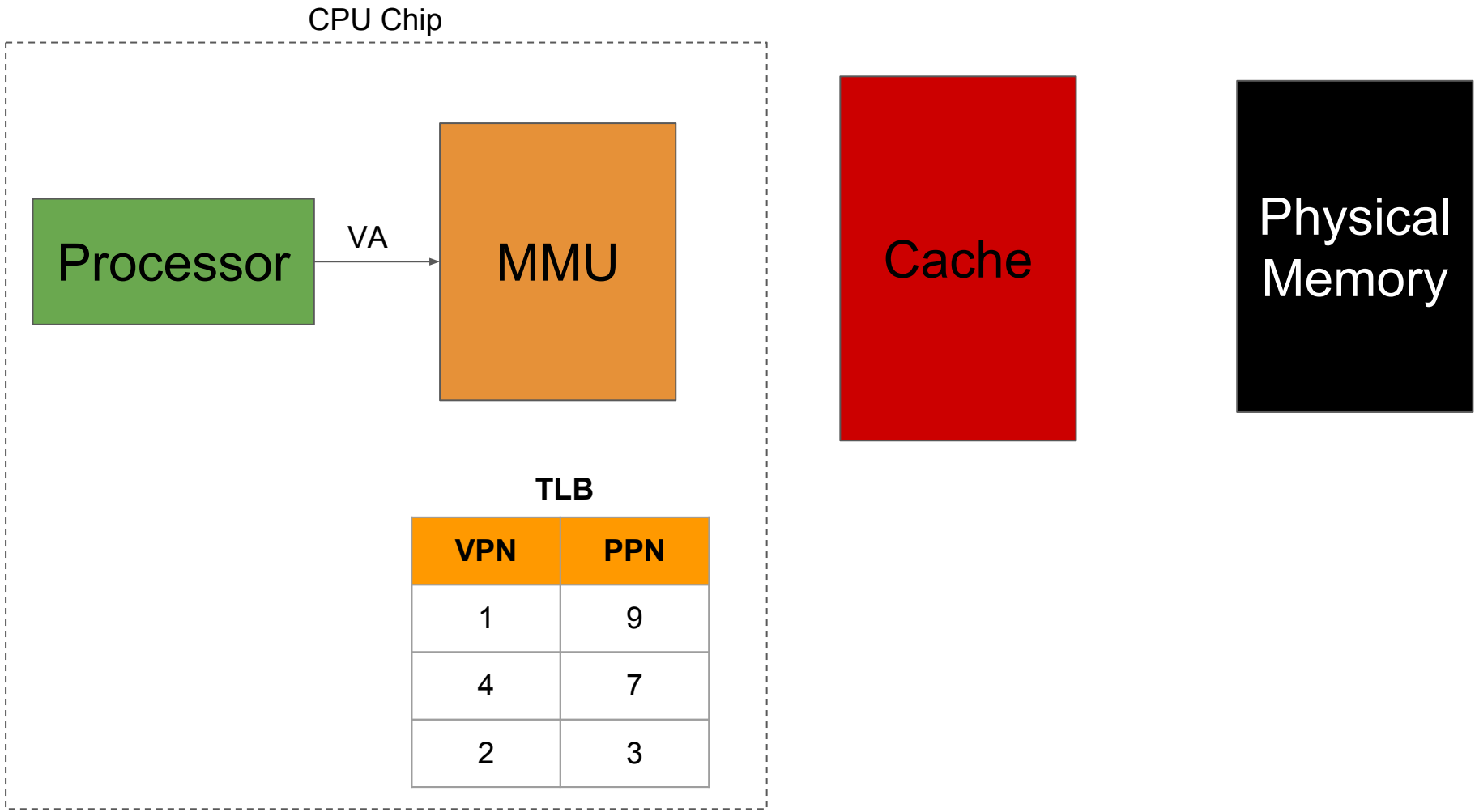

CPU Chip
Processor
VA
MMU
VPN 2
PTE
TLB
VPN
PPN
1
9
4
7
2
3
Cache
Physical Memory
TLB Hit


CPU Chip
Processor
VA
MMU
PA
Cache
Physical Memory
VPN 2
PTE
TLB
VPN
PPN
1
9
4
7
2
3
TLB Hit


CPU Chip
Cache Hit
Physical Memory
Processor
VA
MMU
PA
Cache
VPN 2
PTE
TLB
VPN
PPN
1
9
4
7
2
3
TLB Hit


CPU Chip
Data
Processor
VA
MMU
PA
Cache
Physical Memory
VPN 2
PTE
TLB
VPN
PPN
1
9
4
7
2
3
TLB Hit

TLB Miss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VPN
PPN
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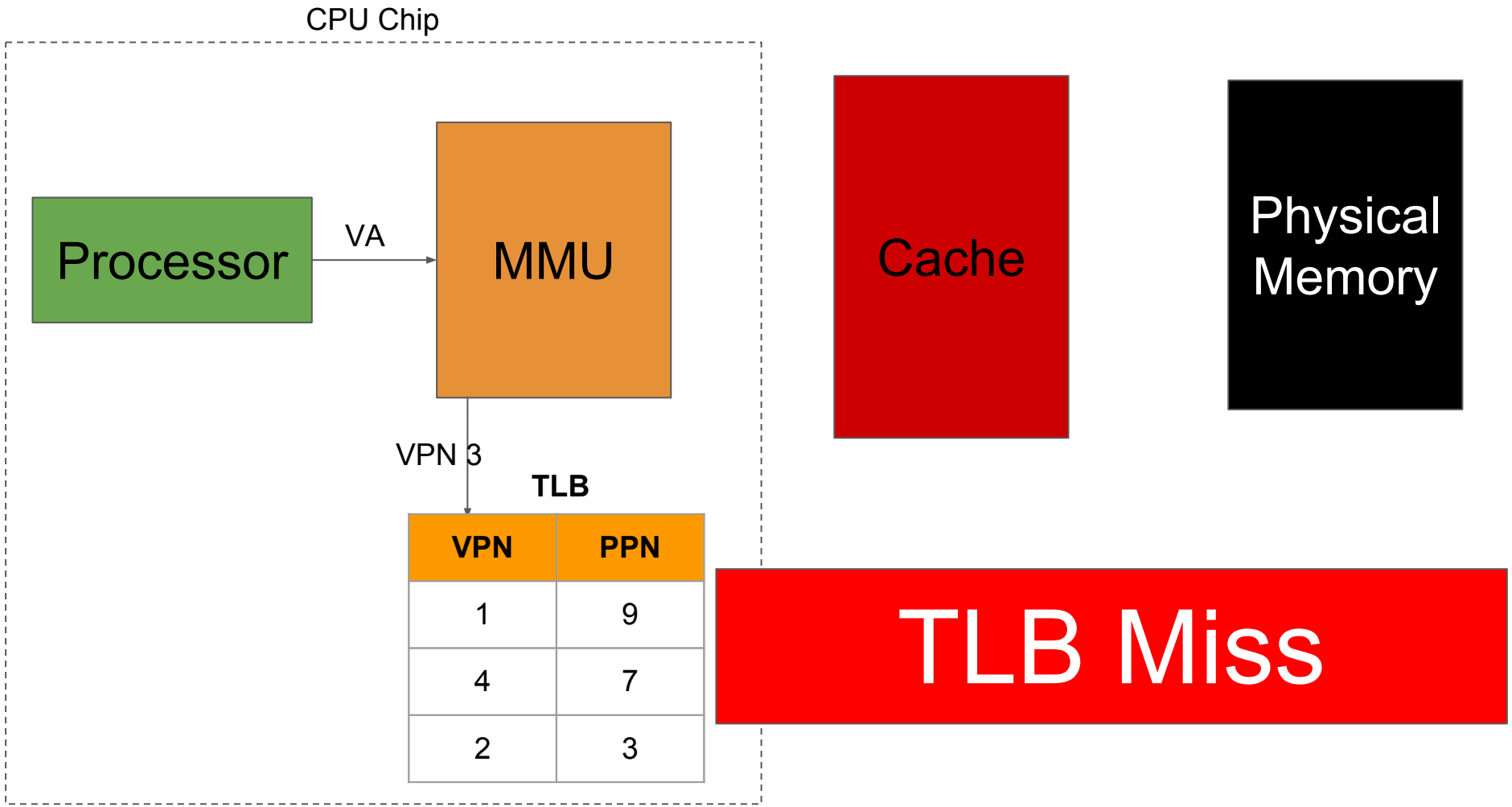
CPU Chip
Processor
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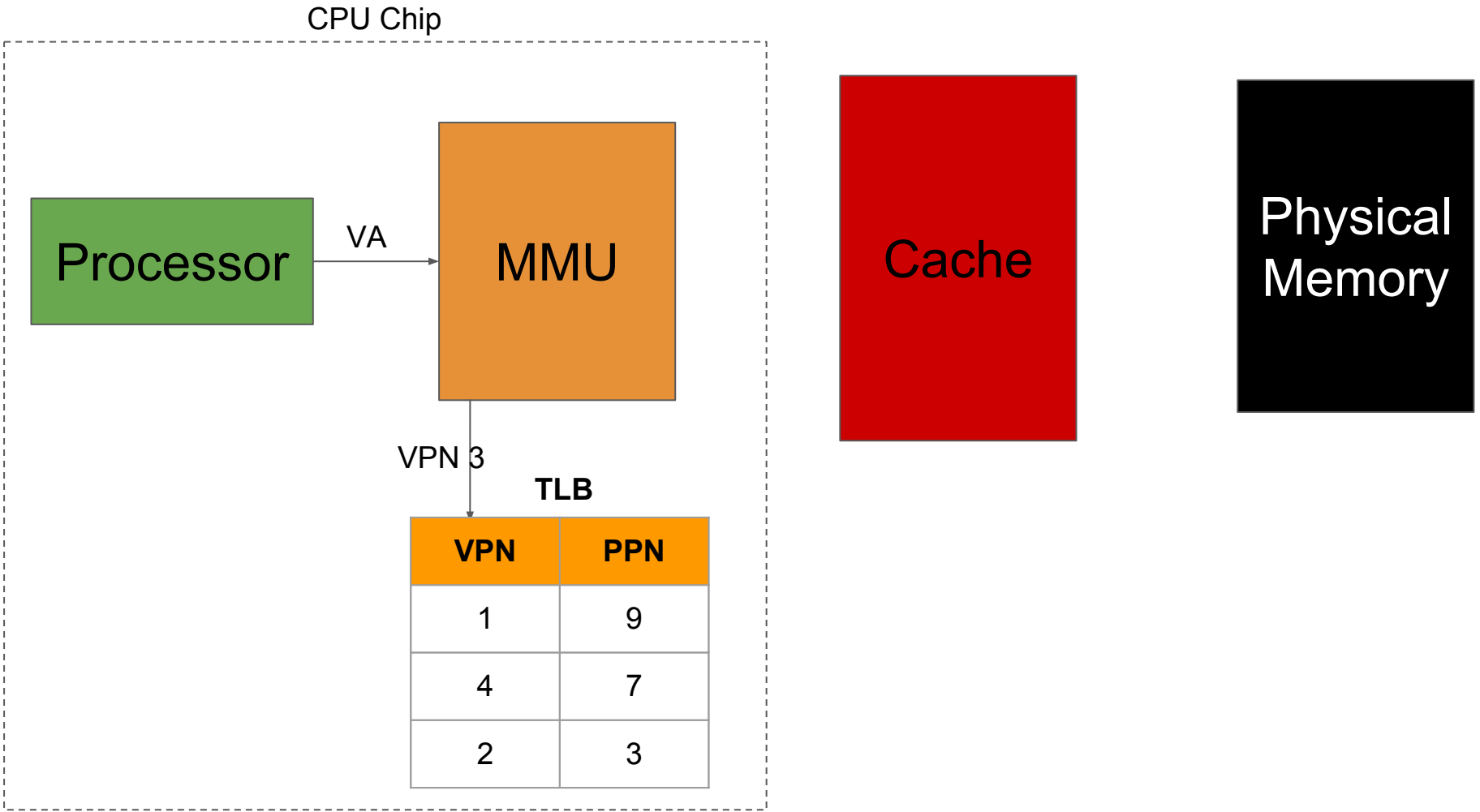
MMU
VPN 3
TLB
VPN
PPN
1
9
4
7
2
3
Cache
Physical Memory
TLB Miss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Processor
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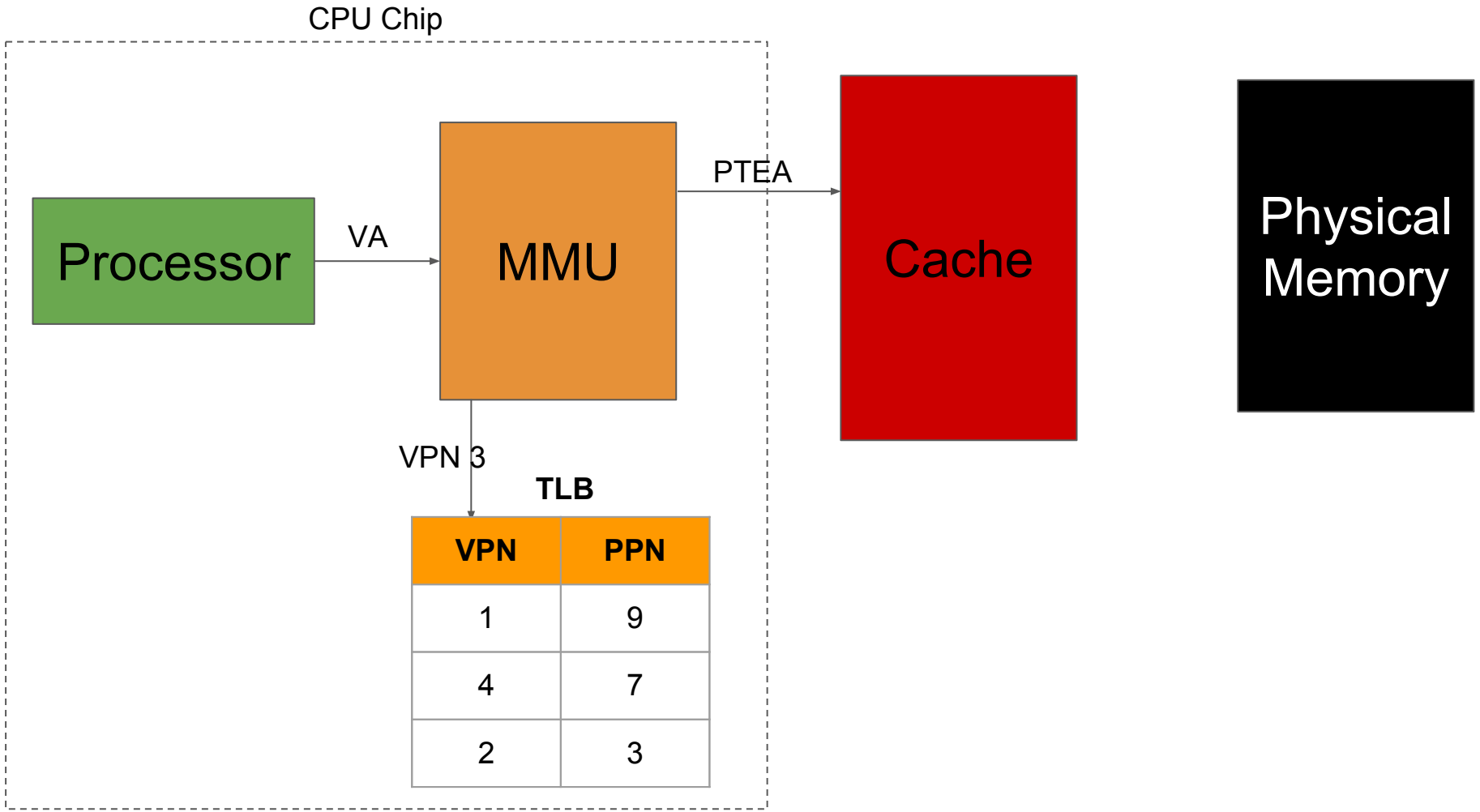
MMU
VPN 3
TLB
VPN
PPN
1
9
4
7
2
3
Cache
Physical Memory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MMU
PTEA
Cache
Physical Memory
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TLB
VPN
PPN
1
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4
7
2
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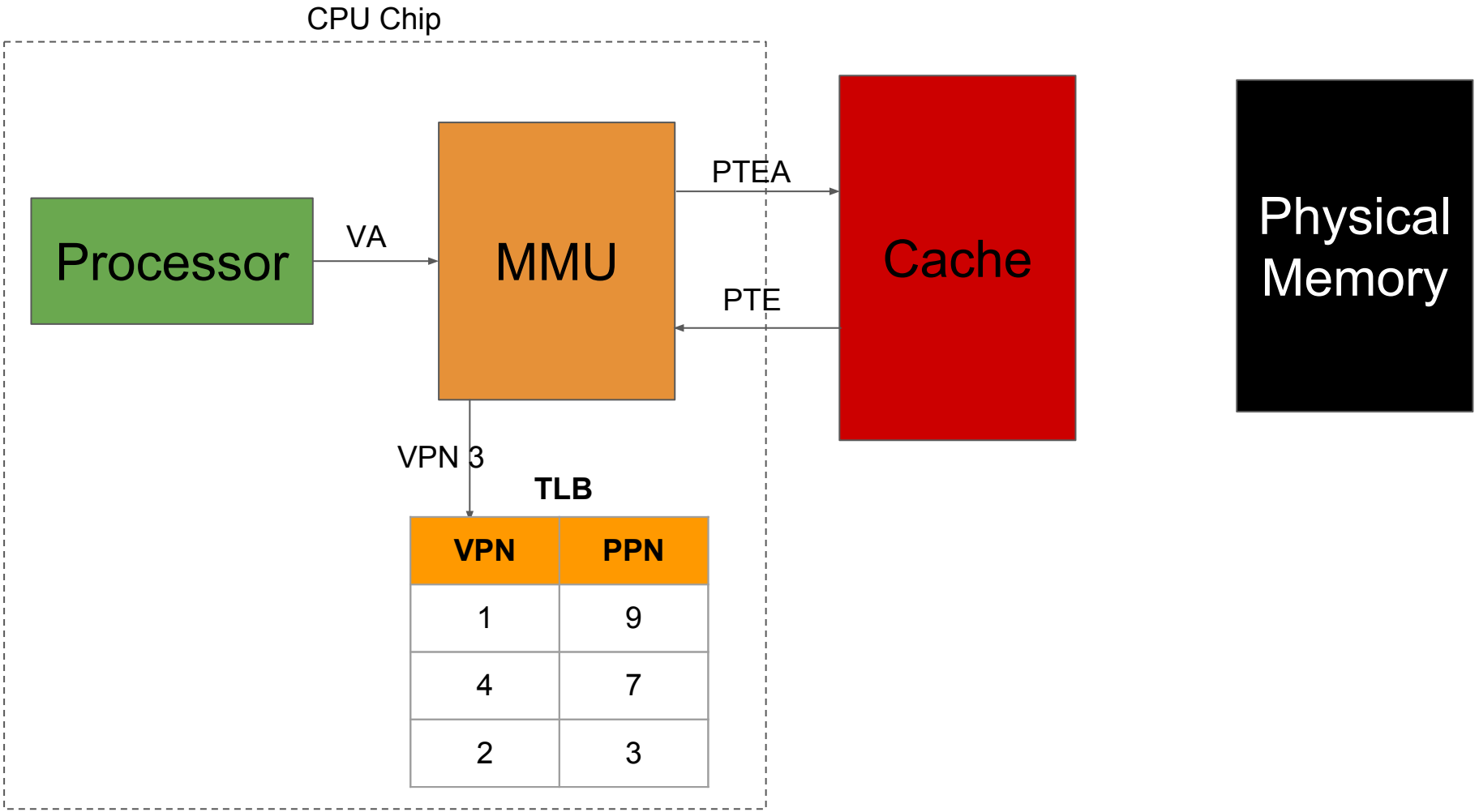
CPU Chip
Processor
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MMU
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PTE
Cache
Physical Memory
VPN 3
TLB
VPN
PPN
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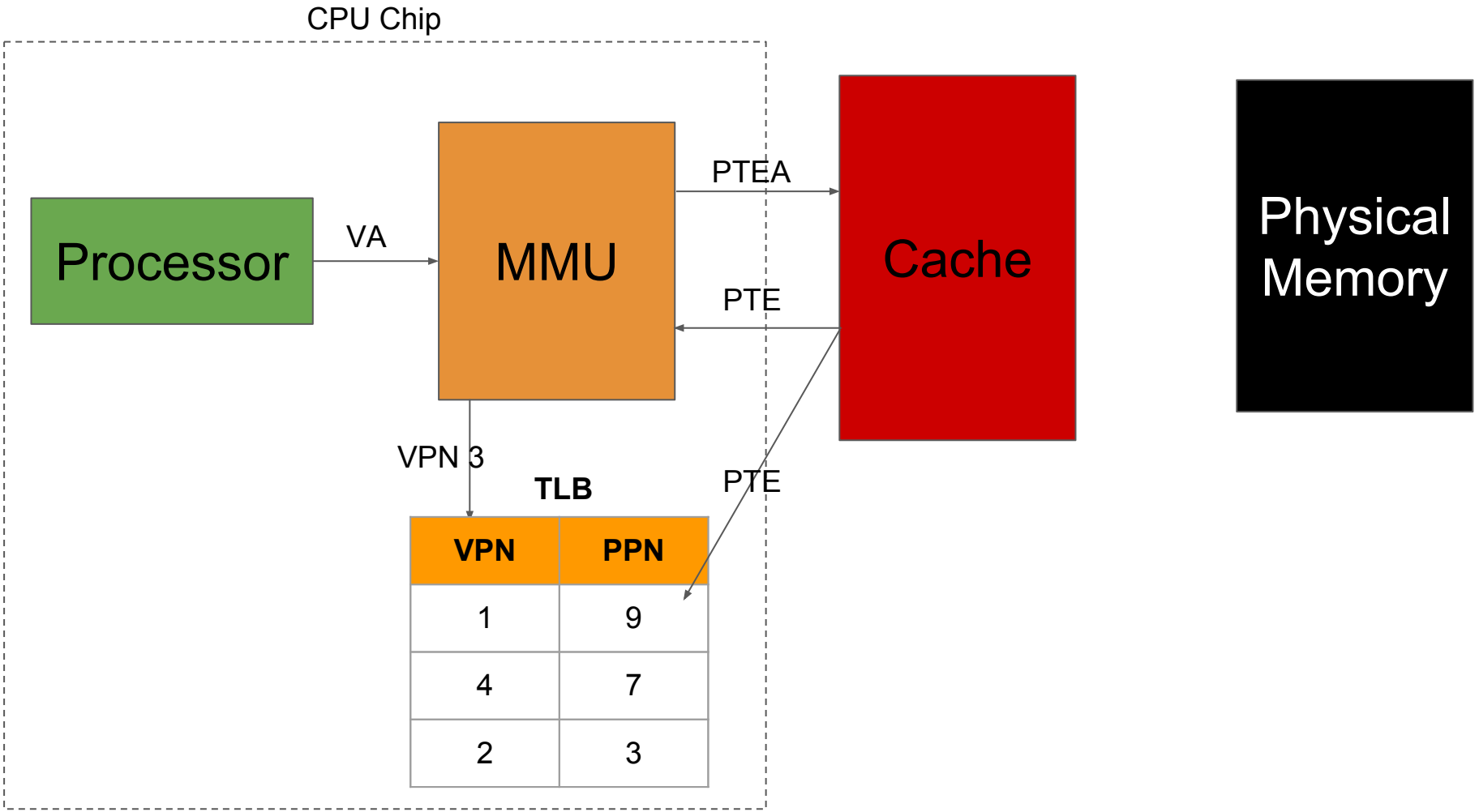
3


CPU Chip
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PTE
Cache
Physical Memory
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VPN
PPN
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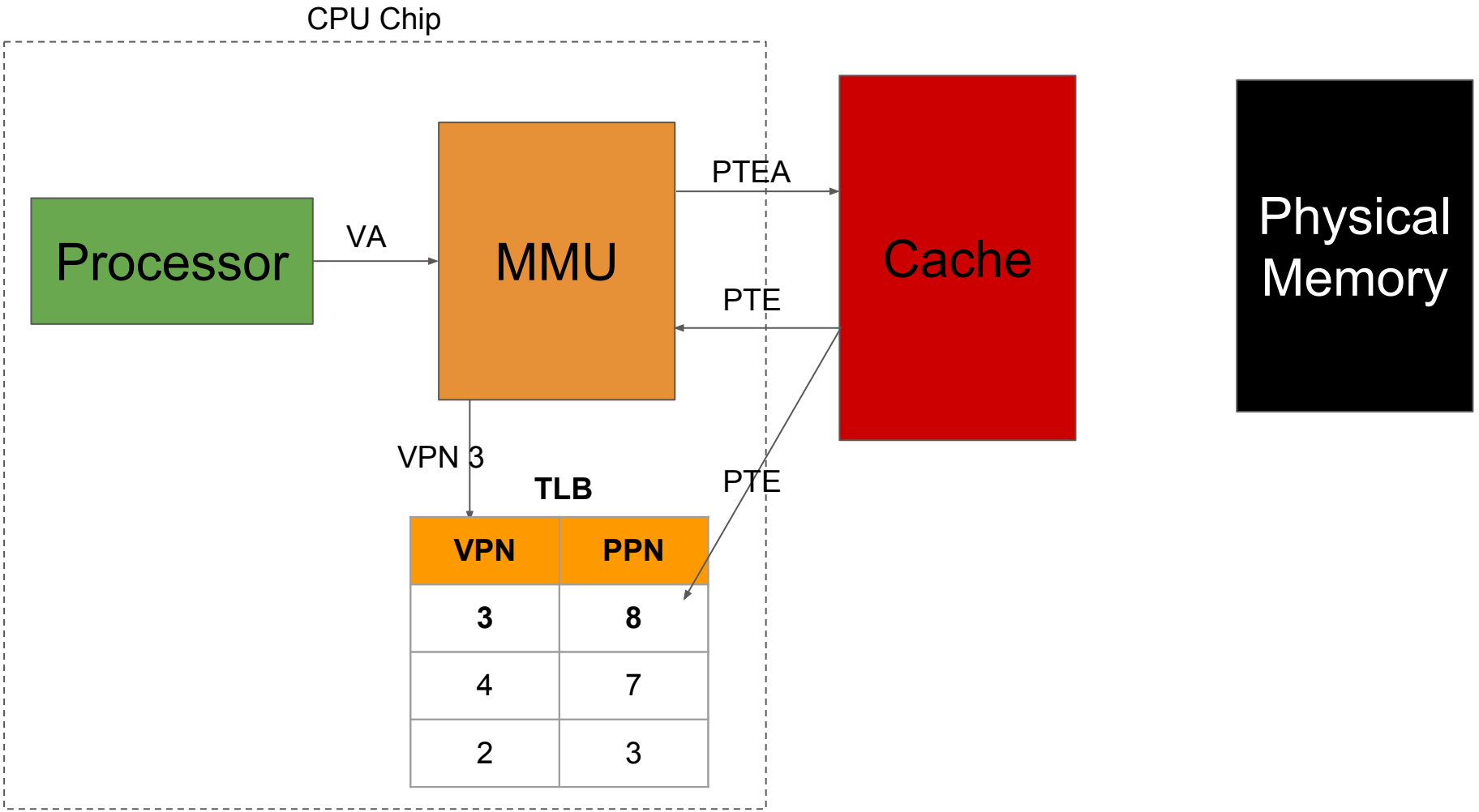
CPU Chip
Processor
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MMU
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PTE
Cache
Physical Memory
VPN 3
TLB
PTE
VPN
PPN
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8
4
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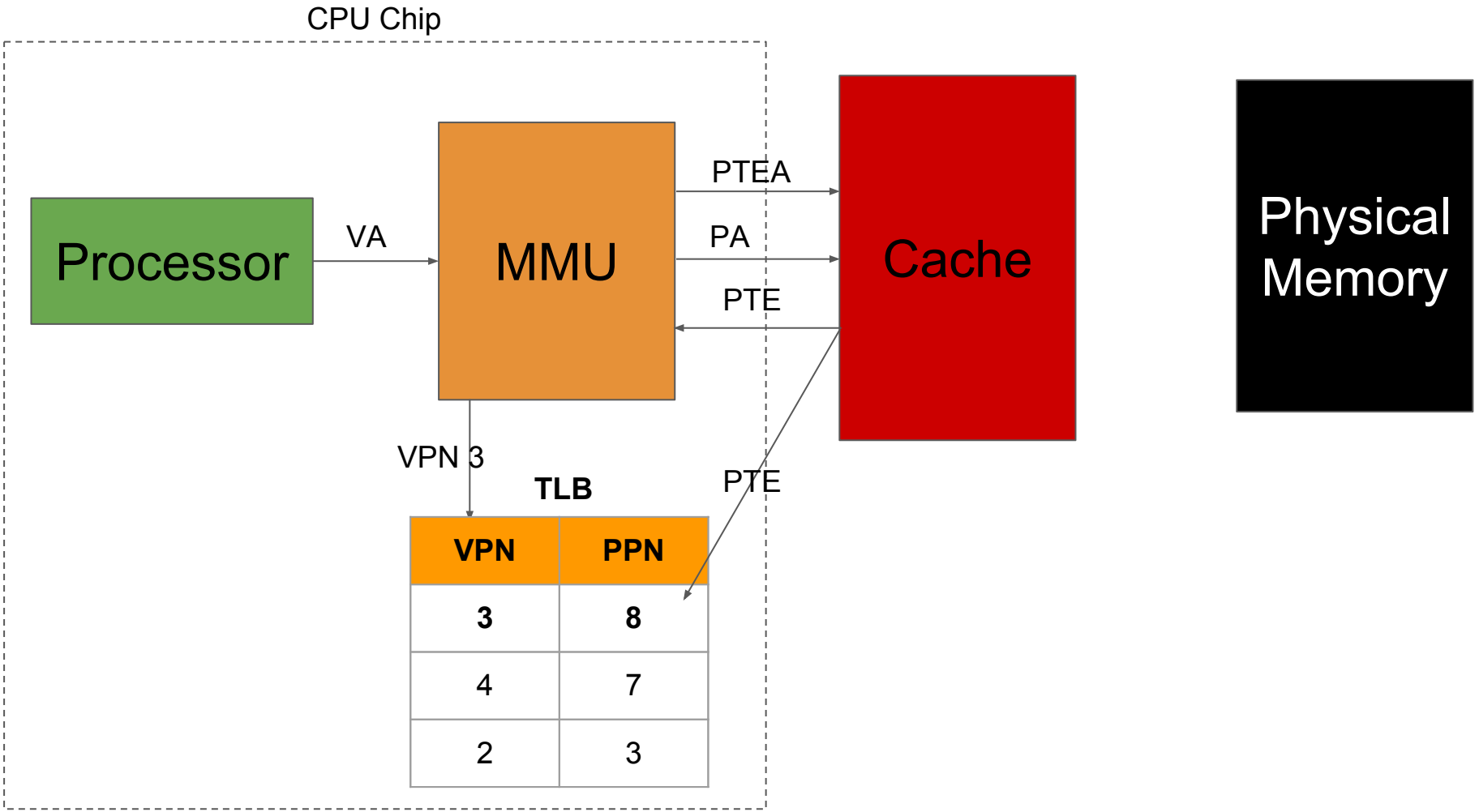
CPU Chip
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TLB
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VPN
PPN
3
8
4
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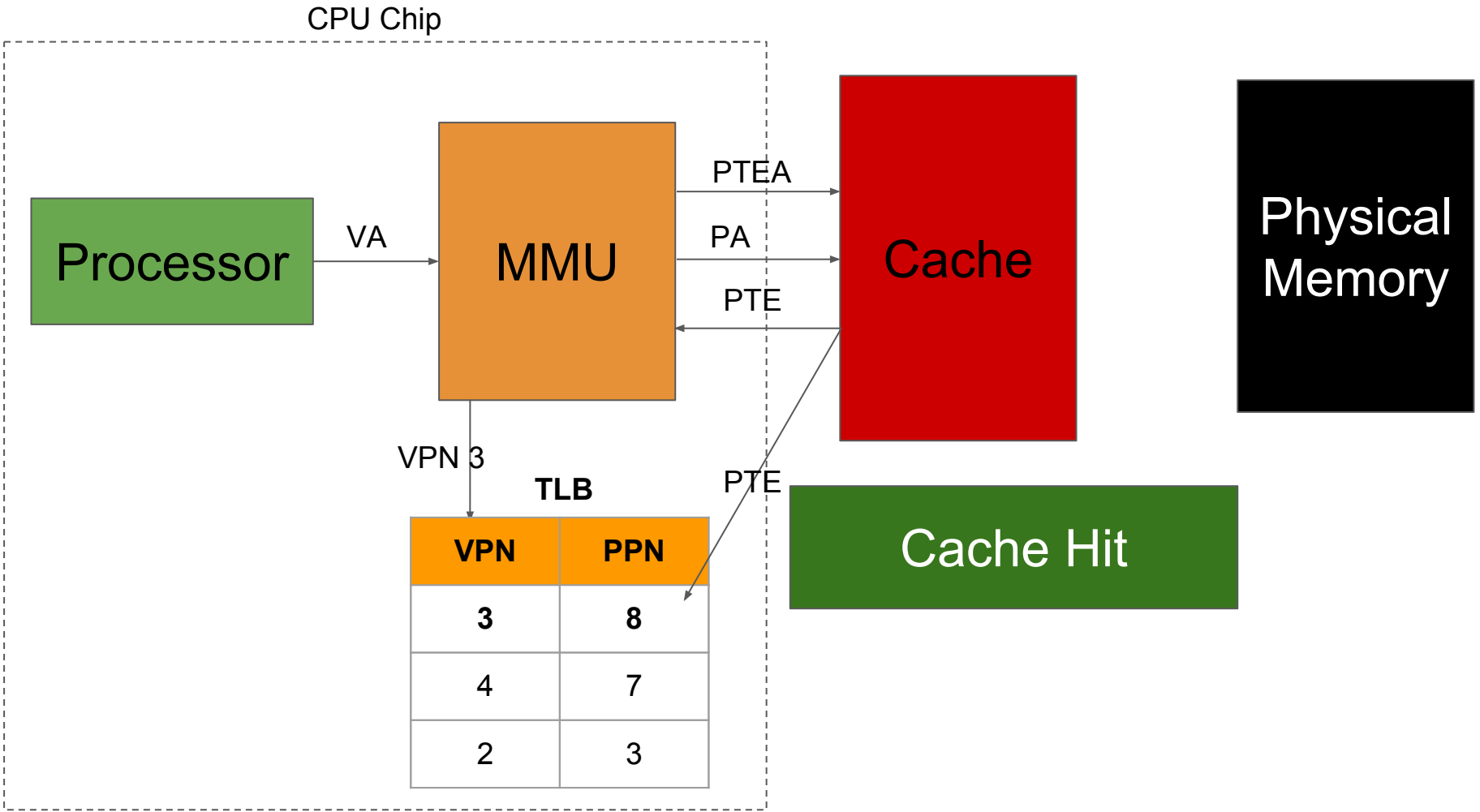
CPU Chip
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VA
MMU
PTEA
PA
PTE
Cache
Physical Memory
VPN 3
TLB
PTE
Cache Hit
VPN
PPN
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8
4
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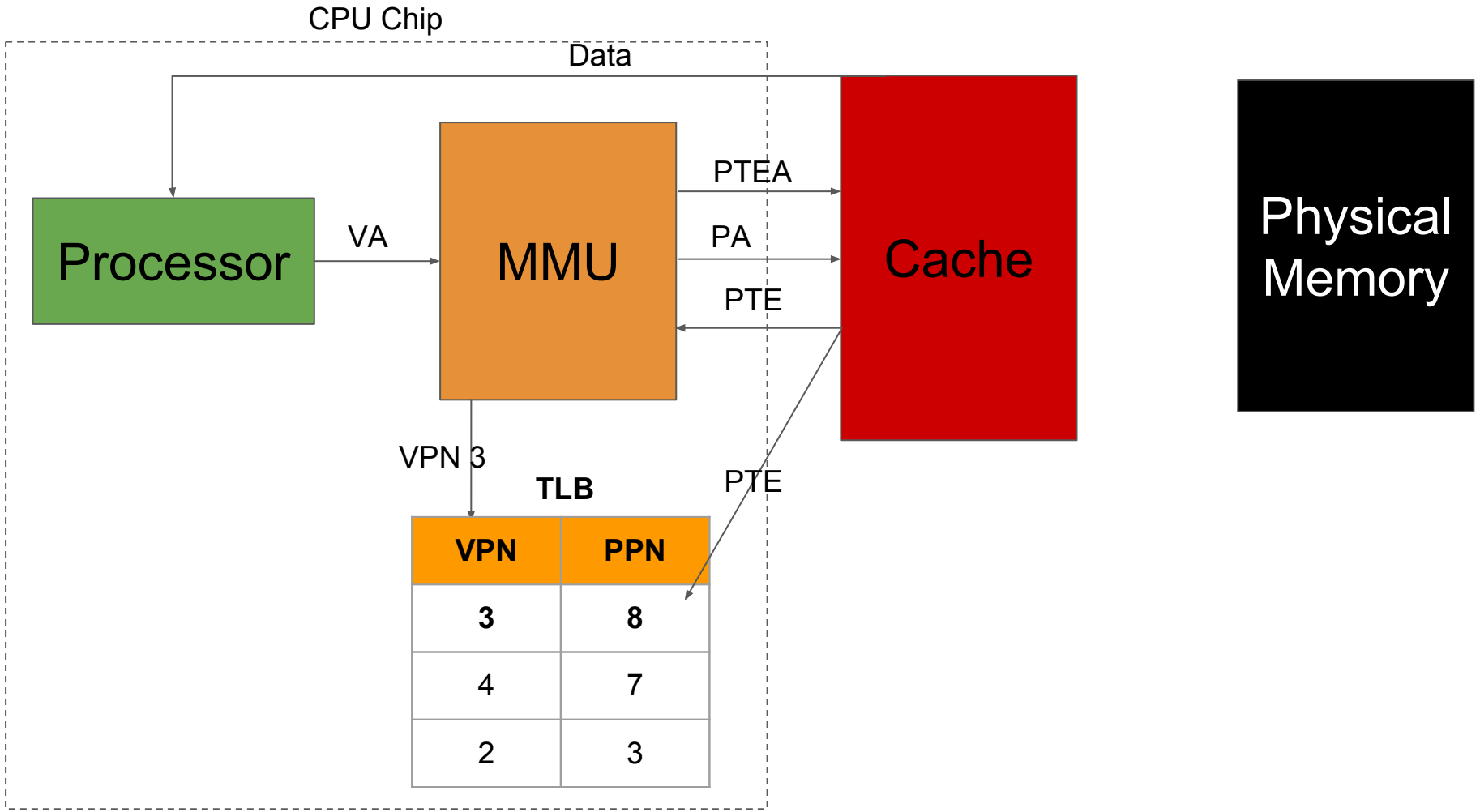

CPU Chip
Data
Processor
VA
MMU
PTEA
PA
PTE
Cache
Physical Memory
VPN 3
TLB
PTE
VPN
PPN
3
8
4
7
2
3

The devil is in the details!

Virtual Address

4-bit Virtual Address

4-bit Virtual Address

Total Number of Virtual Pages = 4

4-bit Virtual Address

Virtual Page Size = 4 bytes

Physical Address

3-bit Physical Address

3-bit Physical Address

Total Number of Physical Pages = 2

3-bit Physical Address

Physical Page Size = 4 bytes

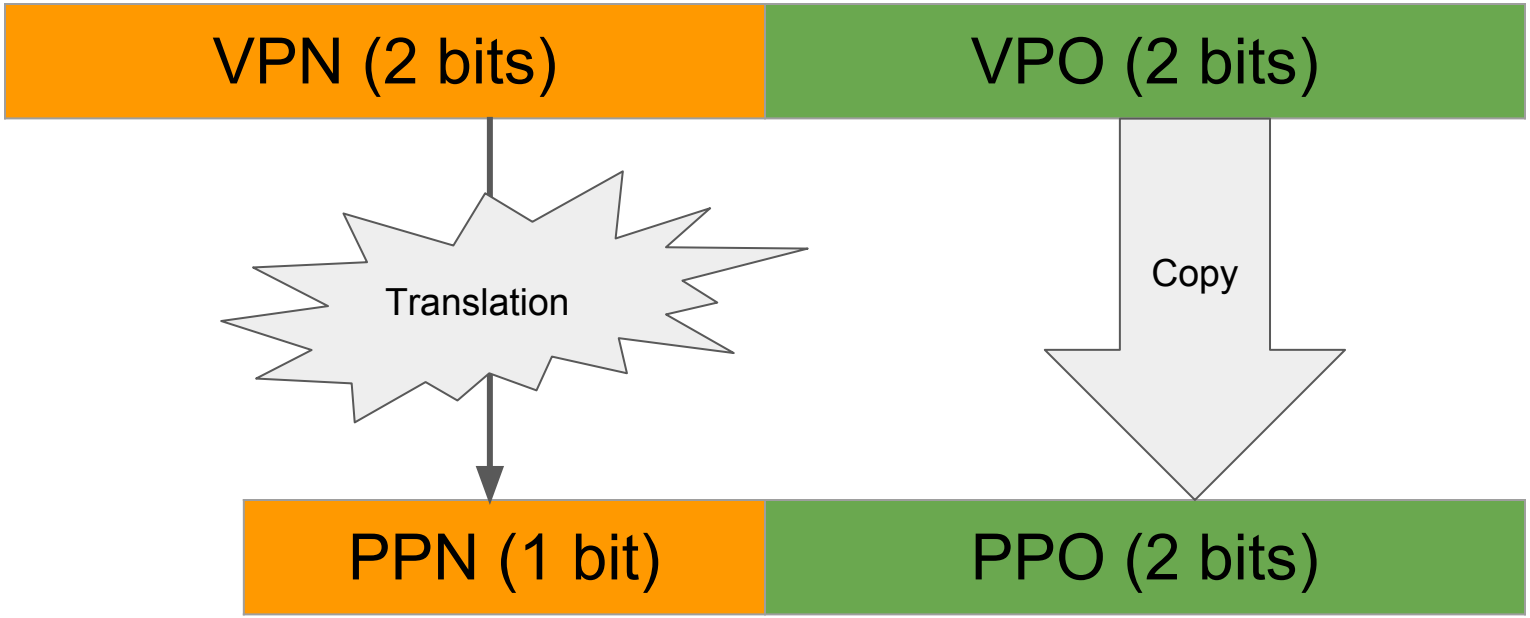
Page Size

Virtual Page Size = Physical Page Size = 4 bytes

Page Offset

Virtual Page Offset (VPO) = Physical Page Offset (PPO)

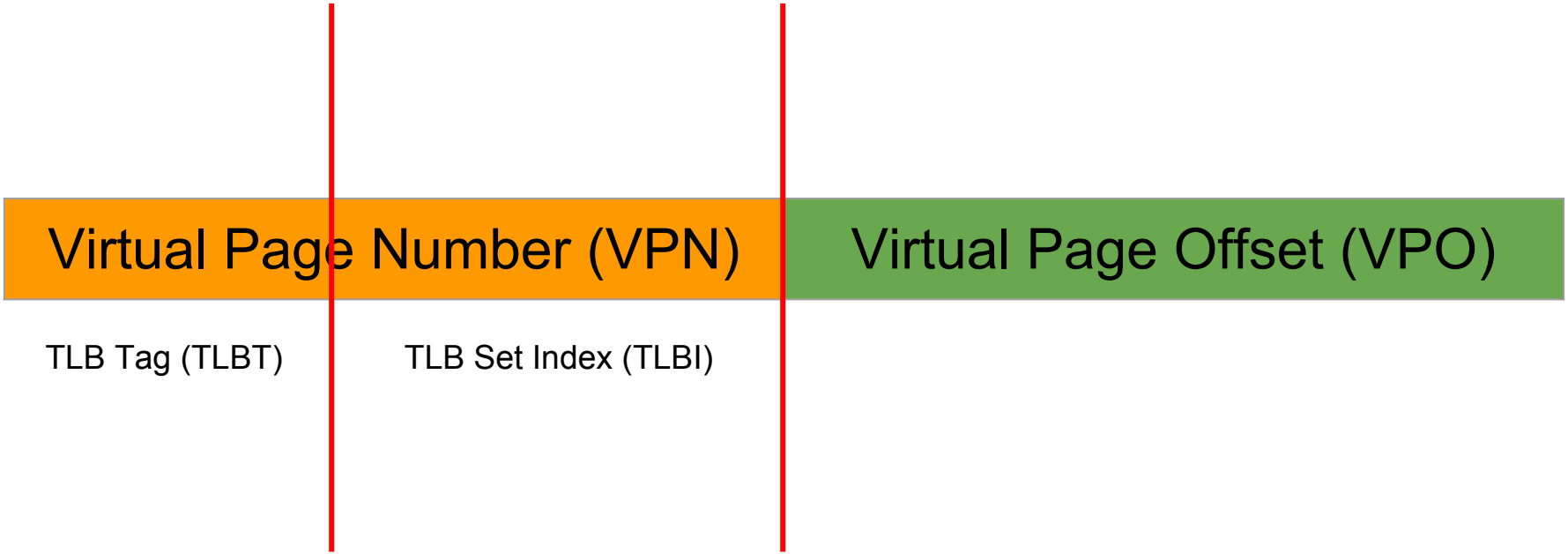
Address Translation



Virtual Address

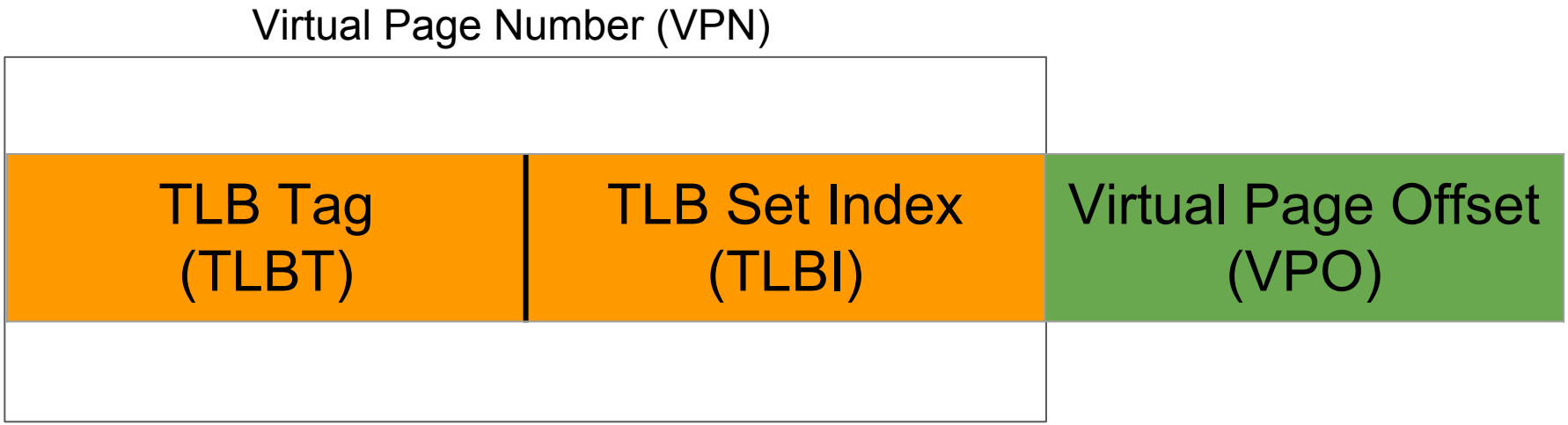
Accessing the TLB

Accessing the TLB



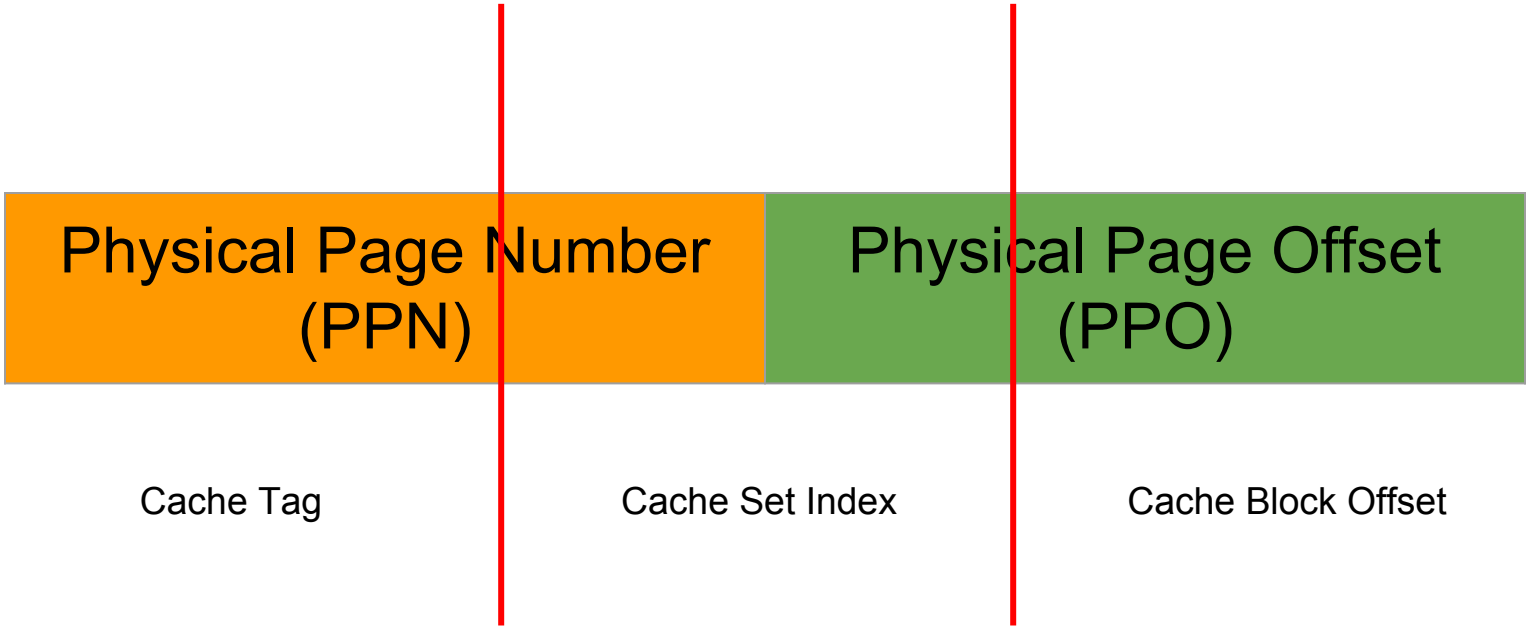
Accessing the TLB

Accessing the TLB



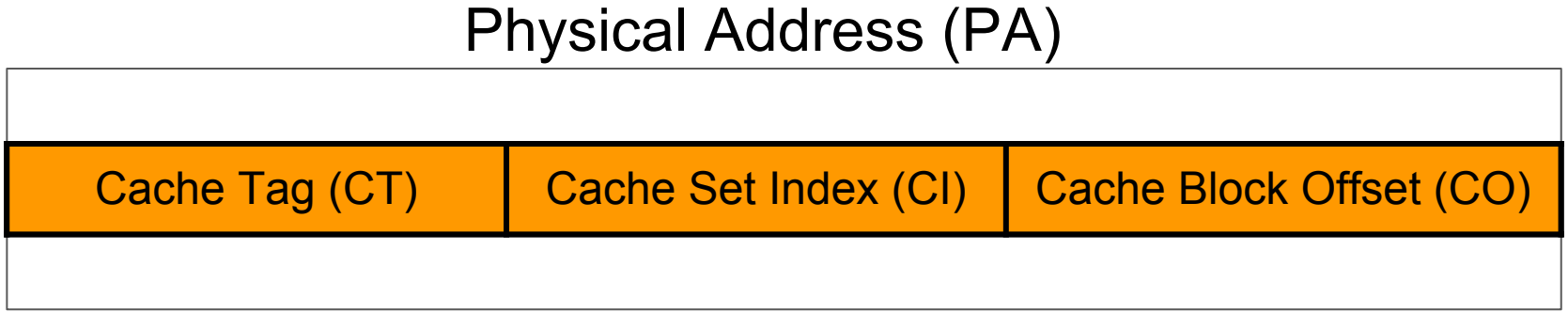
Physical Address

Accessing the Cache



Accessing the Cache

Accessing the Cache



End-to-end Address Translation

1. The memory is byte addressable
2. Memory accesses are to **1-byte words** (not 4-byte words)
3. Virtual addresses are **14 bits wide** (n = 14)
4. Physical addresses are **12 bits wide** (m = 12)
5. The page size is **64 bytes** (P = 64)
6. The TLB is **4-way set associative** with 16 total entries
7. The L1 d-cache is physically addressed and direct mapped, with a 4-byte line size and 16 total sets.

In-class Worksheet!