"caches"  \[\frac{\text{Review}}{\text{caching}}\]

\[K: \rightarrow \text{cache.}\]

\[K+1: \quad \]

Cache hit

Cache miss

1. cold miss
2. conflict miss
3. capacity miss

\[\text{workingset} \quad \overset{b \cdot 10^{-1.4}}{\longrightarrow} \quad \text{cache sat.}\]
Replacement policies

LRU.

Block = group of words

Word = """" bytes

⇒ Block = group of bytes
Cache Organization

CPU cache

Main Memory

L1

H/W device

32-bit system

Addr = 32-bits

Total addr = \( \frac{2^{32}}{2^2 \times 2^{30}} \) = 2

\( b_3 \quad b_2 \quad b_1 \quad b_0 \)

if addr bits = 4

\( \Rightarrow \) Total addr = \( 2^4 \) = 16
1. Sets

\( S_0 \)

\( \vdots \)

\( S_3 \)

Set index bits

\[ s = 2^s = 4 \]

2. Cache Lines

\( S_0 \)

\( \vdots \)

\( S_3 \)
No. of Cache lines \((E)\) / set.

\[
E = \text{no. of cache lines / set.}
\]

3. **Cache block**

![Diagram of cache block with 4 bytes highlighted]
If $b = 3$,

\[
\Rightarrow \quad \text{you can have } 8 \text{ bytes in a block.}
\]

No. of bytes in a block in a cache line 

\[
(B) = 2^b
\]
Valid bit

K

K+1

write
\[ S = 2^s \]
\[ E = \text{no. of cache lines} \]
\[ B = 2^b \]

no. of bytes in a block

Valid Tag

\( S_0 \)

\( 1 \)

\( 0 \)

\( S_1 \)
<table>
<thead>
<tr>
<th>Addr (decimal)</th>
<th>Tag</th>
<th>Set index</th>
<th>byte offset</th>
<th>Block no.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>1</td>
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<td>1</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3</td>
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<td>0</td>
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<td>1</td>
<td>3</td>
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<td>7</td>
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<tr>
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<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
</tbody>
</table>
\[ S = 2^2 = 4 \]
\[ B = 2^1 = 2 \]
\[ E = 1 \]

\[ \Rightarrow 1 \text{ cache line.} \]

<table>
<thead>
<tr>
<th>Valid</th>
<th>Tag</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>m[0]</td>
<td>m[1]</td>
</tr>
</tbody>
</table>

\[ \Rightarrow 1 \text{ cache} \]