

CS 537: Intro to Operating Systems (Fall 2017)

Worksheet 4 - Memory Virtualization

Due: Oct 4th 2017 (Wed) in-class OR email to Simmi before 11:59 pm

1. Simple Paging

Assume a system with a simple linear page table with the following parameters:

- Size of virtual address space = 512 bytes
- Size of physical memory = 1024 bytes
- Page size = 64 bytes
- Size of page table entry (PTE) = 1 byte
- Value of page table base register (PTBR) = 0x1d0

The left most bit (MSB) in the PTE is the valid bit and it determines if the virtual page is valid or not (1 = valid page; 0 = invalid page). The 4 right most bits (LSBs) in a PTE contains the physical frame number (PFN). You may assume that all the other bits are unused. The contents of the page table are shown below.

Entry 0	0x85
Entry 1	0x8a
Entry 2	0x7c
Entry 3	0x57
Entry 4	0x08
Entry 5	0x89
Entry 6	0x23
Entry 7	0x8d

The instruction below loads a single byte from virtual address 372 into the register %eax. This instruction resides at virtual address 24 within the address space of the process

24: mov 372, %eax

In the diagram of **physical memory**, where each number (in hex) represents a physical address, shown on the next page:

- Put a **BOX** around the **page table** and label it.
- Put a **BOX** around each **valid virtual page** and label them.
- CIRCLE** the memory addresses that get referenced during the execution of the instruction, including both the instruction fetch and data access. Remember to include the memory references to the PTEs in the page table too!
- LABEL** the memory address (that you circled) with a **NUMBER** that indicates the **ORDER** in which various physical addresses get referenced.

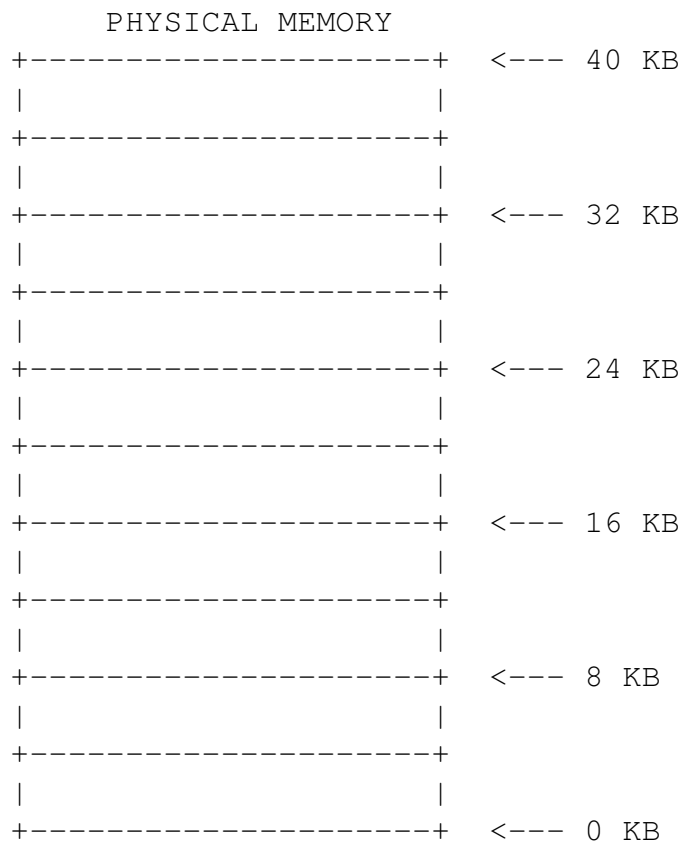
000 001 002 003 004 005 006 007 008 009 00a 00b 00c 00d 00e 00f
010 011 012 013 014 015 016 017 018 019 01a 01b 01c 01d 01e 01f
020 021 022 023 024 025 026 027 028 029 02a 02b 02c 02d 02e 02f
030 031 032 033 034 035 036 037 038 039 03a 03b 03c 03d 03e 03f
040 041 042 043 044 045 046 047 048 049 04a 04b 04c 04d 04e 04f
050 051 052 053 054 055 056 057 058 059 05a 05b 05c 05d 05e 05f
060 061 062 063 064 065 066 067 068 069 06a 06b 06c 06d 06e 06f
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0c0 0c1 0c2 0c3 0c4 0c5 0c6 0c7 0c8 0c9 0ca 0cb 0cc 0cd 0ce 0cf
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1c0 1c1 1c2 1c3 1c4 1c5 1c6 1c7 1c8 1c9 1ca 1cb 1cc 1cd 1ce 1cf
1d0 1d1 1d2 1d3 1d4 1d5 1d6 1d7 1d8 1d9 1da 1db 1dc 1dd 1de 1df
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3d0 3d1 3d2 3d3 3d4 3d5 3d6 3d7 3d8 3d9 3da 3db 3dc 3dd 3de 3df
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3f0 3f1 3f2 3f3 3f4 3f5 3f6 3f7 3f8 3f9 3fa 3fb 3fc 3fd 3fe 3ff

2. Segmentation

Assume a system that uses **segmented virtual memory**. There are **three segments**, namely code, heap, and stack. Note that the code and the heap grow towards high addresses while the stack grows towards low addresses. The size of the **virtual address space is 16KB**, and the size of the **physical address space is 40KB**. The top **three bits (MSBs)** in the virtual address are used to identify the segment. 000 and 001 for code; 010, 011 and 100 for heap; 110 and 111 for stack. The value of the **bounds register for code, heap, and stack** are **2KB, 4KB, and 3KB** respectively.

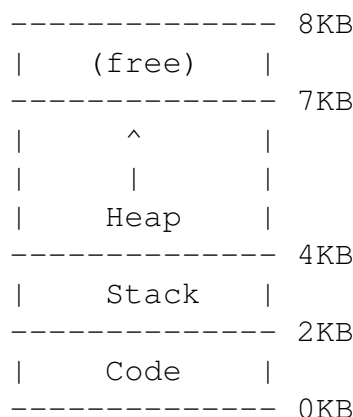
Given the following virtual to physical address translations, sketch the **physical memory** layout below. You should **mark the locations** in physical memory where the three segments, namely code, heap, and stack are placed. You should also label the **start** and **end** addresses (in decimal) of the three segments in physical memory.

Virtual Address	Physical Address
6 KB	34 KB
0 KB	8 KB
14 KB	30 KB



3. Base and Bounds

Consider a machine that uses the **base and bounds technique** for memory virtualization and a slightly **different address space** as shown below. Note that the **stack** is of fixed size and it immediately follows the code section. The heap starts at the end of the stack and grows upward. In this configuration, there is only one direction of growth, towards higher regions of the address space. The figure below is NOT drawn to scale.



Parameters:

Size of the virtual address space = 8KB, size of the physical memory = 32KB, base register = 16KB, and bounds register = 7KB. References to any address within the bounds would be considered legal; references above this value are out of bounds and thus the hardware would raise an exception.

- For each **virtual address**, either write down the **physical address** it translates to OR write down that it is a **segmentation fault** (an out-of-bounds address).

Virtual Address	Physical Address (in hex or decimal) OR Seg Fault
0x1000 (decimal: 4096)	
0x1C00 (decimal: 7168)	
0x0000 (decimal: 0)	
0x2000 (decimal: 8192)	
0x0800 (decimal: 2048)	

- For each physical address, write the corresponding virtual address (in hex or decimal), and the logical segment (code, stack, heap) that the virtual address belongs to.

Physical Address	Virtual Address	Segment
0x5800 (decimal: 22KB)		
0x4400 (decimal: 17KB)		
0x4C00 (decimal: 19KB)		