CS 537-Intro to Operating Systems

Worksheet 2 - Simple Paging

July 6, 2017

Assume a system with a simple linear page table.

Parameters:

- virtual address space size = 128 bytes
- page size = 32 bytes
- physical memory size = 256 bytes
- Size of one Page Table Entry (PTE) = 1 byte
- Value of Page Table Base Register (PTBR) = 8

The **left most bit (MSB)** in a PTE is the **valid** bit and it determines if the virtual page is valid or not. The **3 right most bits (LSBs)** in a PTE contains the **Physical Frame Number (PFN)**. You may assume that all the other bits are unused. The contents of the Page Table are shown below.

Page Table (from entry 0 down to the max size)

0x81
0x00
0x87
0x03

The instruction below loads a **single byte** from virtual address 72 into the register %eax. This instruction resides at virtual address 16 within the address space of the process.

16: mov 72, %eax

In the diagram of physical memory shown on the next page:

1. Put a **BOX** around the **page table** and label it.
2. Put a **BOX** around each **valid virtual page** (and label them).
3. **CIRCLE** the memory addresses that get referenced during the execution of the instruction, including both instruction fetch and data access (assume there is no TLB).
4. **LABEL** the memory addresses (that you circled) with a **NUMBER** that indicates the **ORDER** in which various physical addresses get referenced.

Physical Memory

0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55
56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87
88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103
104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127
128	129	130	131	132	133	134	135
136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151
152	153	154	155	156	157	158	159
160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175
176	177	178	179	180	181	182	183
184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199
200	201	202	203	204	205	206	207
208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223
224	225	226	227	228	229	230	231
232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247
248	249	250	251	252	253	254	255

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Page Table (from entry 0 down to the max size)

0	0x81
1	0x00
2	0x87
3	0x03

4 bytes

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16: mov 72, %eax

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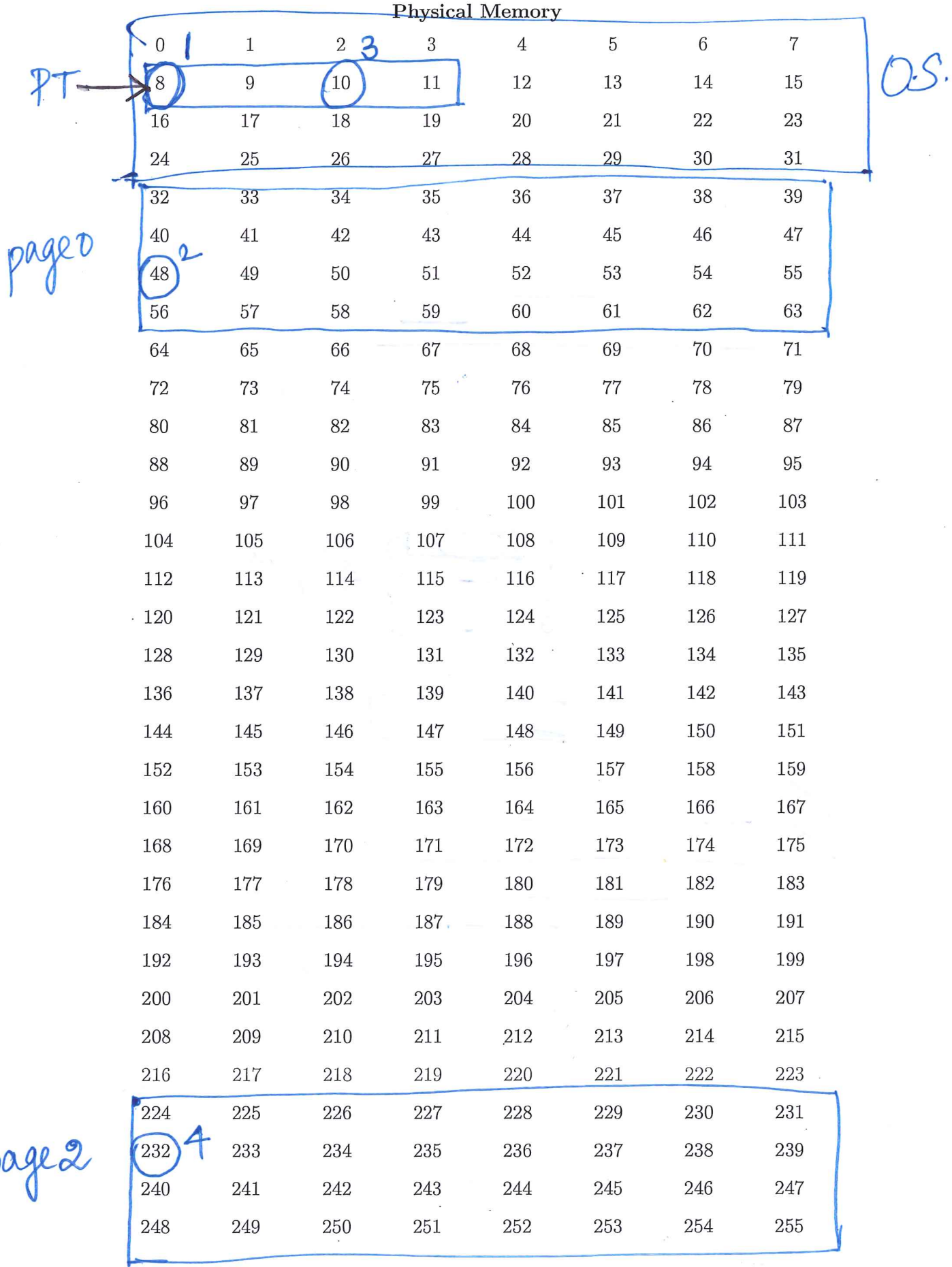
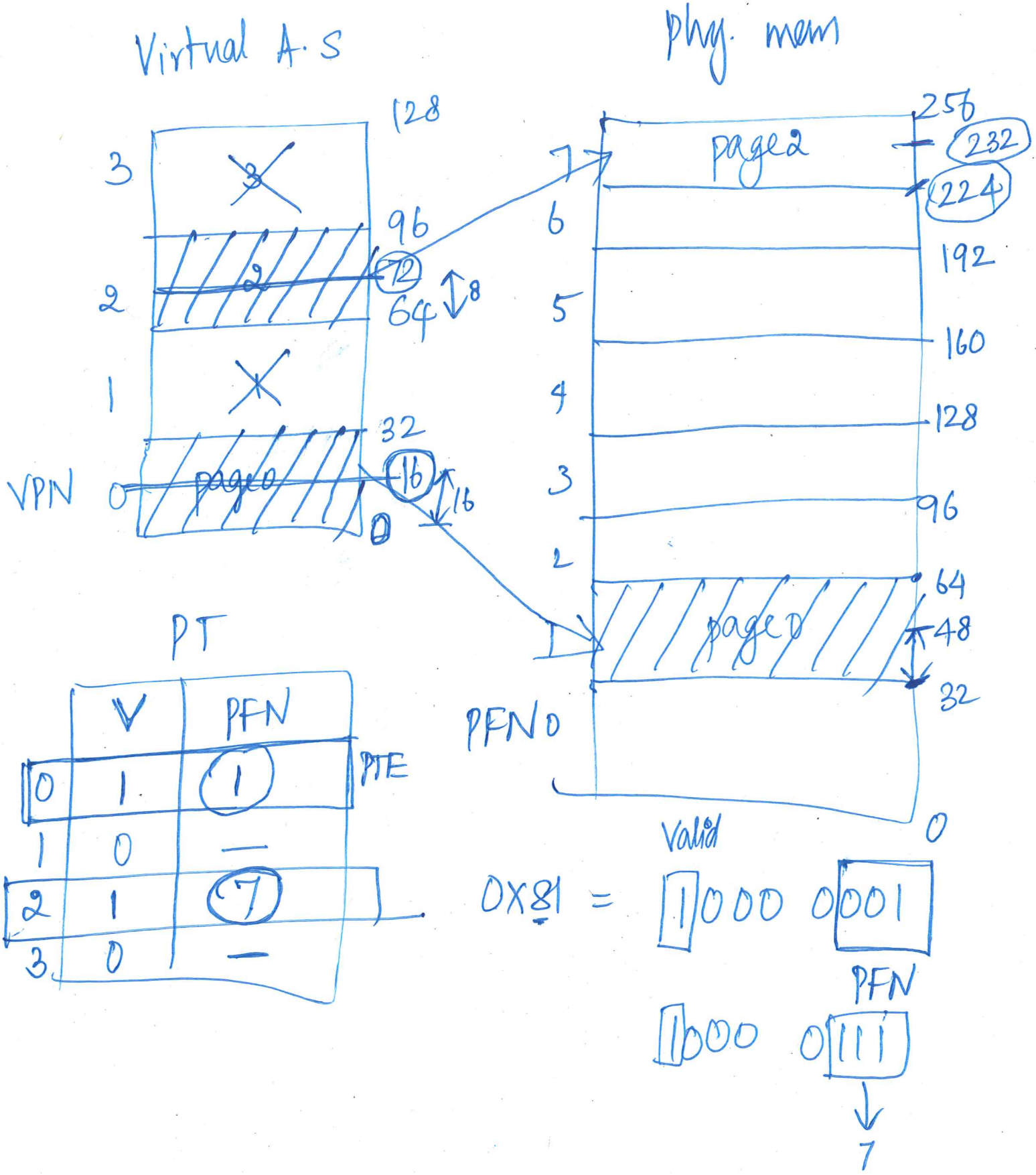
80	81	82	83	84	85	86	87
88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103
104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127
128	129	130	131	132	133	134	135
136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151
152	153	154	155	156	157	158	159
160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175
176	177	178	179	180	181	182	183
184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199
200	201	202	203	204	205	206	207
208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223
224	225	226	227	228	229	230	231
232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247
248	249	250	251	252	253	254	255




Virtual A.S
Phy. mem
128
3
96
2
64
8
1
32
VPN
0
page0
16
0
16
PT
V
PFN
PTE
0
1
1
1
0
—
2
1
7
3
0
—
256
page2
232
224
6
192
5
160
4
128
3
96
2
64
page1
48
32
PFN 0
Valid
0
0X81 = 1000 0001
PFN
1000 0111
7