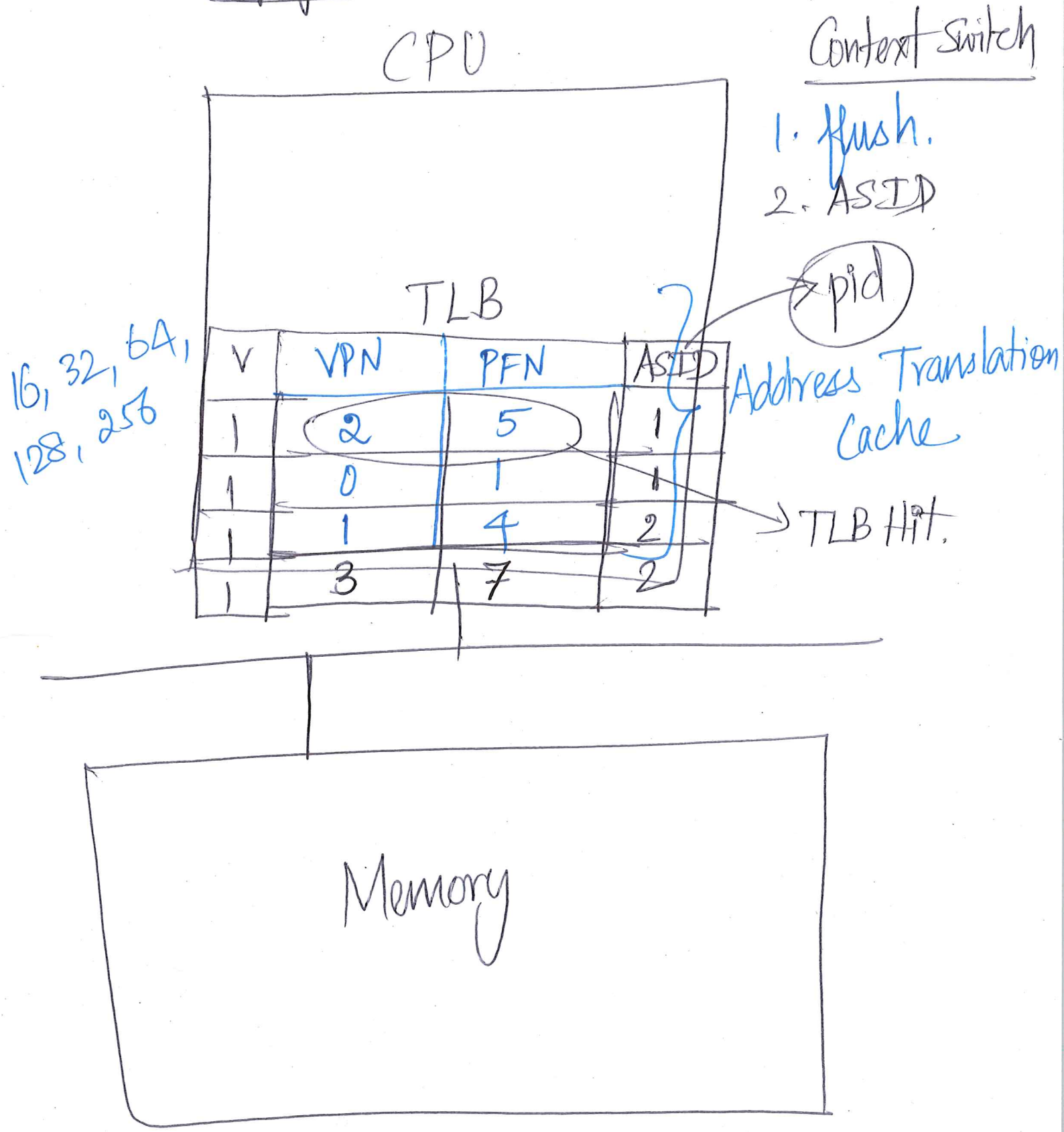
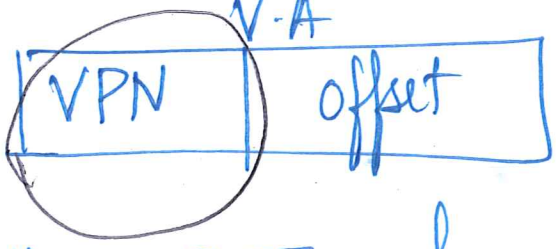
Paging : Faster Translations



H/W: steps on each mem. ref (WITHOUT TLB).

1. extract VPN from the V.A.



2. Get the PTE from the PT.

PTEAddr = PTBR + VPN * sizeof(PTE)

3. Access Memory (PTE) EXPENSIVE

4. Get the PFN from PTE.

5. ~~Ca~~ Form the PA = PFN + offset.

6. Reg ⇐ Access Memory (PA)

H/W: on each mem. ref w/ TLB

1. extract VPN from the V.A.
2. Lookup TLB to see if the entry for VPN is present in the TLB.
3. if yes [TLB Hit]
   - get the PFN from the TLB.
   - form the PA.
   - Access Memory (PA)
4. if NO [TLB Miss]
   - get the PTE from the PT. Memory Access
   - updated the TLB with the PTE.
   - retry the instr. again!

~~int num = x;~~ mov 80, %eax.

H/W | OS-managed TLB | OS

1. same

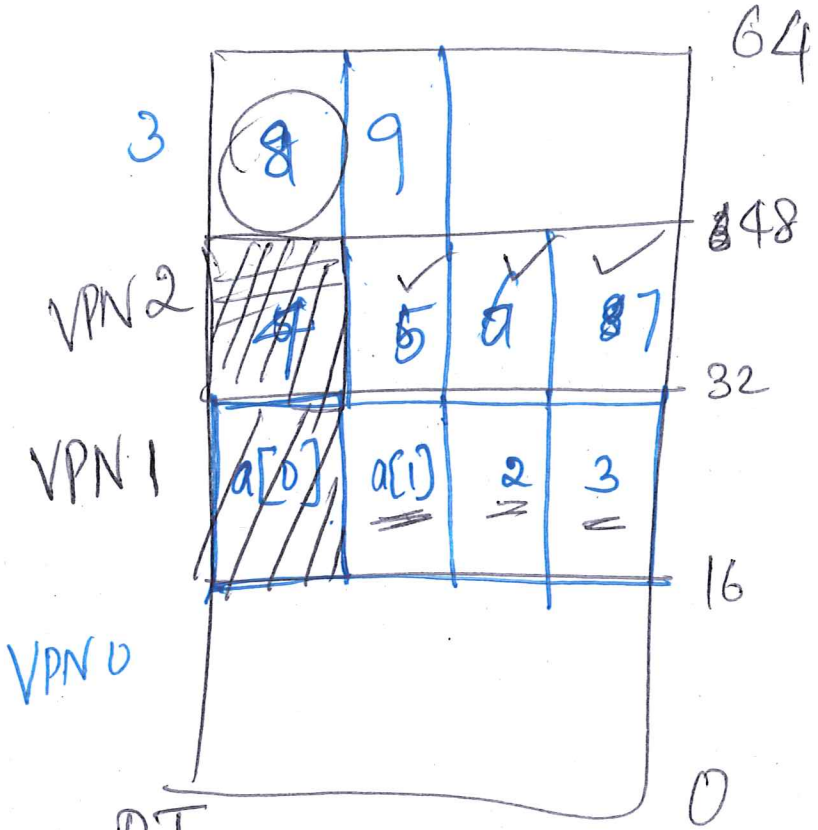
2. same

3. same.

4. if NO [TLB Miss]
raise (TLB Miss Exception)

TRAP

1. runs the TLB Miss exception handler
- get PTE from PT.
- updates the TLB w/ this translation. using special instr. privileged instr.
- retries the ~~current~~ instruction



int array [10];

↳ 4 bytes

PT

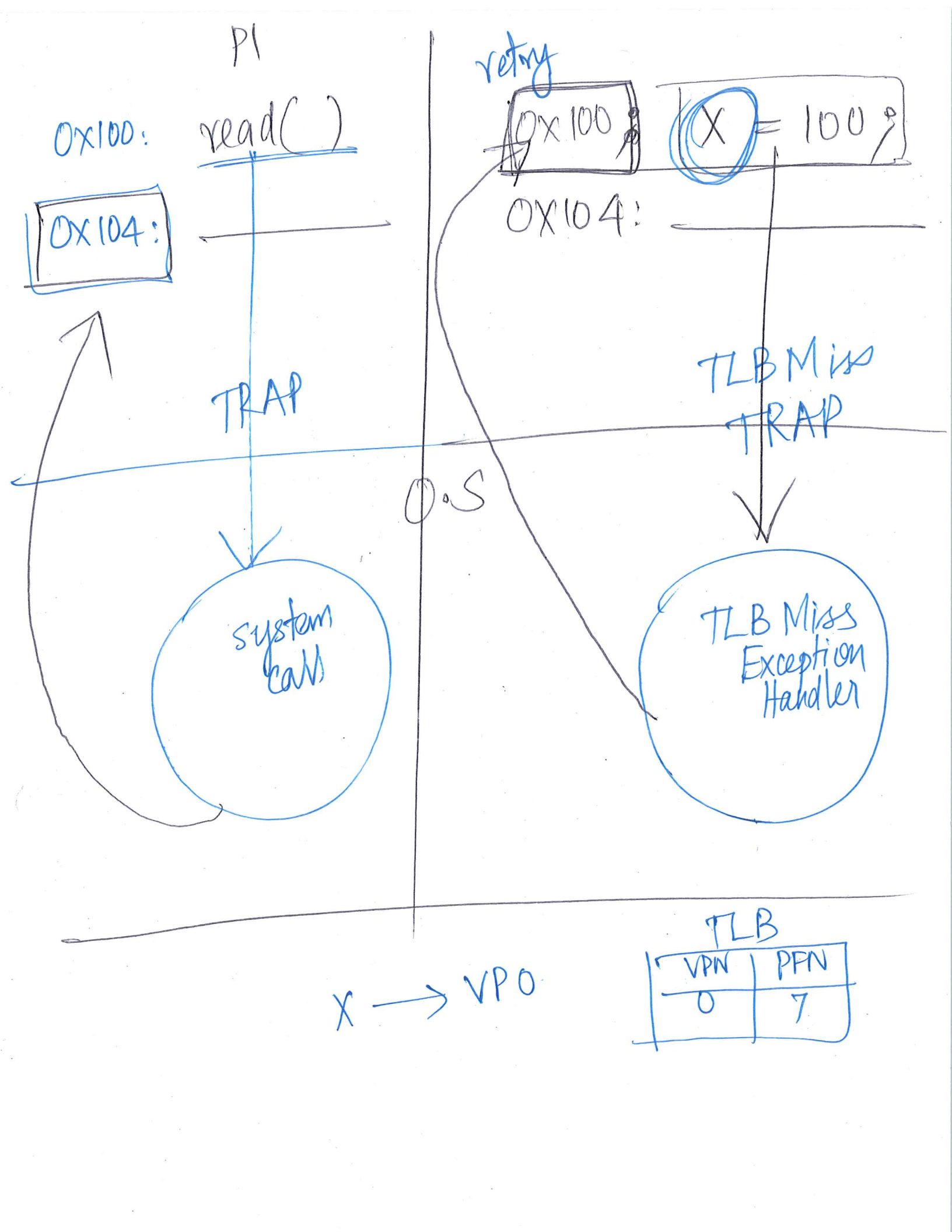
VPN	PFN
0	3
1	2
2	1
3	7

TLB

VPN	PFN
1	2
2	1
3	7

m h h h m h h h m h

hit rate = 70%


P1
0x100:
read( )
0x104:
TRAP
system call
retry
0x100;
X = 100;
0x104:
TLB Miss
TRAP
TLB Miss Exception Handler
O.S
X → VPO
TLB
VPN
PFN
0
7