Problem 1: how many physical loads for each instruction?

Assume 256-byte pages.
Assume 16-bit addresses.
Assume ASID of current process is 211.
Assume this TLB state:

<table>
<thead>
<tr>
<th>ASID</th>
<th>VPN</th>
<th>PFN</th>
<th>valid</th>
<th>Prot</th>
</tr>
</thead>
<tbody>
<tr>
<td>211</td>
<td>0xBB</td>
<td>0x91</td>
<td>1</td>
<td>???</td>
</tr>
<tr>
<td>211</td>
<td>0xFF</td>
<td>0x23</td>
<td>1</td>
<td>???</td>
</tr>
<tr>
<td>112</td>
<td>0x05</td>
<td>0x91</td>
<td>1</td>
<td>???</td>
</tr>
<tr>
<td>211</td>
<td>0x05</td>
<td>0x12</td>
<td>0</td>
<td>???</td>
</tr>
</tbody>
</table>

How many physical accesses are needed for each instruction?
Consider each instruction independently (e.g., for "b", don't worry how "a" changes the TLB).
(a) 0xAA10: movl 0x1111, %edi 4
(b) 0xBB13: addl $0x3, %edi 1
(c) 0x0510:movl %edi, 0xFF10 3

Other questions:
(d) why do two entries map to the same physical page, 0x91? probably shared code
(e) what do the "prot" bits probably contain for the first TLB entry? r-X
(f) would accessing 0x0500 cause a segfault? (assume ASID 211 still) don't know
(g) which fields in the TLB would also appear in a PT? Do any have a different meaning?

Problem 2: how large must PTE's be?

(a) Phys addr space contains 1024 pages. 7 bits needed for extras (prot, valid, etc.): \( \log(1024) + 7 = 17 \) bits
(b) Phys addr are 16-bits, pages are 32 bytes, 8 bits needed for extras 16 - \( \log(32) \) + 8 = 11
(c) Phys addr space is 4 GB, pages are 4 KB, 6 bits needed for extras 26 - 12

Problem 3 how large is the page table?

(a) PTE's are 3 bytes, and there are 32 possible virtual page numbers 96 bytes
(b) PTE's are 3 bytes, virtual addrs are 24 bits, and pages are 16 bytes 3 MB
(c) PTE's are 4 bytes, virtual addrs are 32 bits, and pages are 4 KB 4 MB
(d) PTE's are 4 bytes, virtual addrs are 64 bits, and pages are 4 KB 4 \( 2^{54-12} \) = 256 PB
(e) assume each PTE is 10 bits. We cut the size of pages in half, keeping everything else fixed, including size of virt/phys addresses. By what factor does the PT increase in size?
\[ 2 \times \]

Problem 4: how large should pages be?

(a) Goal PT size is 512 bytes. PTE's are 4 bytes. Virtual addrs are 16 bits. \( \frac{512}{4} = 128 \Rightarrow P = 128 \) bytes
(b) Goal PT size is 1 KB. PTE's are 4 bytes. Virtual addrs are 16 bits. \( \frac{1024}{4} = 256 \Rightarrow P = 256 \) byte
(c) Goal PT size is 4 KB. PTE's are 4 bytes. Virtual addrs are 32 bits. \( \frac{1024}{4} = 256 \Rightarrow P = 4 \) MB
Problem 5: translate with segments over page tables

Translate the following (refer to slides):
(a) 0x12FFF => \(04\ FFE\)
(b) 0x10FFF => \(22\ FFE\)
(c) 0x01ABC => \(15\ ABC\)
(d) 0x11111 => \(02\ 11\)

Problem 6: translate with page directory (of PT pieces)

(a) how many PT pages would have been needed if we instead had a simple, linear array? \(16\)
(b) how many bits of a virt addr are used for the page-directory index? \(4\)
(c) how large in the virtual address space (in terms of number of virtual pages)? \(16^2\)
(d) translate 0x01ABC \(23\ ABC\)
(e) translate 0x00000 \(10\ 000\)
(f) translate 0x00000 \(SS\ ED\ 0\)
(g) does 0x10000 segfault? \(Yes\)

Problem 7: how many levels are needed?

How large is the virtual addr space, assuming 4-KB pages and 4-byte entries with N levels?
(PT can now no longer require more than 1 contiguous page for bookkeeping)
(a) \(N = 1\) \(4\ MB\)
(b) \(N = 2\) \(4\ GB\)
(c) \(N = 3\) \(4\ TB\)

Problem 8: how many physical loads for each instruction (v2)?

Assume a 3-level page table.
Assume 256-byte pages.
Assume 16-bit addresses.
Assume ASID of current process is 211.
Assume this TLB state:

<table>
<thead>
<tr>
<th>ASID</th>
<th>VPN</th>
<th>PFN</th>
<th>valid</th>
<th>Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>211</td>
<td>0xB</td>
<td>0x91</td>
<td>1</td>
<td>???</td>
</tr>
<tr>
<td>211</td>
<td>0xFF</td>
<td>0x23</td>
<td>1</td>
<td>???</td>
</tr>
<tr>
<td>412</td>
<td>0x85</td>
<td>0x91</td>
<td>1</td>
<td>???</td>
</tr>
<tr>
<td>211</td>
<td>0x06</td>
<td>0x12</td>
<td>0</td>
<td>???</td>
</tr>
</tbody>
</table>

How many physical accesses are needed for each instruction?
Consider each instruction independently (e.g., for "b", don't worry how "a" changes the TLB).
(a) \(0x\text{A10}:\) movl \(0x\text{1111}, \%\text{edi} \ 8\)
(b) \(0x\text{B13}:\) addl \(\$0x3, \%\text{edi} \ 1\)
(c) \(0x\text{519}:\) movl \(\%\text{edi}, 0x\text{F10} \ 5\)