USJ 1875
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IEEE IMCET 2023

Enhancing Transistor Sizing in Analog IC Design using a Circuit-Focused Semi-Supervised Learning

ESIB – USJ

Meta

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Beirut, December 2023

Agenda

- **Context**
- **Machine Learning in IC Design**
- **Novelty of this Work**
- **Conclusions and Perspectives**

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The Analog Challenge

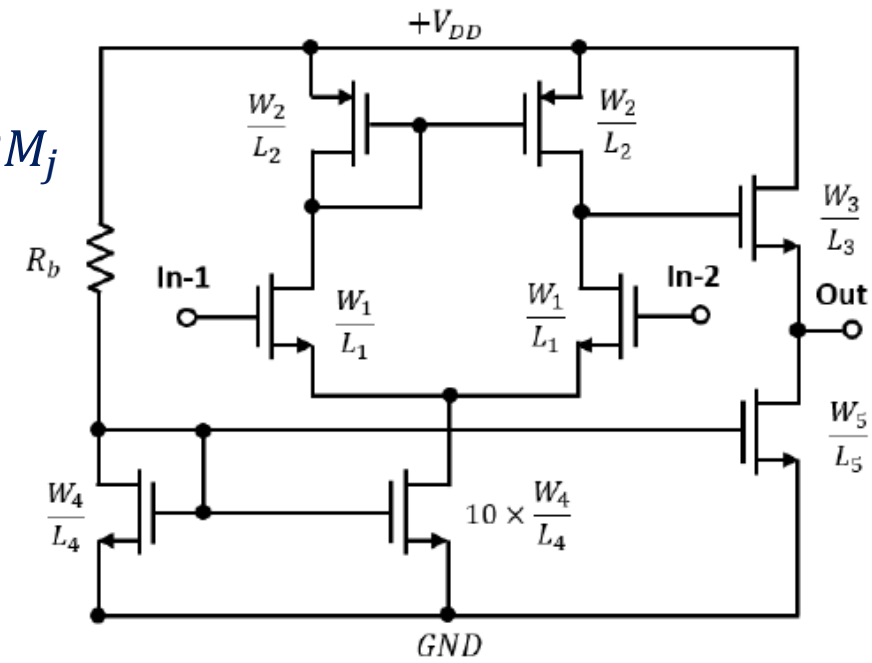
- **Analog IC Design is a 2-step process**
  - **Front-End Design (50%):** Schematic, computer simulations to tune component dimensions
  - **Back-End Design (50%):** Layout, schematic to physical representation of devices
- **Scope of this work → Front-End Design**
- **CHALLENGE** → Front-End Design cycles are time-consuming and expensive
  - Analog circuit performance depends heavily on physical dimensions of circuit components
  - Analog IC designers are rare

Analog IC Design Example

- A simple CMOS 2-stage op-amp has 11 design parameters

- The circuit performance is a set of 12 metrics PM_j
  - Gain, CMRR, …
  - Each PM_j depends on the design parameters

$$PM_j = f_j(W_k, L_k, \dots)$$



- 12 mathematical functions of 11 variables $\in \mathbb{R}^+$ each → The design space is huge

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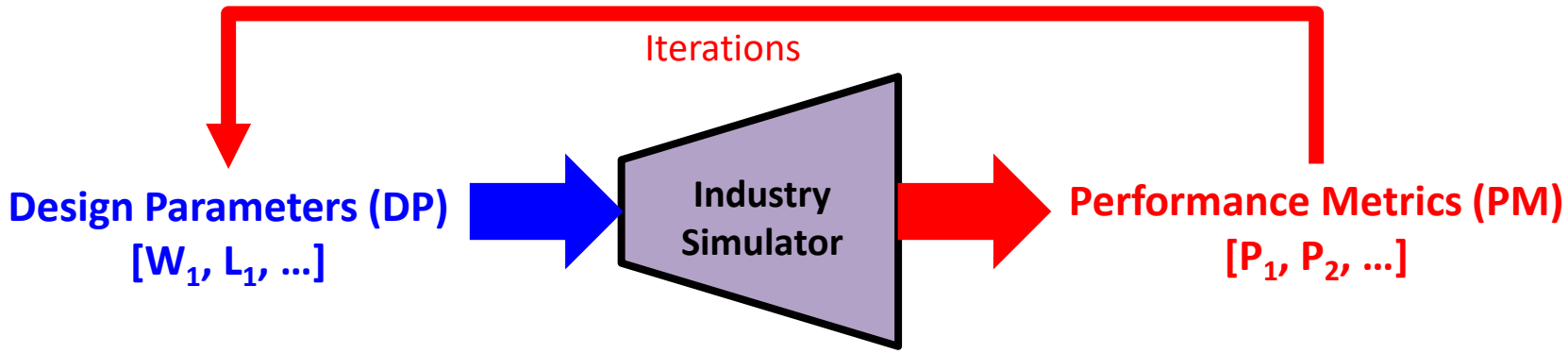
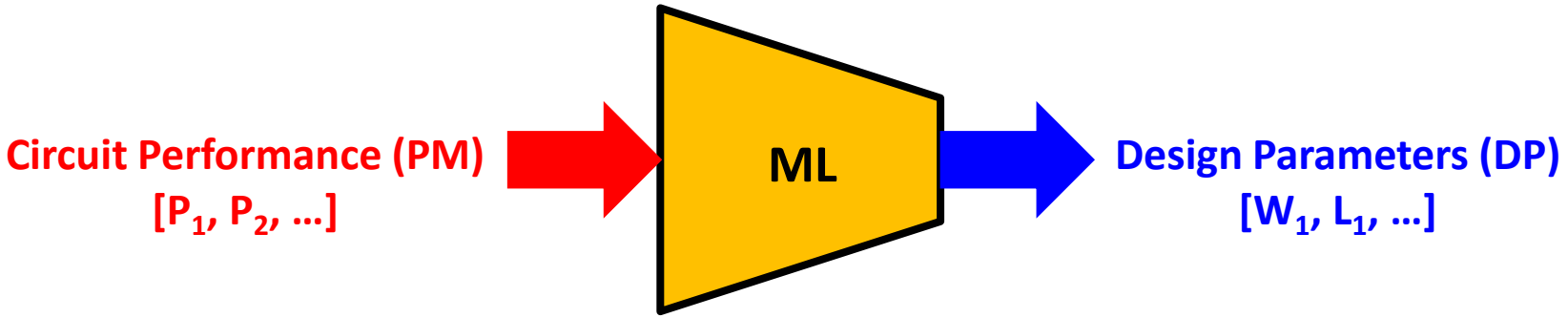
ML Application in IC Design

- Time-consuming Iterative Analog IC design approach:



- ML offers a solution by solving the Inverse-Problem in analog circuit design
  - One-shot design and Instantaneous re-design Solution*



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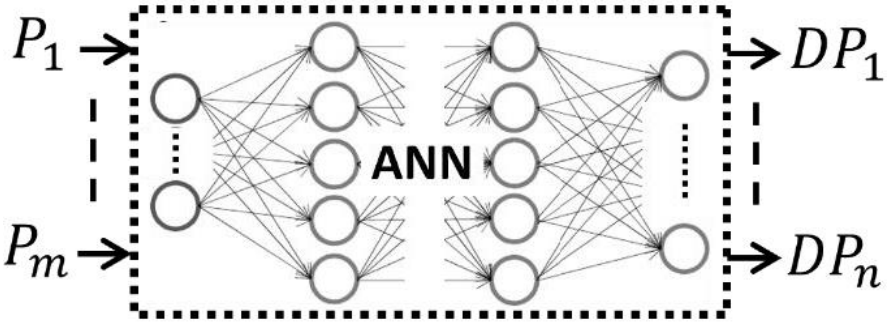
First Attempt: Joint Approach (1)

- **Target Circuit**: 2-stage CMOS op-amp showed in slide #6, 11 DP
- **Dataset**: 150,000 samples = 120k +10k + 10k
- **Idea**: PM are inputs to one ANN, trained to predict all the DP simultaneously
  - This joint approach is intuitive and straightforward

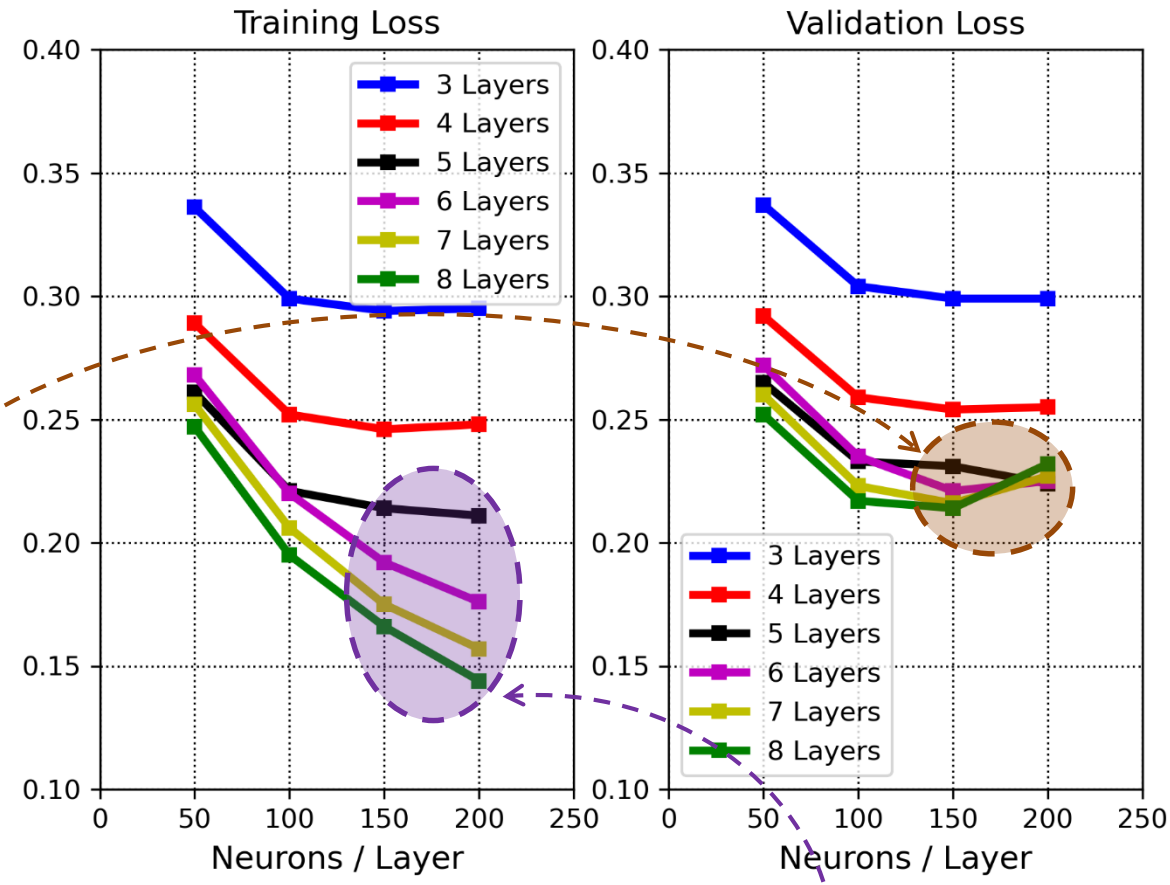


PM

A_V	Open-loop voltage Gain
CMRR	Common-mode rejection ratio
PSRR+	Positive supply rejection ratio
NSRR-	Negative supply rejection ratio
IIN	Integrated noise level
NTH	Thermal noise floor
F_C	Noise corner frequency
GBW	Gain-bandwidth product
PhM	Phase margin
Ibs	Current consumption
V_{OUT}	dc output level
IIP_3	3rd order Input-intercept point

First Attempt: Joint Approach (2)

- **Training and Validation Results**



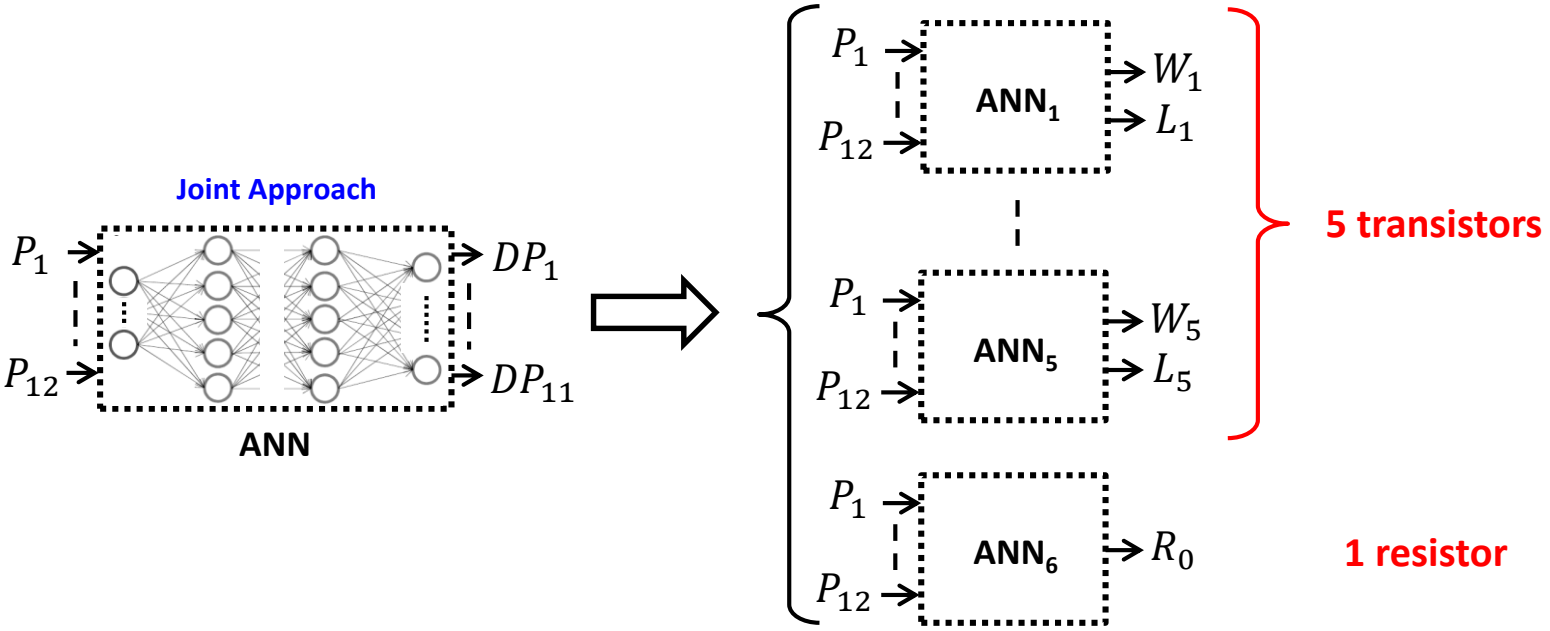
- **Inherent Minimum for VL**

- Increasing ANN does not help, as VL ↗ while Training Loss values ↘ → Overfitting

Investigation: Single Approach (1)

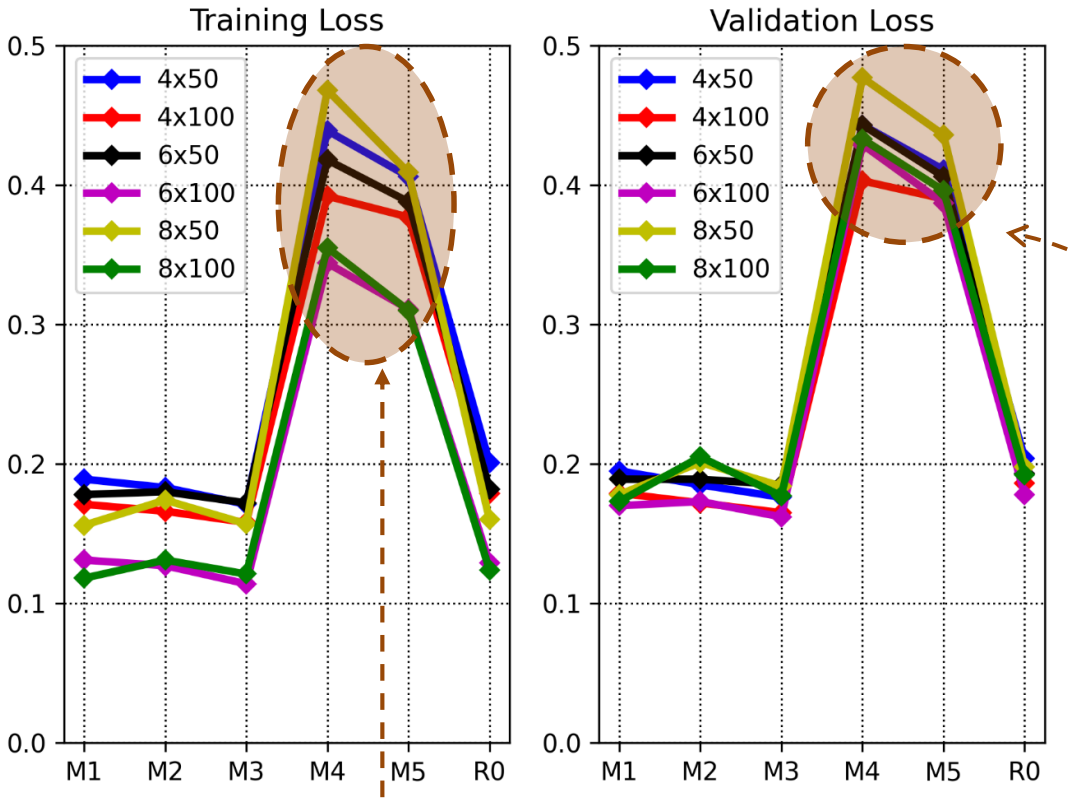
- To understand why we reached a minimum for VL, investigation is carried out

- **Idea**
  - Each component is tuned as a standalone entity
  - Width and Length of MOS transistors should be tuned together
  - Assign a different ANN for each transistor to predict its W/L simultaneously



Investigation: Single Approach (2)

- Training and Validation Loss results of the investigation → two loss patterns

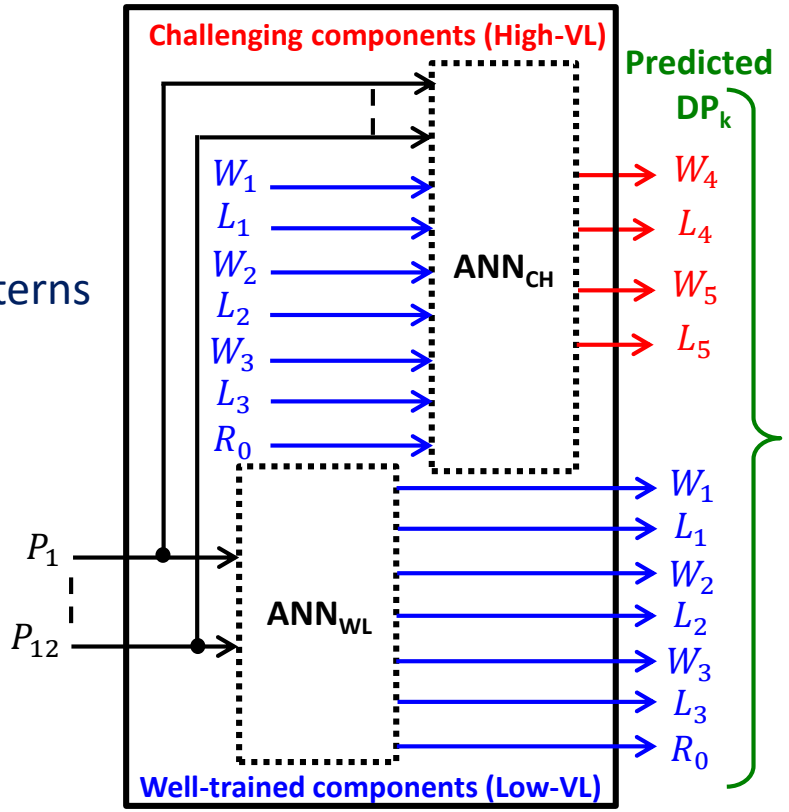


- **Conclusions:**
  - Transistors M_4 & M_5 are challenging components for ANN to learn, high Training Loss & VL
  - Relationships between PM & M_4 / M_5 are less meaningful than those with the remaining DP

Innovative Focused Approach (1)

- Based on VL results, we identified 2 patterns:
  - Well-trained components with low VL values
  - Challenging components with significant high VL values

- **Solution** → propose a **Focused Learning Approach**
  - **Target** → enhance the VL results
  - Split the DP prediction into 2 ANNs based on VL patterns
  - Challenging ANN_{CH} has more inputs than ANN_{WL}
    - ✓ $Inputs = PM + DP_{well\text{-}trained}$

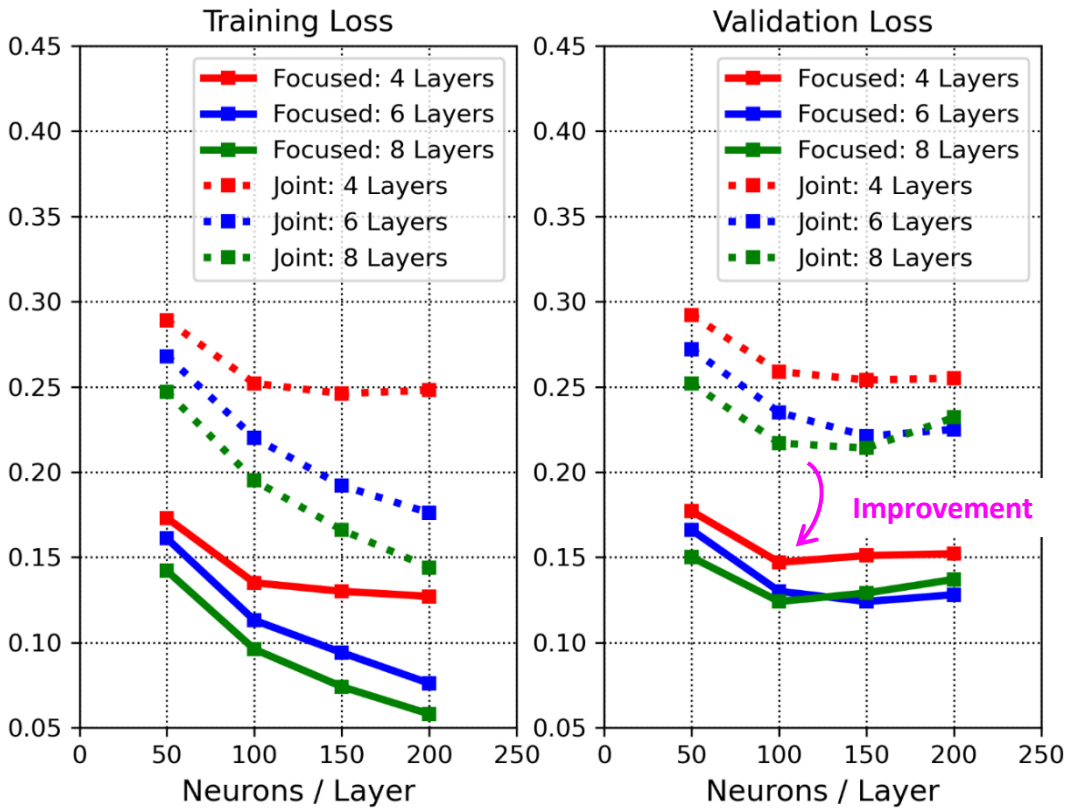


Innovative Focused Approach (2)

- For the challenging transistors, VL decreased by ~3.5 compared to the single approach
  - 6-layer ANN, 100 neurons/layer: VL ↘ from ~0.4 to ~0.11

ANN Architecture		Investigative Approach (ANN for each transistor)		Focused Approach	
		VL	*VL*	*VL*	*TL*
Layers	Neurons per Layer	*M4*	*M5*	*M5*	
4	50	0.44	0.41	0.16	0.18
4	100	0.40	0.39	0.12	0.13
6	50	0.44	0.41	0.15	0.16
6	100	0.43	0.39	0.11	0.12
8	50	0.48	0.44	0.13	0.13
8	100	0.43	0.40	0.10	0.11

- **Joint vs Focused:**
  - 50% VL improvement on all ANN complexities



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Conclusions and Perspectives

- Outcome of this work → "**Proposed and validated a 3-step design procedure for analog circuit sizing based on hierarchical ANN training process**"
  - Evaluate the component predicting difficulty by training 1 ANN for each, using PM as inputs
  - Classify components into two categories, challenging (high VL) and straightforward (low VL)
  - Split the learning process into an ANN for each category, the challenging having a modified input structure incorporating DP of remaining components
- **Future work**: test and validate the proposed focused approach on more analog circuits