

Haris Volos

Senior Researcher
Hewlett Packard Enterprise, Hewlett Packard Labs

Email: hvolos@cs.wisc.edu

Web: <http://www.cs.wisc.edu/~hvolos>

Interests

Operating and distributed systems, file and storage systems, persistent memory, transactional memory, interaction of hardware with systems.

Education

<i>Ph.D., Computer Sciences</i> University of Wisconsin–Madison	December 2012
<i>M.S., Computer Sciences</i> University of Wisconsin–Madison	May 2007
<i>Diploma, Electrical and Computer Engineering</i> National Technical University of Athens (Metsovion), Honors (ranked 1st)	July 2005

Experience

- *Senior Researcher*, Hewlett Packard Enterprise, Hewlett Packard Labs (March 2016 – present)
- *Researcher*, Hewlett Packard Enterprise, Hewlett Packard Labs (November 2015 – February 2016)
- *Researcher*, Hewlett Packard, HP Labs (February 2013 – October 2015)
- *Graduate Research Assistant*, University of Wisconsin–Madison, Computer Sciences Department (June 2006 – December 2012)
- *Graduate Technical Intern*, Intel Corporation, Programming Systems Lab (PSL), Microprocessor Technology Lab (MTL) (May 2008 – August 2008)
- *Teaching Assistant*, University of Wisconsin–Madison, Computer Sciences Department (August 2005 – May 2006)

Awards and Honors

- IEEE Micro's Top Picks from Microarchitecture Conferences, 2008
- Summer Research Fellowship by the Computer Sciences Department, University of Wisconsin–Madison, 2006
- Awarded by the Chancellor the Medal of the National Technical University of Athens for ranking 1st among the students of the School of Electrical and Computer Engineering, National Technical University of Athens, 2005
- *Paris Kanellakis* award for ranking 1st among the students of the School of Electrical and Computer Engineering in Computer Science Division, National Technical University of Athens, 2004

Publications

Refereed Conference Papers

- [C1] Qi Wang, Ludmila Cherkasova, Jun Li, and Haris Volos. “Interconnect Emulator for Aiding Performance Analysis of Distributed Memory Applications”. In: *ICPE '16: Proceedings of the 7th ACM/SPEC on International Conference on Performance Engineering*. 2016.
- [C2] Haris Volos, Guilherme Magalhaes, Ludmila Cherkasova, and Jun Li. “Quartz: A Lightweight Performance Emulator for Persistent Memory Software”. In: *Middleware '15: Proceedings of the 16th International Middleware Conference*. 2015.
- [C3] Goetz Graefe, Haris Volos, Hideaki Kimura, Harumi Kuno, Joseph Tucek, Mark Lillibridge, and Alistair Veitch. “In-memory performance for big data”. In: *PVLDB: Proceedings of the Very Large Data Bases Endowment Volume 8.1* (2014).
- [C4] Haris Volos, Sanketh Nalli, Sankaralingam Panneerselvam, Venkatanathan Varadarajan, Prashant Saxena, and Michael M. Swift. “Aerie: Flexible file-system interfaces to storage-class memory”. In: *EuroSys '14: Proceedings of the 9th ACM European conference on Computer systems*. 2014.
- [C5] Haris Volos, Andres Jaan Tack, Michael M. Swift, and Shan Lu. “Applying transactional memory to concurrency bugs”. In: *ASPLOS '12: Proceedings of the 17th International Conference on Architectural Support for Programming Languages and Operating Systems*. 2012.
- [C6] Haris Volos, Andres Jaan Tack, and Michael M. Swift. “Mnemosyne: Lightweight persistent memory”. In: *ASPLOS '11: Proceedings of the 16th International Conference on Architectural Support for Programming Languages and Operating Systems*. 2011.
- [C7] Haris Volos, Andres Jaan Tack, Neelam Goyal, Michael M. Swift, and Adam Welc. “xCalls: Safe I/O in memory transactions”. In: *EuroSys '09: Proceedings of the 4th ACM European conference on Computer systems*. 2009.
- [C8] Haris Volos, Adam Welc, Ali-Reza Adl-Tabatabai, Tatiana Shpeisman, Xinmin Tian, and Ravi Narayanaswamy. “NePaLTM: Design and implementation of nested parallelism for transactional memory systems”. In: *ECOOP '09: Proceedings of the 23rd European Conference on Object-Oriented Programming*. 2009.
- [C9] Jayaram Bobba, Kevin E. Moore, Haris Volos, Luke Yen, Mark D. Hill, Michael M. Swift, and David A. Wood. “Performance pathologies in hardware transactional memory”. In: *ISCA '07: Proceedings of the 34th International Symposium on Computer Architecture*. 2007.
- [C10] Luke Yen, Jayaram Bobba, Michael R. Marty, Kevin E. Moore, Haris Volos, Mark D. Hill, Michael M. Swift, and David A. Wood. “LogTM-SE: Decoupling hardware transactional memory from caches”. In: *HPCA '07: Proceedings of the 13th International Symposium on High Performance Computer Architecture*. 2007.

Journal Papers

- [J1] Jayaram Bobba, Kevin E. Moore, Haris Volos, Luke Yen, Mark D. Hill, Michael M. Swift, and David A. Wood. “Performance Pathologies in Hardware Transactional Memory”. In: *IEEE Micro* (2008).

Refereed Workshop Papers

- [W1] Haris Volos, Sankaralingam Panneerselvam, Sanketh Nalli, and Michael M. Swift. “Storage-class memory needs flexible interfaces”. In: *APSys '13: Proceedings of the 4th Asia-Pacific Workshop on Systems*. 2013.

- [W2] Haris Volos and Michael M. Swift. *Storage systems for storage-class memory*. NVMW '11: 2nd Annual Non-Volatile Memories Workshop. 2011.
- [W3] Michael M. Swift, Haris Volos, Neelam Goyal, Luke Yen, Mark D. Hill, and David A. Wood. *OS Support for virtualizing hardware transactional memory*. TRANSACT '08: 3rd ACM SIGPLAN Workshop on Transactional Computing. 2008.
- [W4] Haris Volos, Neelam Goyal, and Michael M. Swift. *Pathological interaction of locks with transactional memory*. TRANSACT '08: 3rd ACM SIGPLAN Workshop on Transactional Computing. 2008.

Patents and Patent Applications

- [P1] Henggang Cui, Kimberly Keeton, Indrajit Roy, Krishnamurthy Viswanathan, and Haris Volos. "Processing a query using transformed raw data". U.S. Patent Application No. WO2016068829. 2016.
- [P2] Guilherme De Campos Magalhaes, Haris Volos, and Ludmila Cherkasova. "Inject delay to simulate latency". U.S. Patent Application No. PCT/US2016/014479. 2016.
- [P3] Haris Volos and Jun Li. "Allocating a zone of a shared memory region". U.S. Patent Application No. PCT/US2016/018227. 2016.
- [P4] Jun Li and Haris Volos. "In-Memory data shuffling". U.S. Patent Application No. PCT/US2015/061843. 2015.
- [P5] Sanketh Nalli, Haris Volos, and Kimberly Keeton. "Ordering updates for non-volatile memory accesses". U.S. Patent Application No. PCT/US2015/013958. 2015.
- [P6] Sriram Narasimhan, Tuan Dinh Bui, Jun Li, and Haris Volos. "Distributed data shuffling". U.S. Patent Application No. PCT/US2015/061964. 2015.
- [P7] Haris Volos, Jun Li, Kimberly Keeton, and Joseph Tucek. "Distributed datasets in shared non-volatile memory". U.S. Patent Application No. PCT/US2015/042134. 2015.
- [P8] Charles Stuart Johnson, Harumi Kuno, Goetz Graefe, Haris Volos, Mark Lillibridge, James Hyung-sun Park, and Wey Guy. "Page modification". U.S. Patent Application No. WO2016053313. 2014.
- [P9] Goetz Graefe, Haris Volos, Hideaki Kimura, Harumi Kuno, Alistair Veitch, Joseph Tucek, and Alvin AuYoung. "Structuring page images in a memory". U.S. Patent Application No. WO2015163898. 2013.
- [P10] David A. Wood, Mark D. Hill, Michael M. Swift, Michael R. Marty, Luke Yen, Kevin E. Moore, Jayaram Bobba, and Haris Volos. "Non-broadcast signature-based transactional memory". U.S. Patent No. 8239633. 2012.
- [P11] Adam Welc, Haris Volos, Ali Adl-Tabatabai, and Tatiana Shpeisman. "Methods and systems for transactional nested parallelism". U.S. Patent Application No. US20100162247. 2008.

Other Articles (including technical reports and posters)

- [O1] Haris Volos, Adam Welc, Ali-Reza Adl-Tabatabai, Tatiana Shpeisman, Xinmin Tian, and Ravi Narayanaswamy. *NePalTM: Design and implementation of nested parallelism for transactional memory systems*. PPOPP '09: Proceedings of the 4th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, Poster abstract. 2009.
- [O2] Mark D. Hill, Derek Hower, Kevin E. Moore, Michael M. Swift, Haris Volos, and David A. Wood. *A case for deconstructing hardware transactional memory systems*. Tech. rep. CS-TR-2007-1594. University of Wisconsin - Madison, Computer Sciences, 2007.

Tutorials

- [1] Dhruva Chakrabarti, Haris Volos, and Indrajit Roy. “How Should We Program Non-volatile Memory?” In: *PLDI '16: 37th ACM SIGPLAN Conference on Programming Language Design and Implementation*. 2016.
- [2] Michael M. Swift and Haris Volos. “Programming and Usage Models for Non-Volatile Memory”. In: *ASPLOS '15: 17th International Conference on Architectural Support for Programming Languages and Operating Systems*. 2015.

Talks

- [1] *Flexible file-system interfaces to storage-class memory*. Given at various places including Eurosys '14, SNIA SDC '14. 2014.
- [2] *Applying transactional memory to concurrency bugs*. ASPLOS '12. 2012.
- [3] *Revamping the system interface to storage-class memory*. Given at various places including HP Labs, Intel Labs, Netapp, Oracle Labs, Qualcomm. 2012.
- [4] *Mnemosyne: Lightweight Persistent Memory*. Given at various places including ASPLOS '11, Microsoft's Jim Gray Systems Lab, Google Madison, Wisconsin Architecture Affiliates, Wisconsin Database Affiliates. 2010-2011.
- [5] *xCalls: Safe I/O in Memory Transactions*. EuroSys '09. 2009.
- [6] *Pathological Interaction of Locks with Transactional Memory*. TRANSACT. 2008.
- [7] *A virtualization stack for hardware transactional memory*. Wisconsin Architecture Affiliates. 2007.

Professional Service

- Program Committee Member, ACM/IFIP/USENIX International Conference on Middleware, 2015
- Program Committee Member, ACM/IFIP/USENIX International Conference on Middleware, 2014
- External Secondary Reviewer, USENIX Annual Technical Conference, 2014
- Reviewer, IEEE Computer Architecture Letters, 2014

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