CS 252
Lecture 27; 2015 Nov 16th; Transcribed Lecture notes

Outline

In-class exercise to do cycle-by-cycle what happens in the machine.

In-class Exercise

Start with an instruction.
Go to state diagram.
Trace through the states.

```
ldi r16, 5
ldi r17, 23
ldi r18, 11
add r17, r18 ;  add r17, r18 = 000011_1_10001_0010 = 0x0F12
breq 4
rjmp -3
```

cycle 1: Start at state 00000 (0d0)
cycle 2: add signal -> go to state 00010 (0d2)
cycle 3: add signal -> go to state 00111 (0d7)
cycle 4: add signal -> go to state 01010 (0d10)
cycle 5: add signal -> go to state 01000 (0d8)
cycle 6: add signal -> go to state 01011 (0d11)
cycle 7: add signal -> go to state 01101 (0d13)
cycle 8: add signal -> go to state 10010 (0d18)
cycle 9: add signal -> go to state 10011 (0d19)

Every state has the name of the auxiliary register

Solution subject to change depending on simulator updates.
At cycle 1:
- control signal: INST_we = 1; all_others = 0
- aux reg: INST = 0x0F12

At cycle 2:
- control signal: REG_we = 1; REG_sel = 1; all_others = 0
  - (for muxes, 0 is top and 1 is bottom unless stated otherwise)
- aux reg: REG = 0b10001 (0d17)

At cycle 3:
- control signal: VAL1_we = 1; RF_sel = 0; all_others = 0
- aux reg: VAL1 = 0b00010111 (0d23)

At cycle 4:

control signal: REG2_we = 1; all_others = 0

aux reg: REG2 = 0b00010010 (0d18)

At cycle 5:

control signal: VAL2_we = 1; VAL2_sel = 0; RF_sel = 1; all_others = 0

aux reg: VAL2 = 0b00001011 (0d11)

At cycle 6:

control signal: VAL_we = 1; VAL_sel = 1; A_sel = 1; B_sel = 0; ALU_op = 0; all_others 0

aux reg: VAL = 0b00100010 (0d34)

At cycle 7:

control signal: SREG_we = 1; all_others 0

aux reg: update SREG

Z is cleared since the result is 34, not zero;

C cleared since unsigned op1+op2 <= 255;

N is cleared because 34 is not negative

At cycle 8:

control signal:RF_we = 1; RF_sel = 0; all_others 0

aux reg: none

register file: r17 = 0b00100010 (0d34)

At cycle 9:

control signal: PC_we = 1; PC_sel = 1; all_others 0

(aux) reg: PC = PC + 1 = 3 + 1 = 4

I think there may be an inconsistency between the book and the simulator on whether PC and SREG is an auxiliary register.