Announcements

- No class Friday. Happy Thanksgiving!
- Homework 8 released later today, due Friday, Dec 11
- Exam 3 & HW 7 up front
- Exam 3 Review today
ISA -> Binary conversions

a. 0000_1111_0011_0110 (Hex 0x0F36)  
a. 1110_0001_0011_0101 (HEX: E135)
   
   add ?  
   ldi ?

b. ldi r17, 15  
b. add r17, r20

ldi:

```
1110_IIII_RRRR_IIII
```

add:

```
000011_S_RRRRR_SSSS
```
2. Stages vs states

Each state performs a single small instruction, while a stage is a broad classification for states describing their overall function.
3. Muxes & select lines
4. Tracing RJMP states 1100_0000_0000_0101

1. 00000: INST=PM [PC]
2. 00100: OFF=SEXT16(INST [11:0])
3. 01110: VAL=OFF+PC
4. 10100: PC = VAL
5. 10011: PC = PC +1
5. Adding instructions

<table>
<thead>
<tr>
<th>ISA example</th>
<th>inc r17 (should increment value in r17 by 1)</th>
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</thead>
<tbody>
<tr>
<td>Opcode</td>
<td>10010100011</td>
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<tr>
<th>Bit-level encoding (C = opcode, R = register)</th>
<th>CCCCCCCRRRRRRCCCC 1001010??????0011</th>
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5. Adding instructions

**00010**: Put name in REG

**00111**: Read RF[REG] and put into VAL1

**NEW STATE [10110]**: Put 1 into OFF (new state)

**NEW STATE [10111]**: Perform ALU_op = 1 (addition), VAL=VAL1+OFF (new state)

**10010**: Write VAL into REG

**10011**: PC=PC+1
6. Tracing Instruction Cycles

Done live in class. No slides, please see solution.