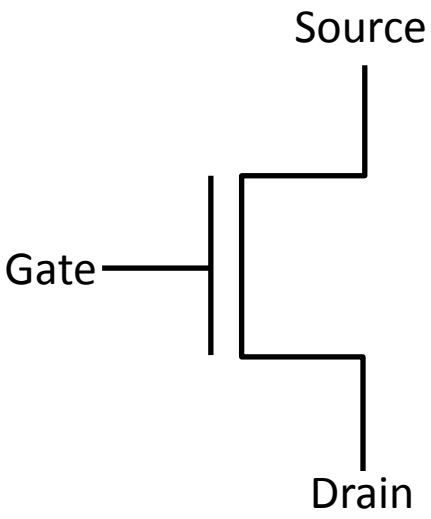
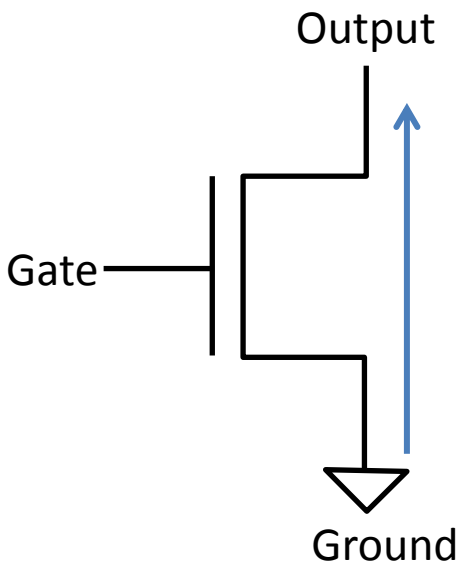
Today

- Transistor behavior
- Logic gates using transistors
- Moore’s Law and Dennard Scaling

Transistor

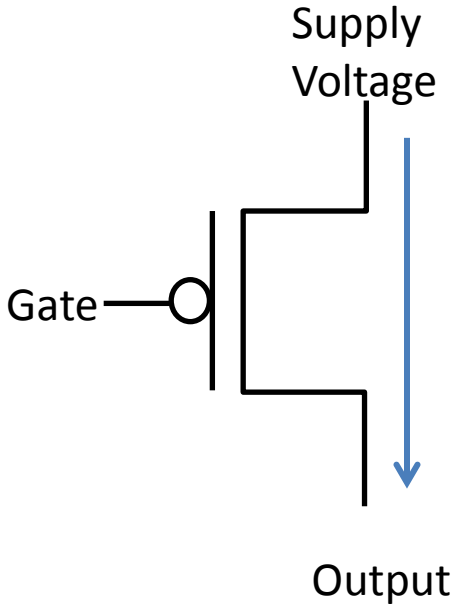


Transistor terminals



N-type transistor

Gate	Behavior
1	Closed Output=0
0	Open Output=Z



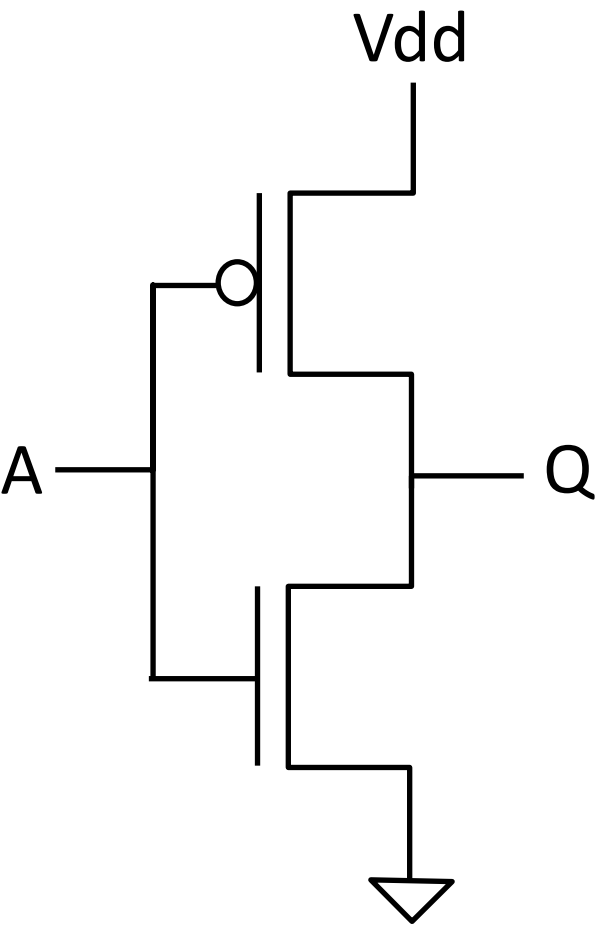
P-type transistor

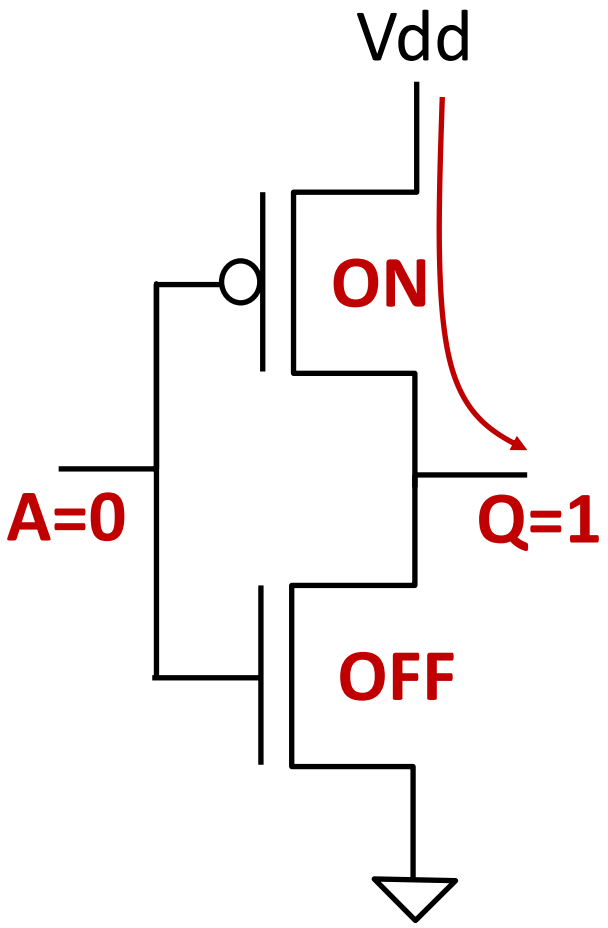
Gate	Behavior
0	Closed Output=1
1	Open Output=Z

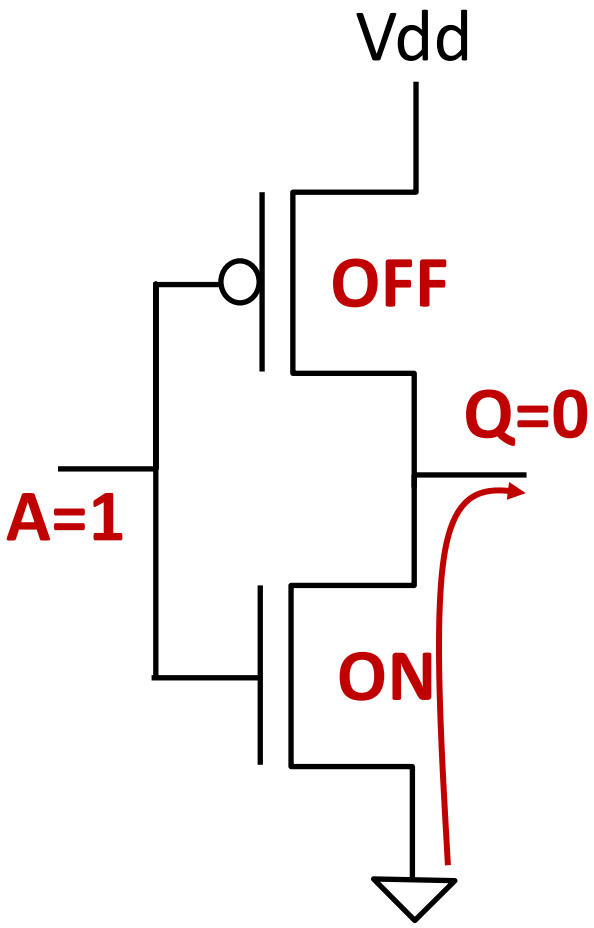
NOT Gate with Transistors

N-type	
Gate	Behavior
1	Closed Output=0
0	Open Output=Z

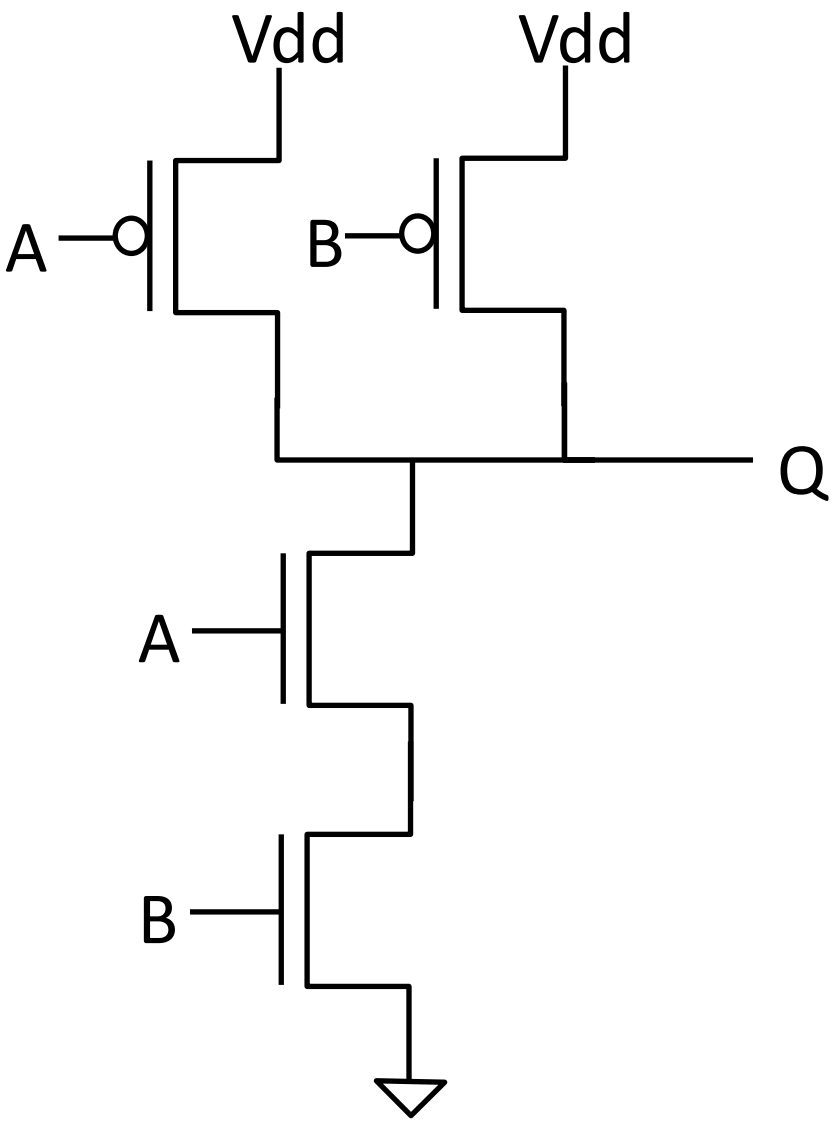
P-type	
Gate	Behavior
0	Closed Output=1
1	Open Output=Z



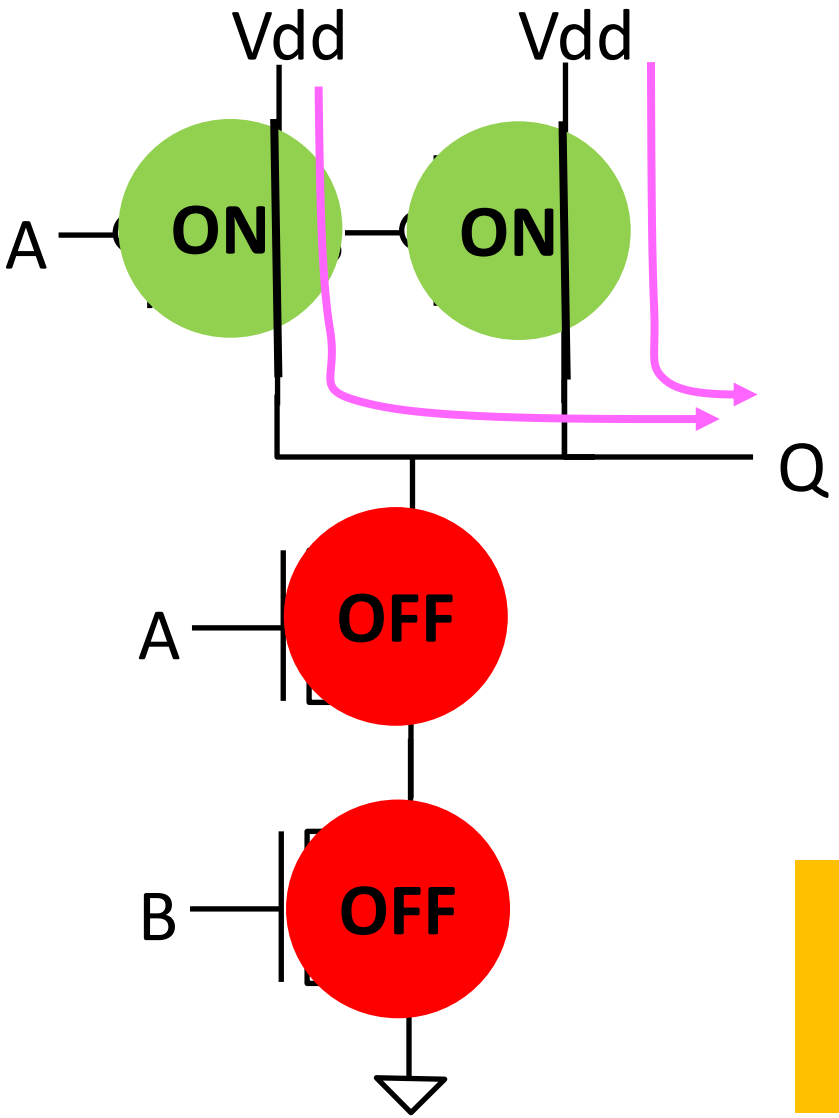




Transistor Circuits (NAND gate)



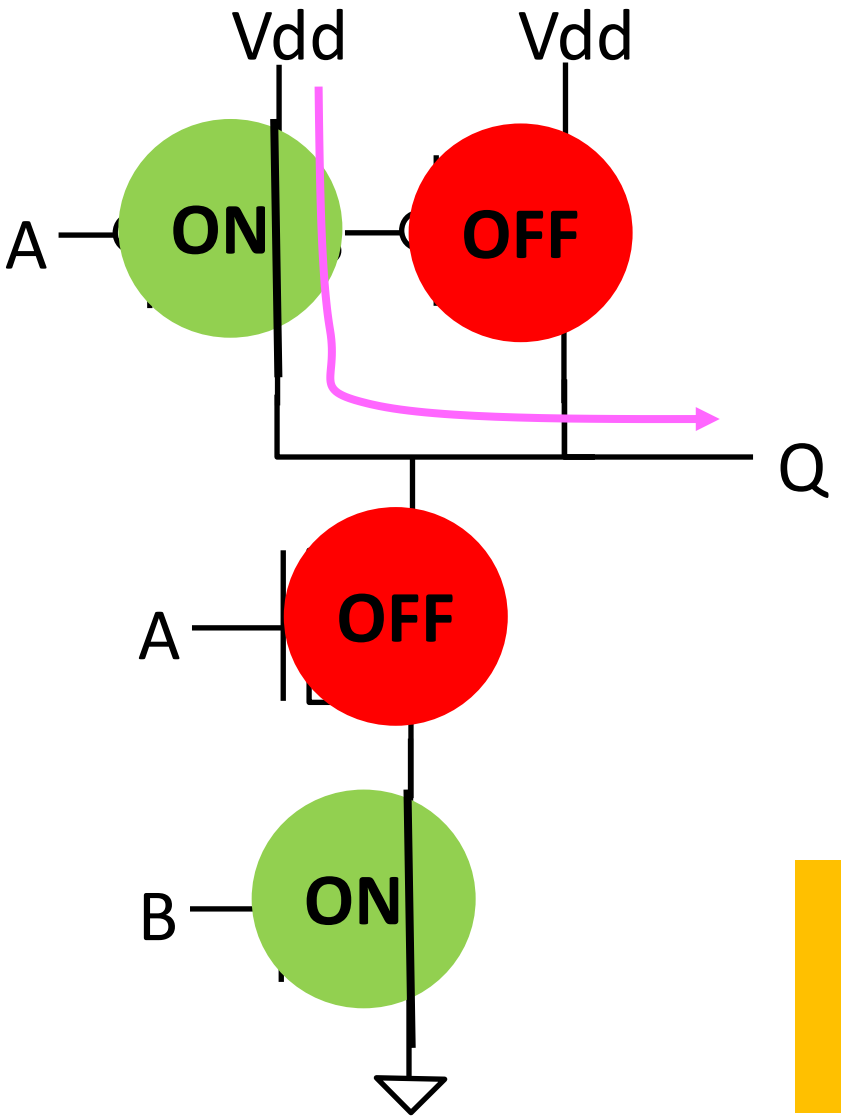
Transistor Circuits (NAND gate)



A	B	Q
0	0	1

P-type ON when gate is 0
N-type ON when gate is 1

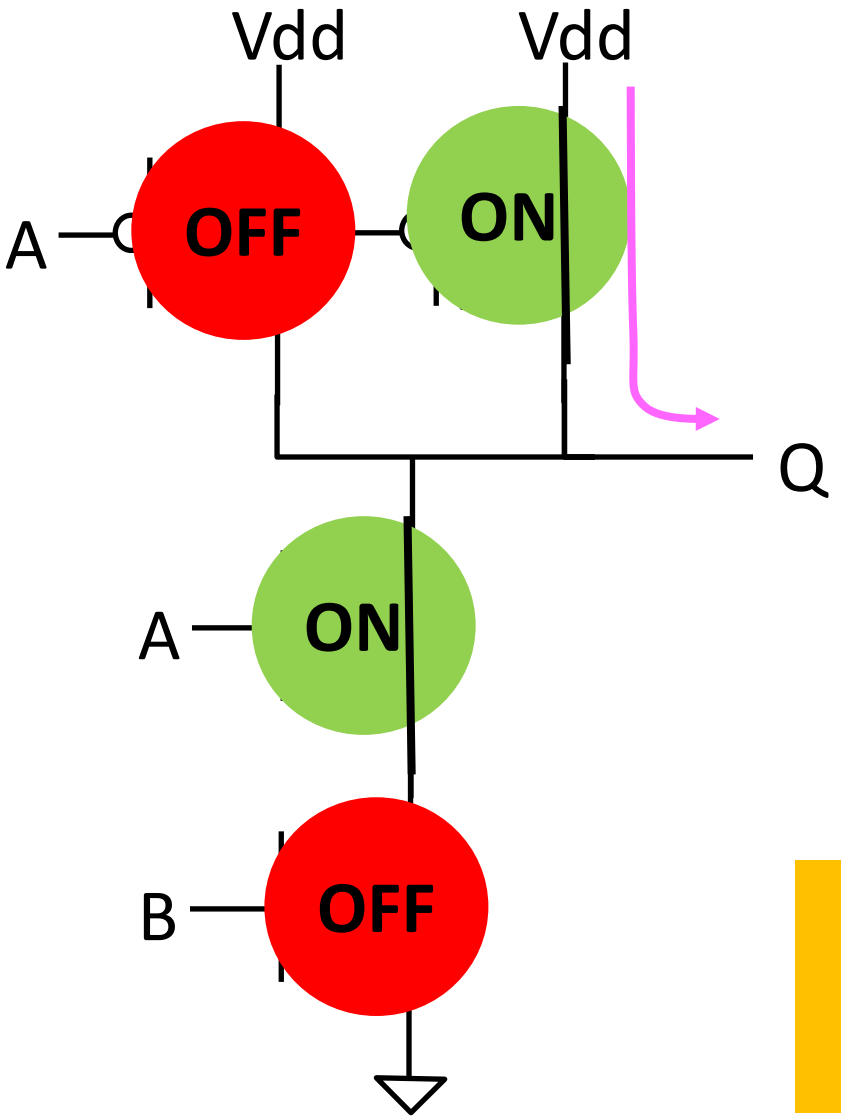
Transistor Circuits (NAND gate)



A	B	Q
0	0	1
0	1	1

P-type ON when gate is 0
N-type ON when gate is 1

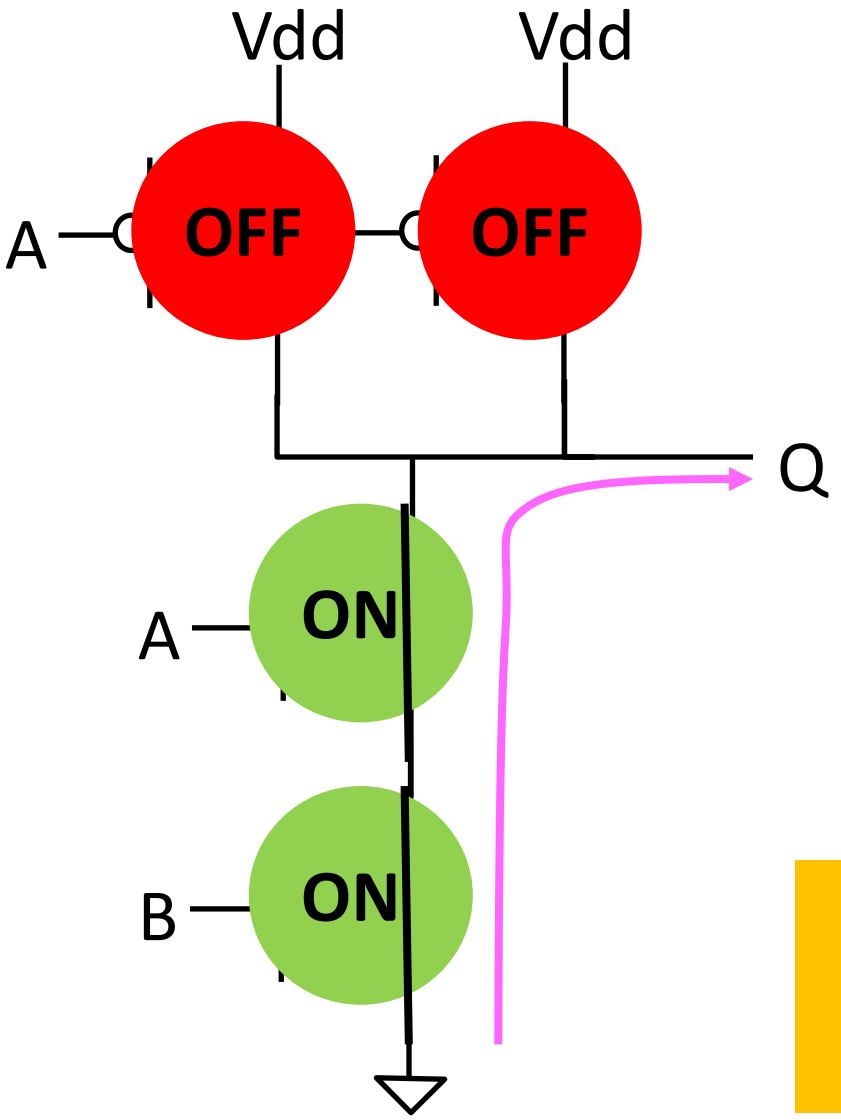
Transistor Circuits (NAND gate)



A	B	Q
0	0	1
0	1	1
1	0	1

P-type ON when gate is 0
N-type ON when gate is 1

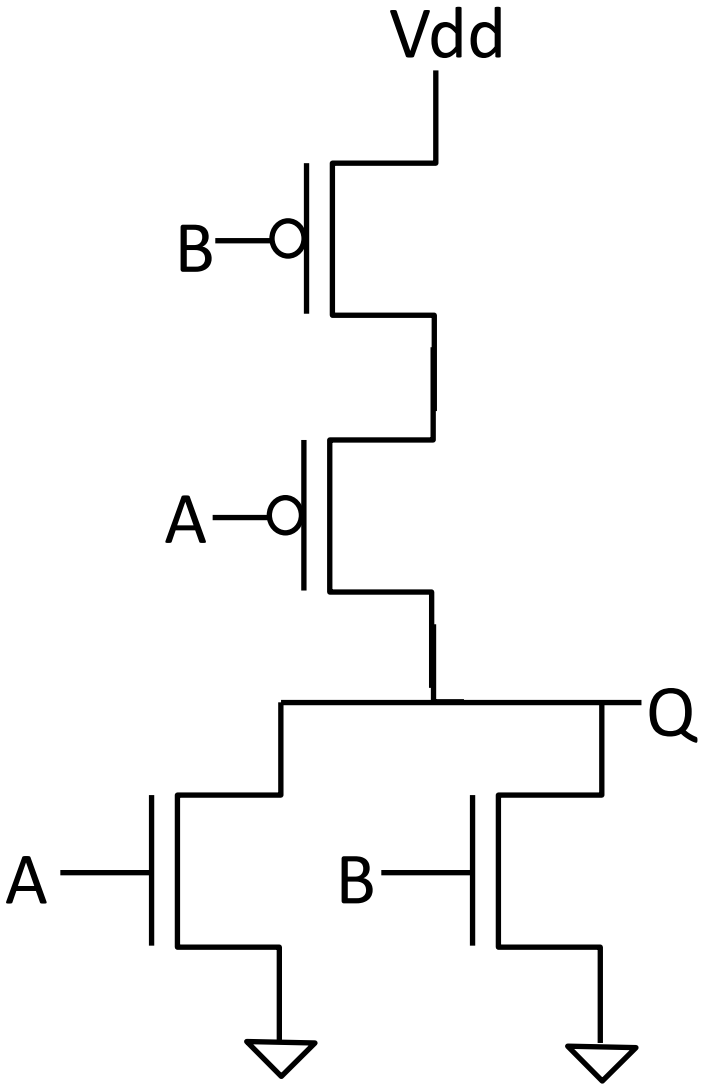
Transistor Circuits (NAND gate)



A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

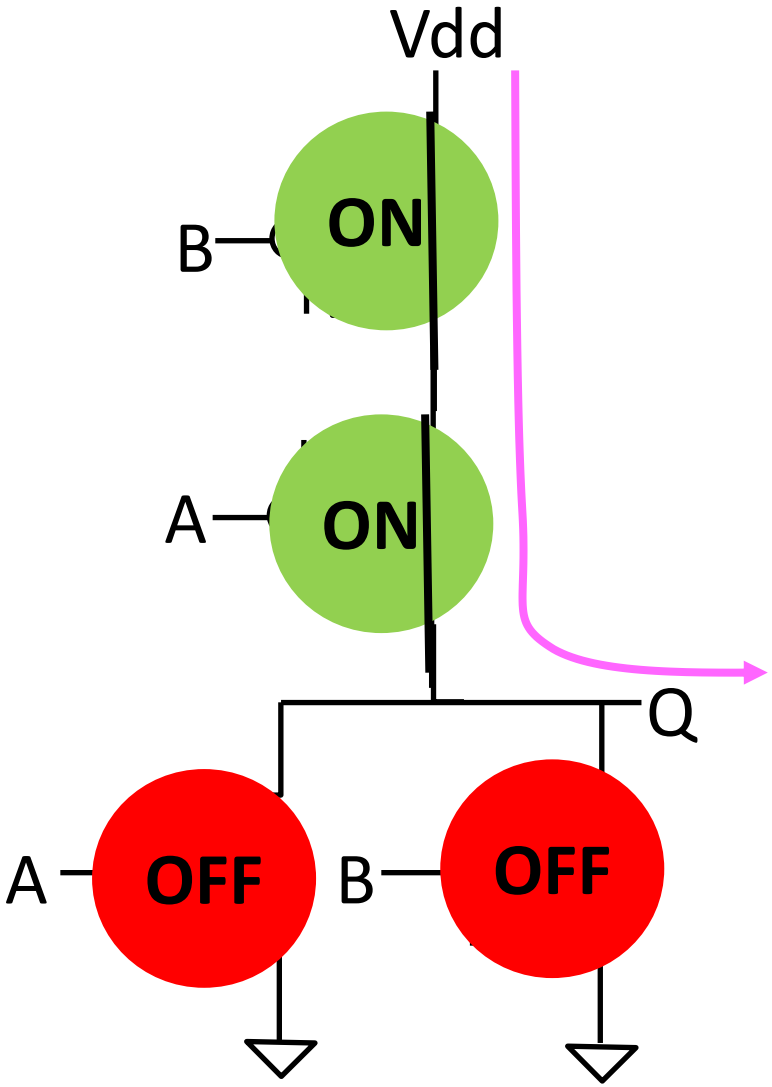
P-type ON when gate is 0
N-type ON when gate is 1

Transistor Circuits (NOR gate)



NOR Gate

Transistor Circuits (NOR gate)

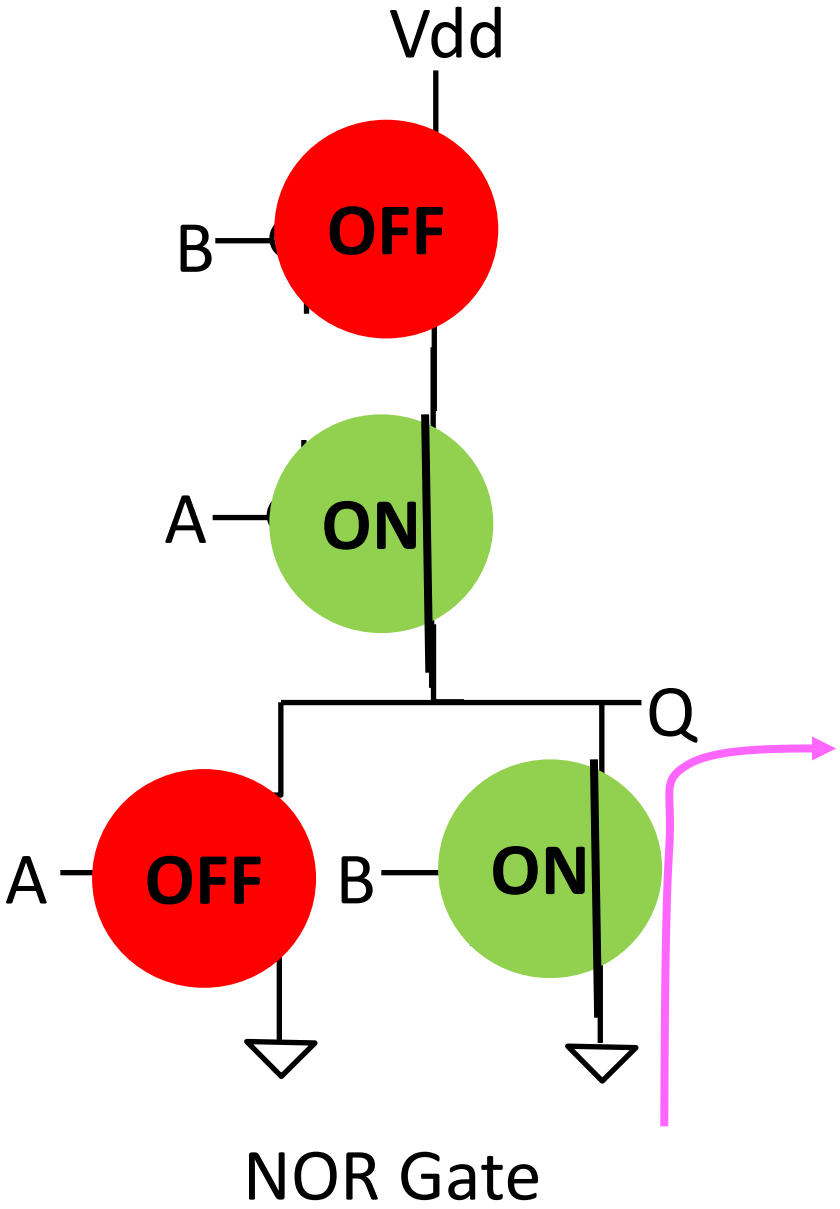


NOR Gate

A	B	Q
0	0	1

P-type ON when gate is 0
N-type ON when gate is 1

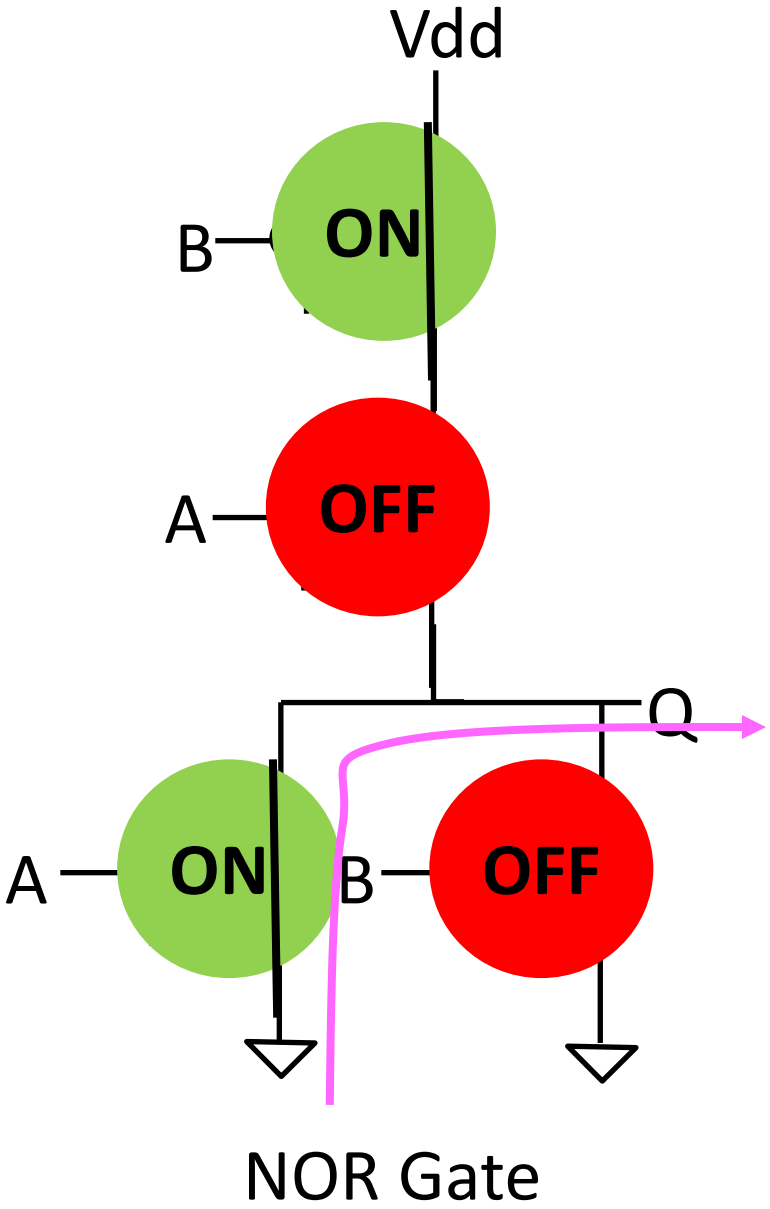
Transistor Circuits (NOR gate)



A	B	Q
0	0	1
0	1	0

P-type ON when gate is 0
N-type ON when gate is 1

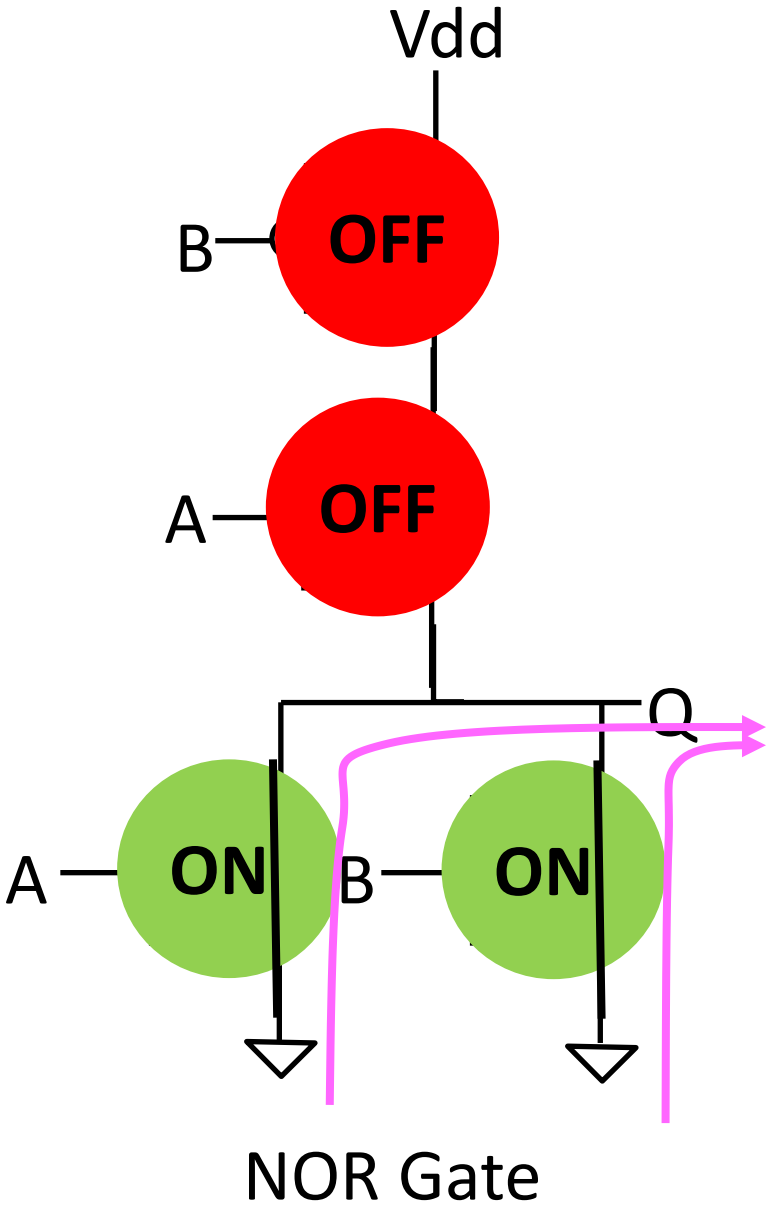
Transistor Circuits (NOR gate)



A	B	Q
0	0	1
0	1	0
1	0	0

P-type ON when gate is 0
N-type ON when gate is 1

Transistor Circuits (NOR gate)

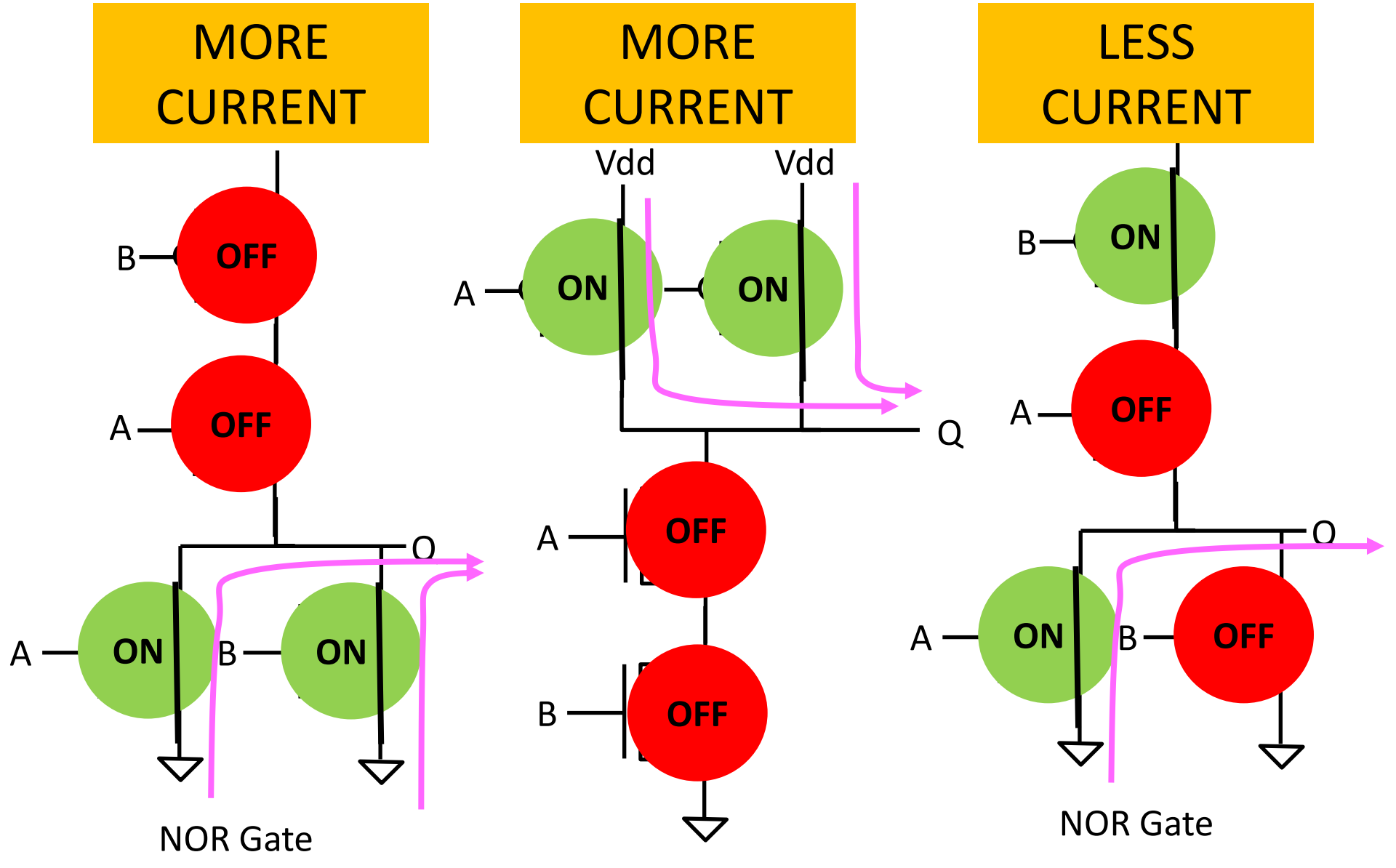


NOR Gate

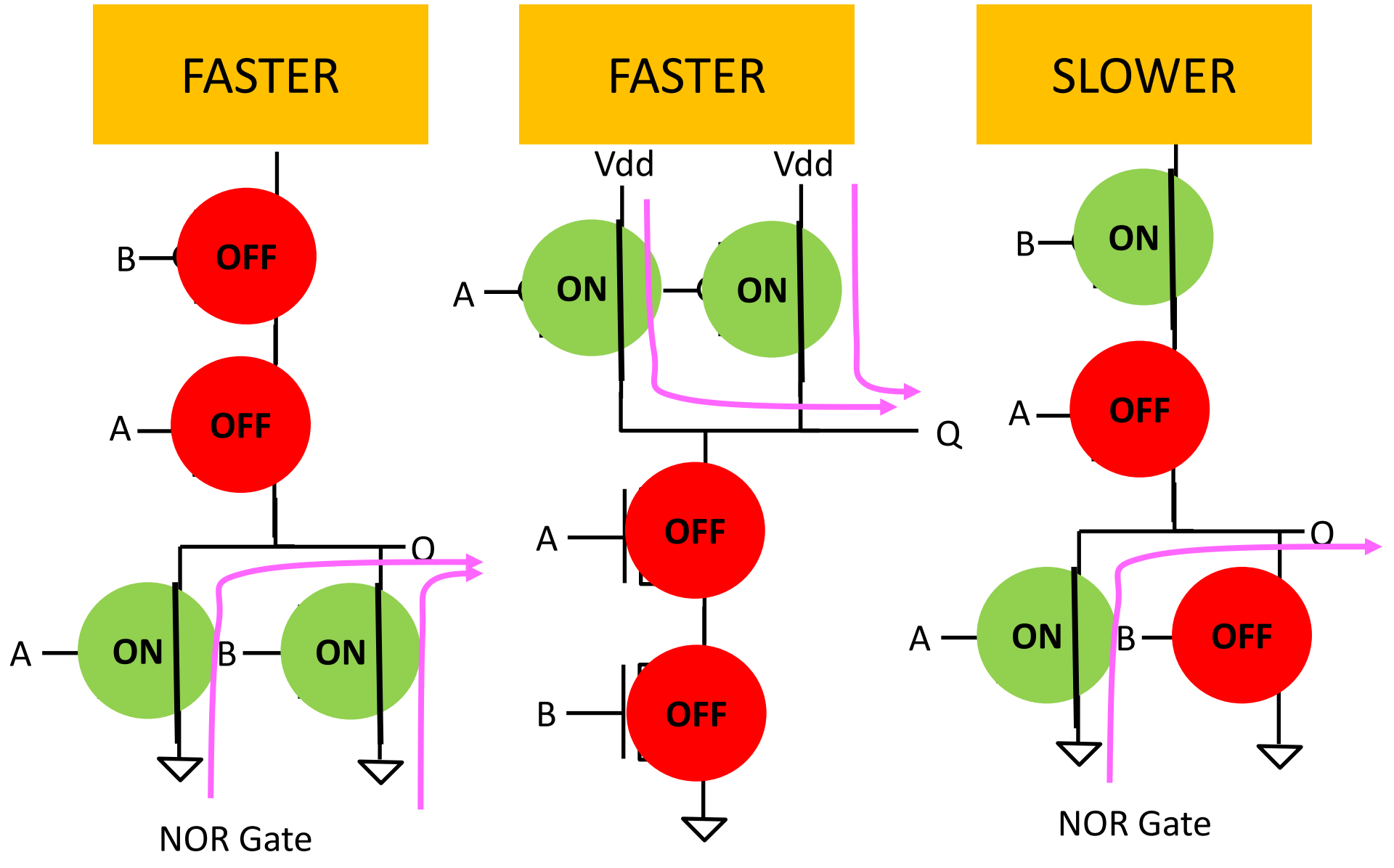
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

P-type ON when gate is 0
N-type ON when gate is 1

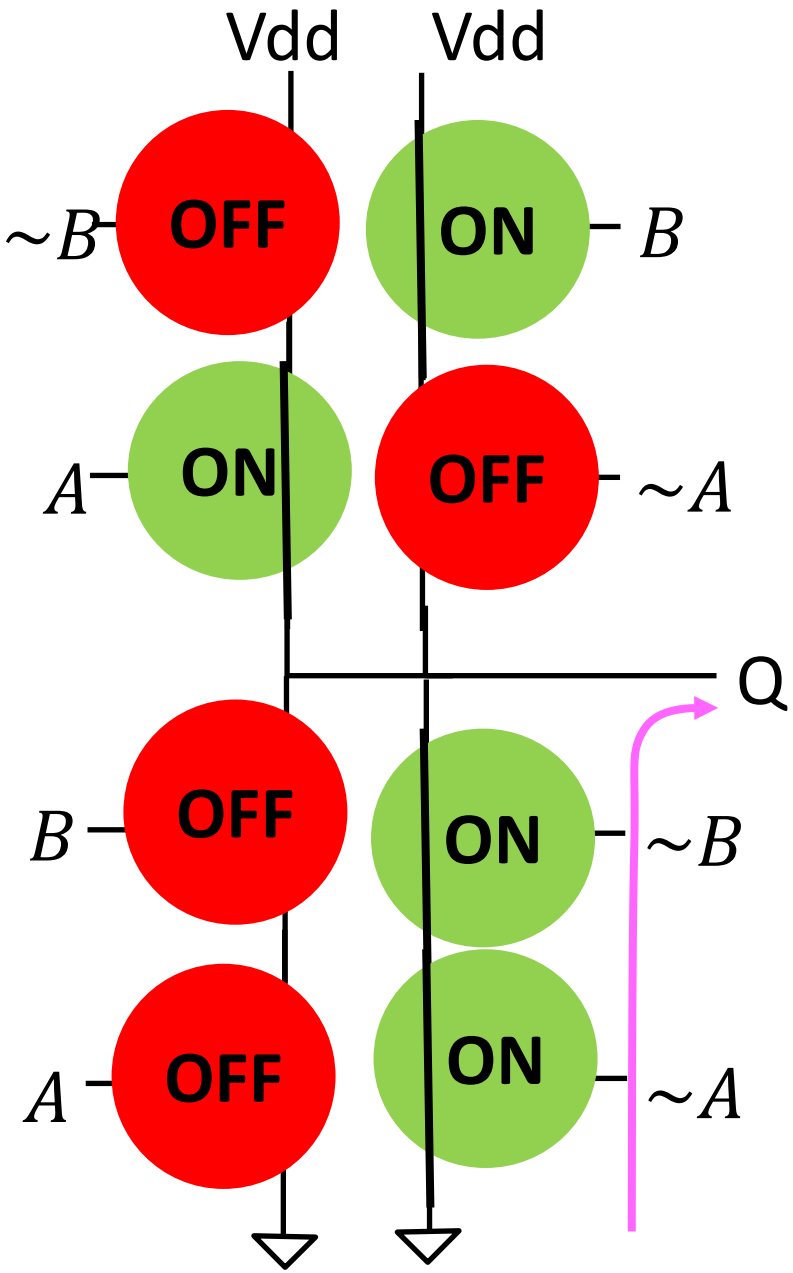
Delays (NOT ON TEST)



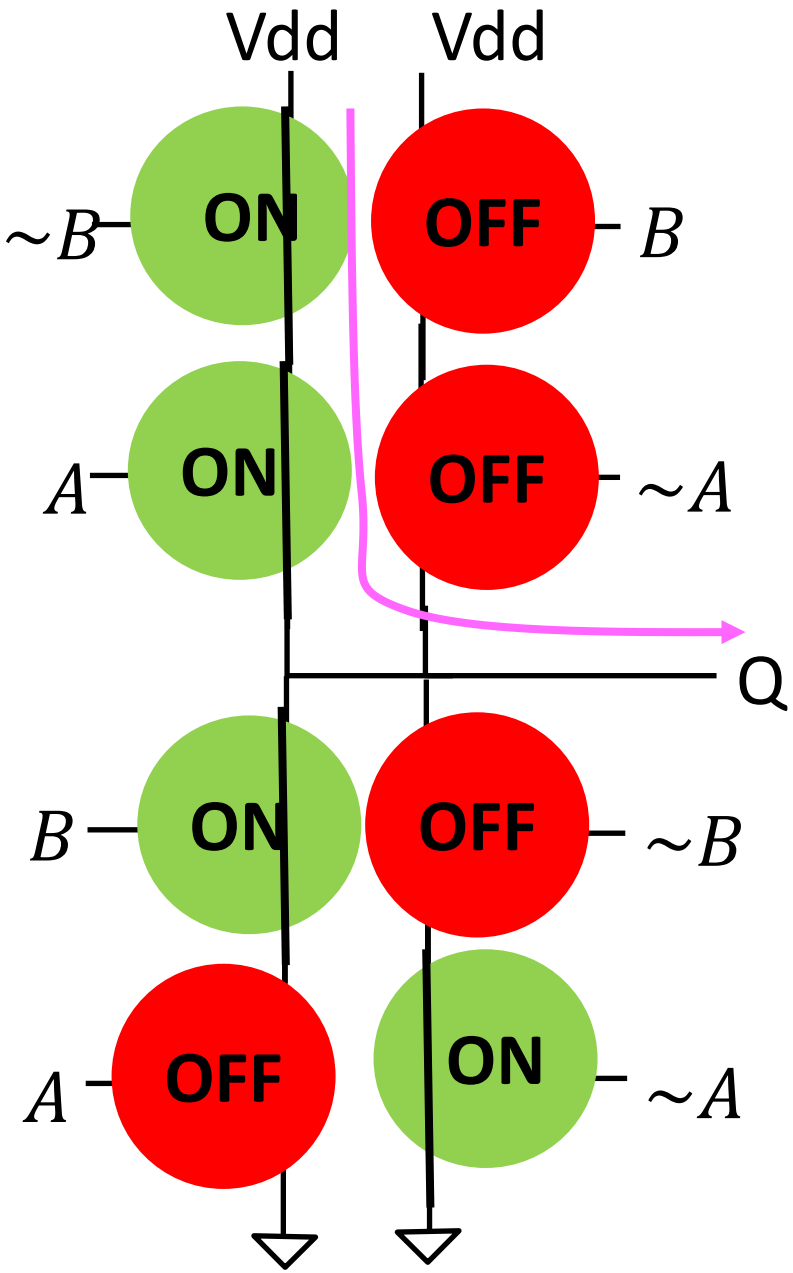
Delays (NOT ON TEST)



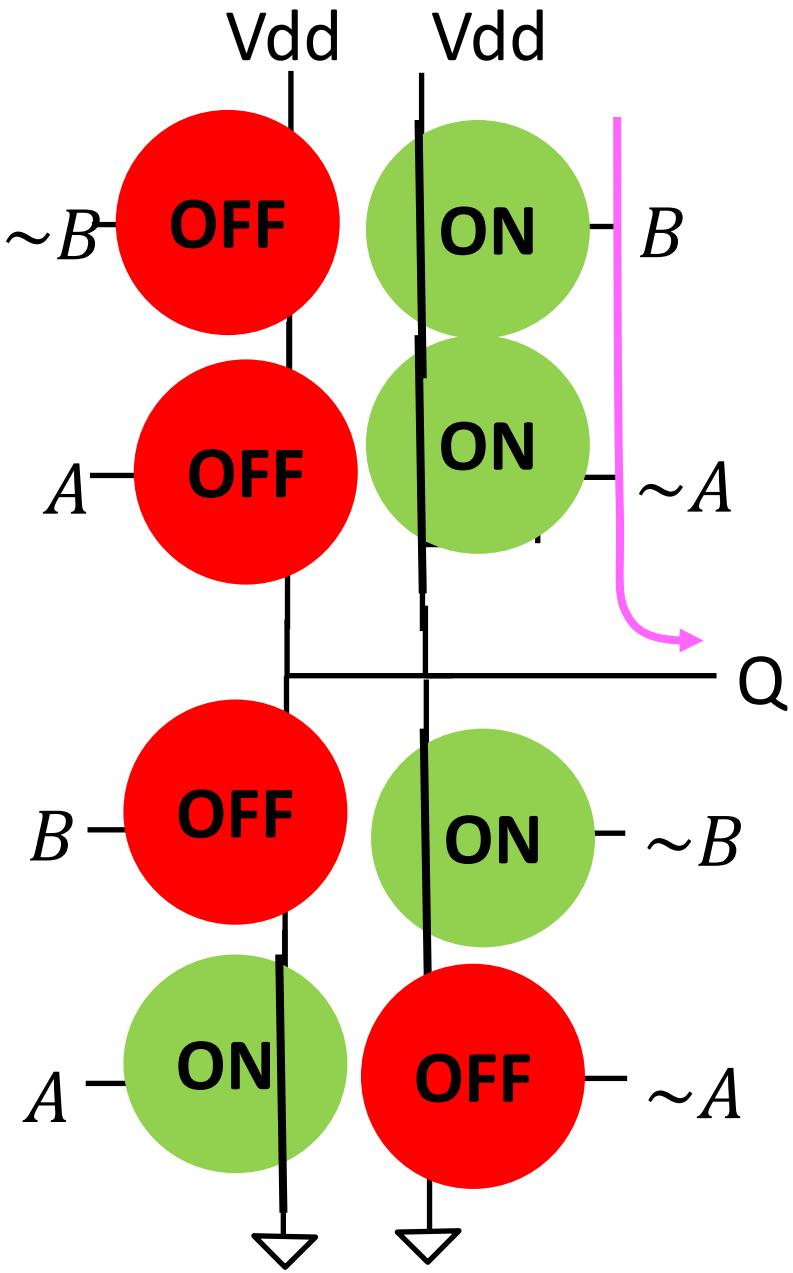
Gate delays and transistor delays vary based on the input!



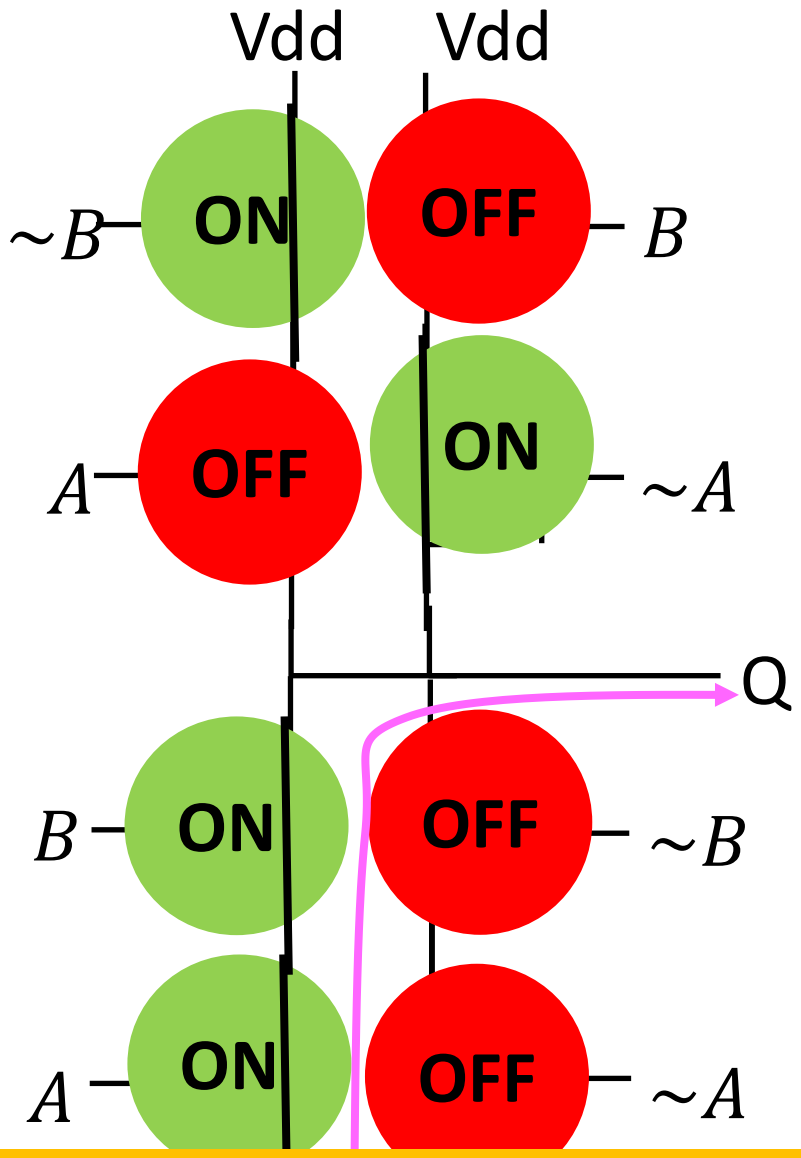
A	B	Q
0	0	



A	B	Q
0	0	0
0	1	



A	B	Q
0	0	0
0	1	1
1	0	



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

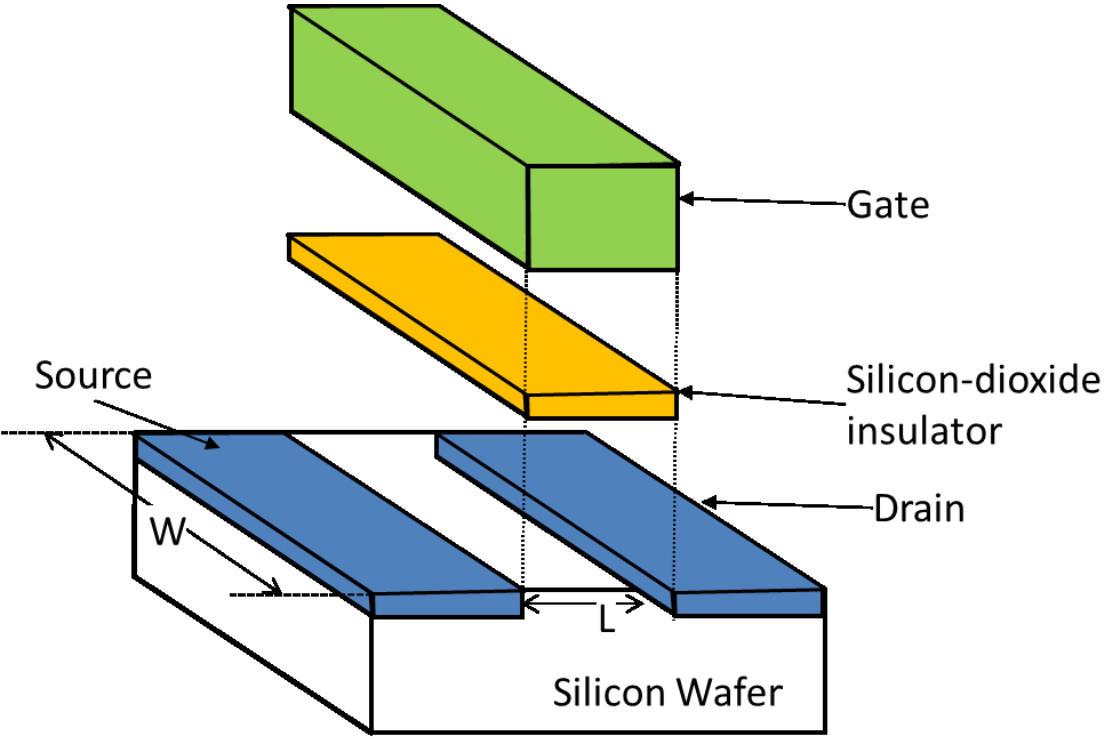
That is an 8 transistor XOR gate!

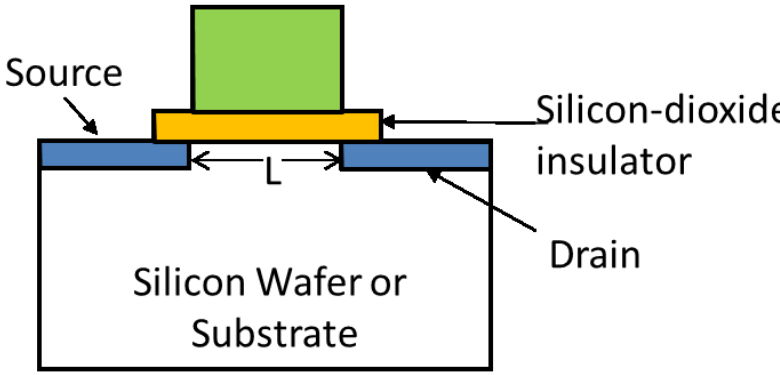
Block	# Transistors
Basic elements	
NAND2	4
NOR2	4
NOT	2
AND2	6
OR2	6
AND (n inputs)	2n+2
OR (n inputs)	2n+2
MUX	40
Combined logic gates	
FA 1-bit	74
HA 1-bit	6
1-bit REG	40
3-to-8 Decoder	68
8-to-3 Encoder	30

Datapath modules	
FA 8-bit	592
CHECKZ 8-bit	32
NOT 8-bit	16
MUX 8-bit	320
8-bit REG	320
Microarchitecture blocks	
ALU	1000
Incrementor	48
State machine controller (control sigs)	274
State machine controller (next state)	1,450
Total AUX regs (9 8-bit REGS)	2,880
RF (32 8-bit REGs)	10,240
PM (16384 1-bit REGs)	655,360
RAM (16384 1-bit RGEs)	655,360
Total	**1,326,612**

	# Transistors	Year	Transistor size	Chip size
Intel 4004	2,300	1971	10 micron	12 mm2
Intel 8086	29,000	1978	3 micron	33 mm2
Zilog Z80	8,500	1976		
Intel 80386	275,000	1985	1.5 micron	104 mm2
Pentium	3,100,000	1993	0.8 micro	294 mm2
Apple A7 (dual-core ARM64 "mobile SoC")	1,000,000,000	2013	28 nm	102 mm2
18-core Haswell	5,560,000,000	2014	22 nm	363 mm2

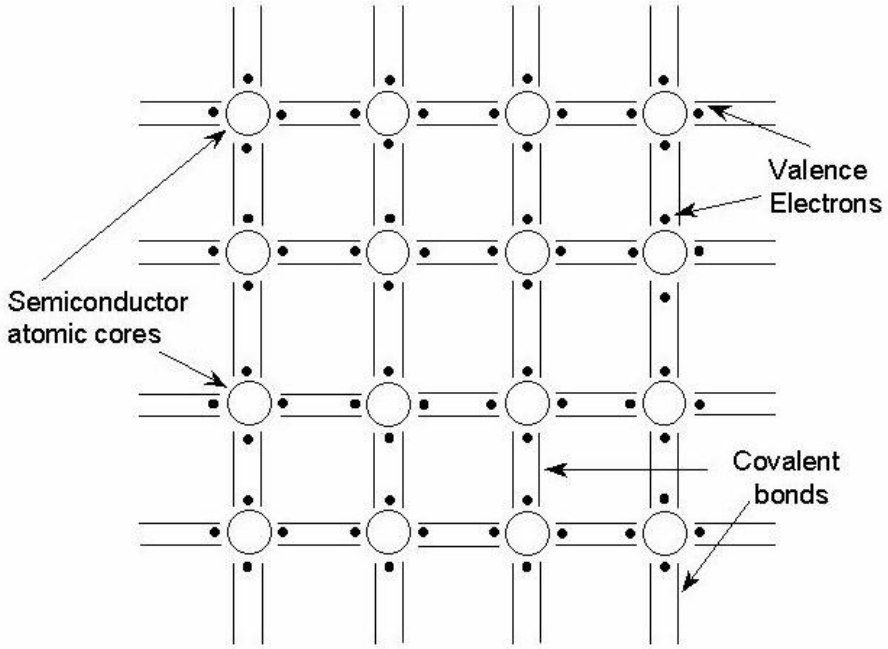
Transistor physical diagram





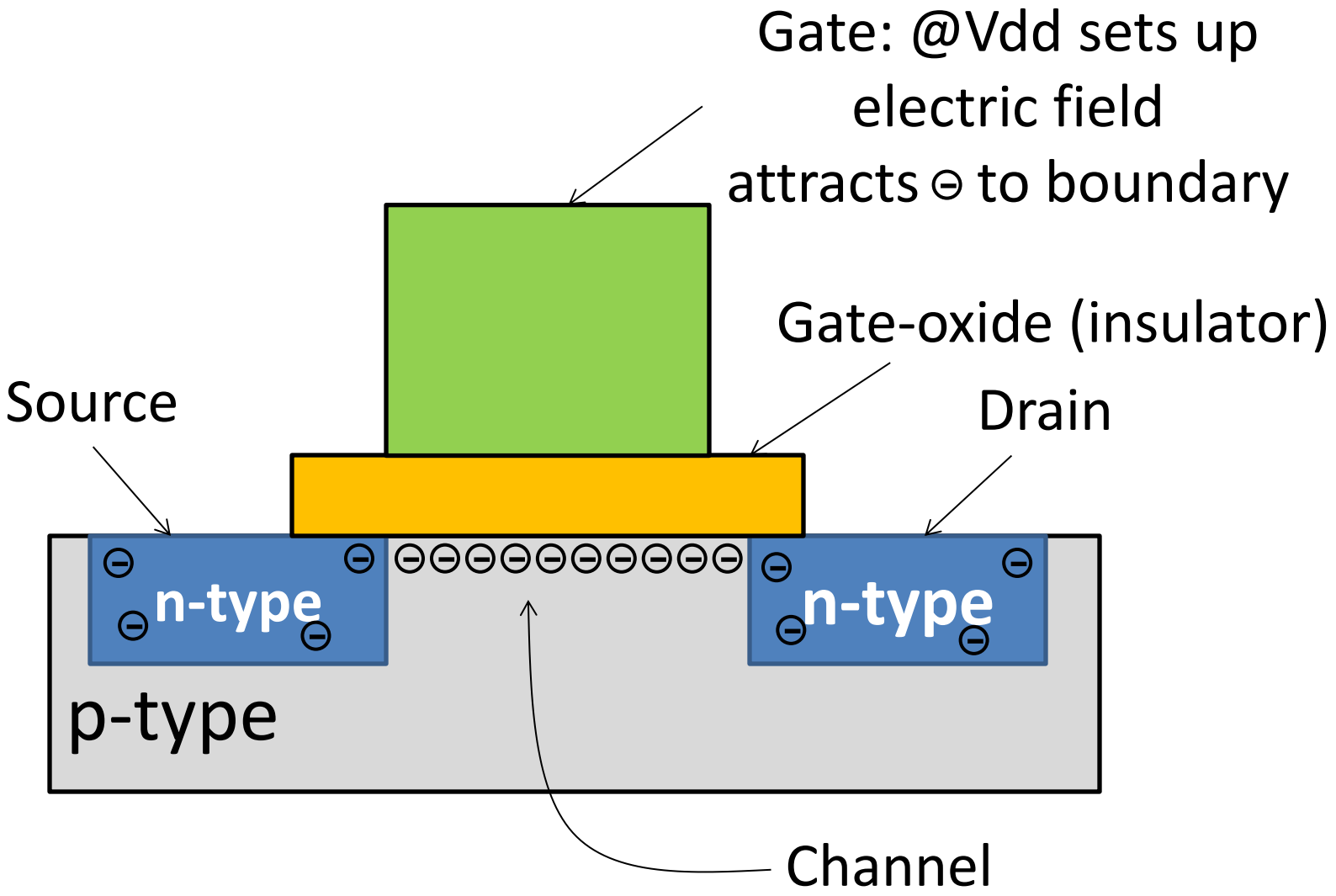
Side view

- Silicon by itself is semiconductor
  - Has 4 valence electrons and forms a co-valent bond with 4 neighbors
  - Hard to break and does not conduct ☹



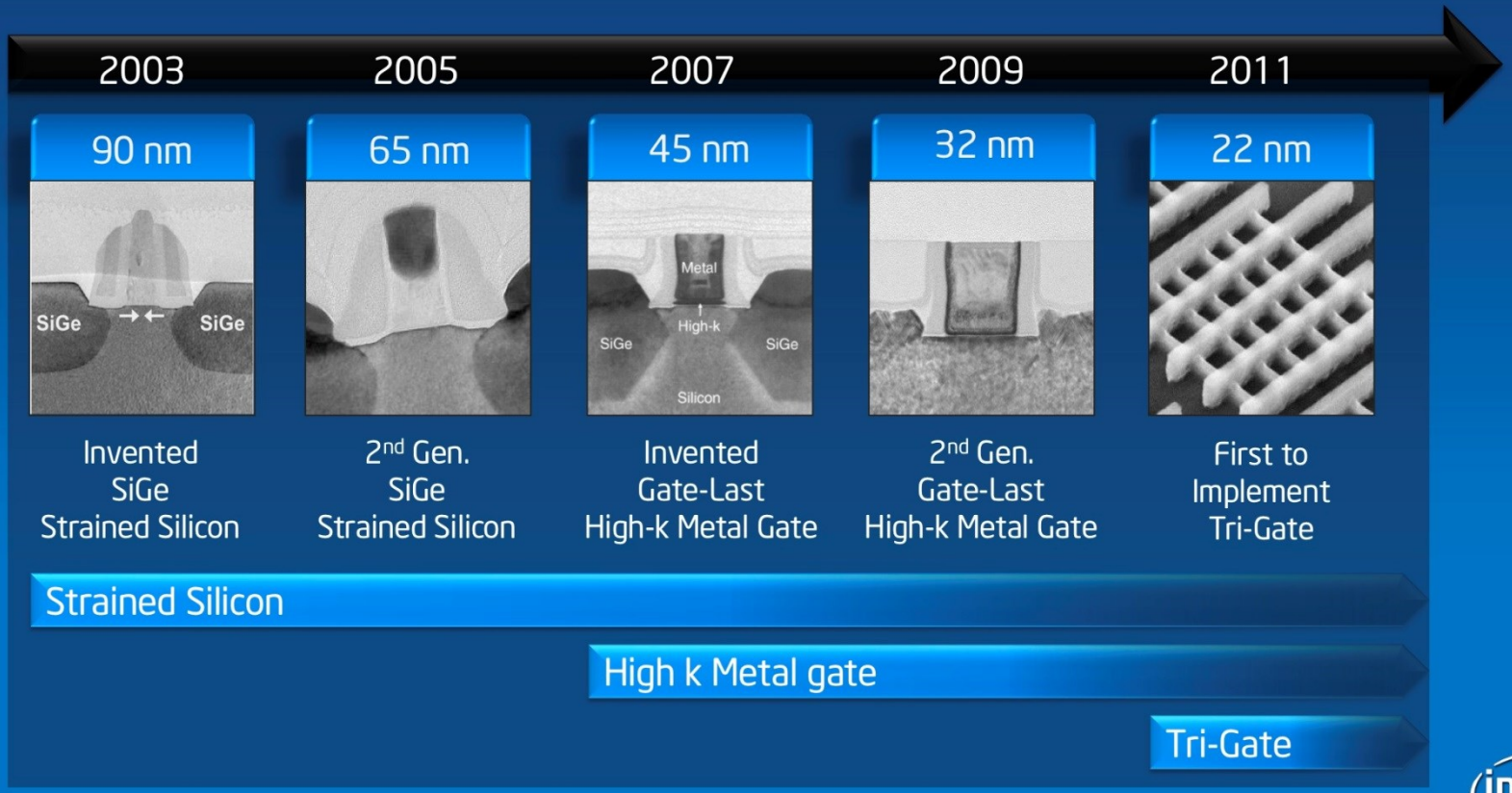
- Silicon by itself is insulator
  - Has 4 valence electrons and forms a co-valent bond with 4 neighbors
  - Had to break and does not conduct ☹
- Silicon + Arsenic makes it filled with electrons and conducting
- Silicon + Boron makes it filled with “holes” and conducting

Transistor Operation



“Miracle Month” of November 17 to December 23, 1947

Transistor Innovations Enable Technology Cadence



Source: Intel

Moore's Law

- Number of transistors that can be cost-effectively integrated will double every 18 months
  (revised to 24 and 36 months later)
- In practice:
  - Reduce the Length and width by 1.41
  - Area reduces by 2X
  - Can also reduce the thickness of the gate-oxide

Dennard Scaling

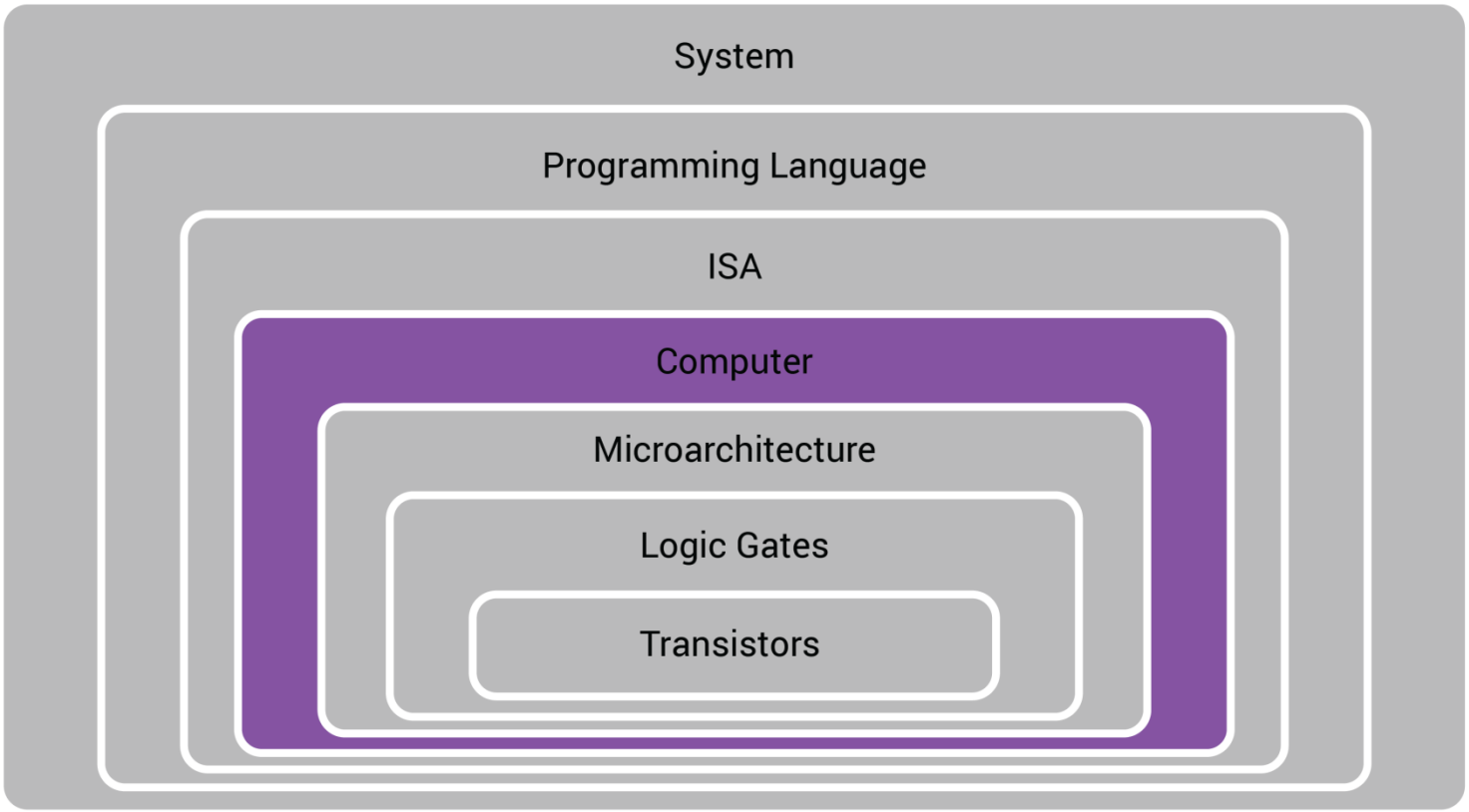
- Voltage can be reduced linearly with the channel Length
- Remember Moore's Law:
  - Since gate oxide thickness also reduces, capacitance reduces linearly
- Power consumption = $C * V^2 * Frequency$
- As C and V are each reduced by a factor of X every generation of transistors:
  - Power reduces by a cubic factor
  - Area reduces by a square

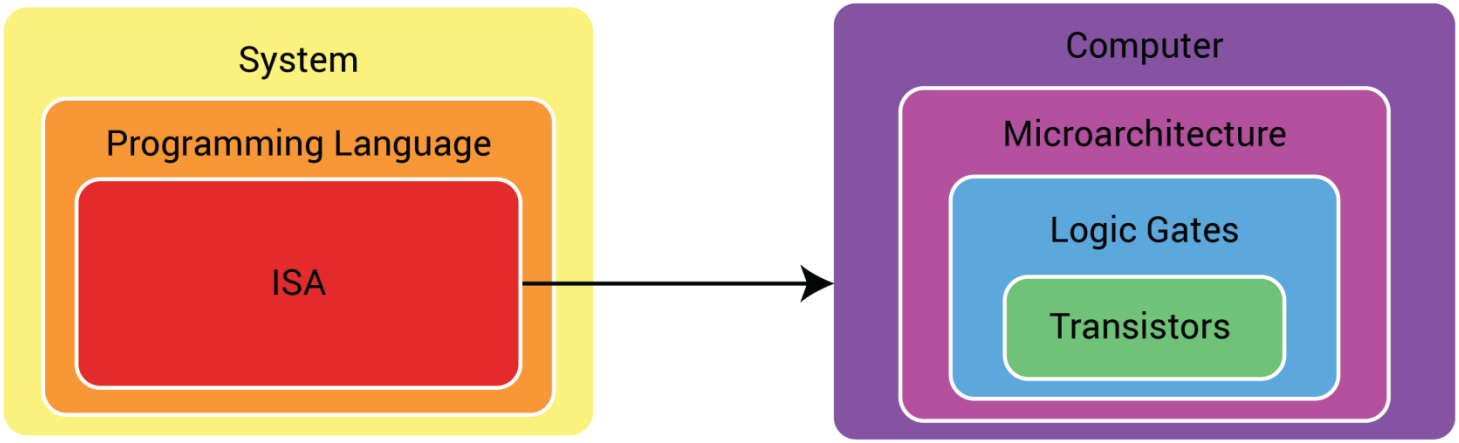
Bad news

- Dennard's scaling has ended
  - No more power benefit from building smaller transistors
- Moore's law is also likely ending or ended

This is GOOD news!

More than ever it is important to know how to use gates, transistors, microarchitecture to build power-efficient and high-performance computers!


System
Programming Language
ISA
Computer
Microarchitecture
Logic Gates
Transistors


System
Programming Language
ISA
Computer
Microarchitecture
Logic Gates
Transistors

CS 252

Lecture 33; 2015 Dec 7th; Transcribed Lecture Notes

Transistors

Announcements

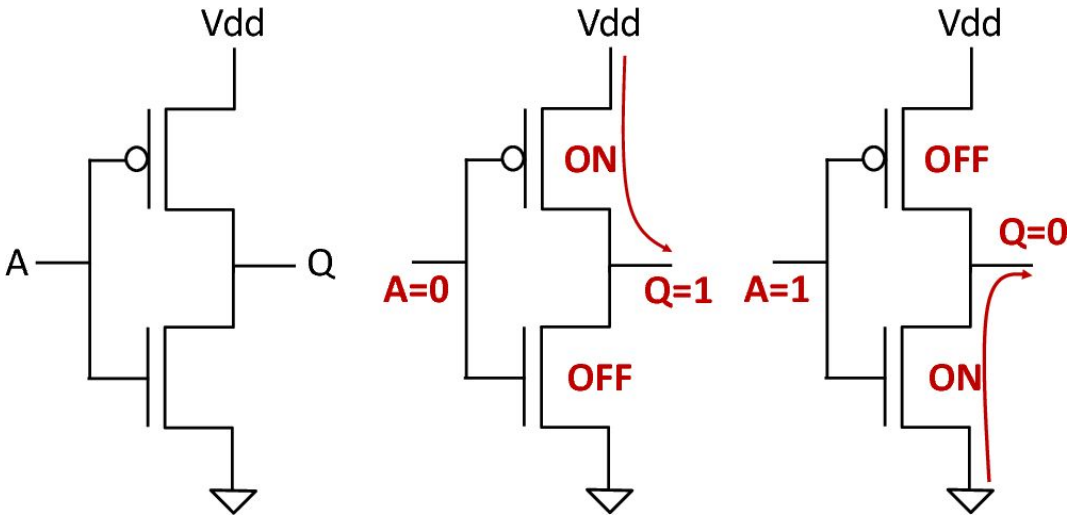
survey at end of class today
homework 8 due Friday, December 11th

Outline

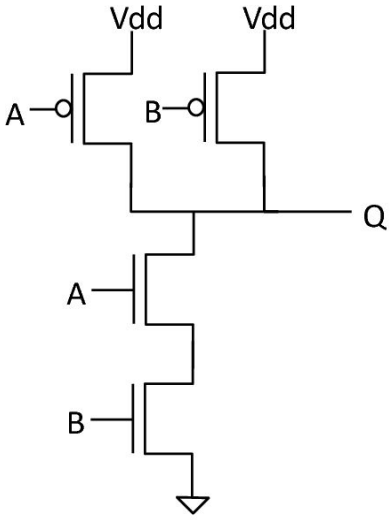
state transition diagram (Figure 8.1.5.4 and Figure 8.1.5.5)
transistors
    digital behavior
    simple rules
    truth table
book survey

Transistor

3 terminals:
    gates (nothing to do with logical gate)
    source
    drain
Turns on or off depending on the voltage at gate
    N-type transistor is turned on when gate input is high (1)
    P-type transistor is turned on when gate input is low (0)
Fails in 8 through 10 years
An inverter with transistors (figure below)

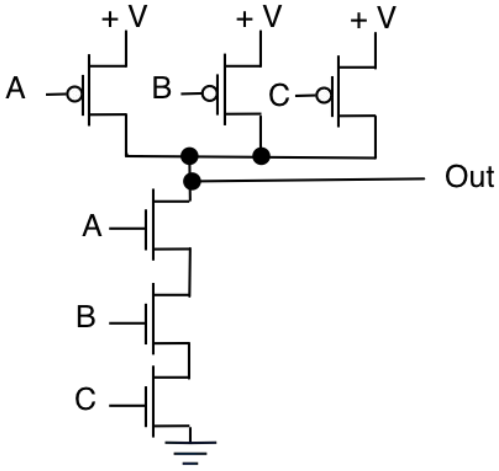


A 2-input NAND gate with transistors (figure below)

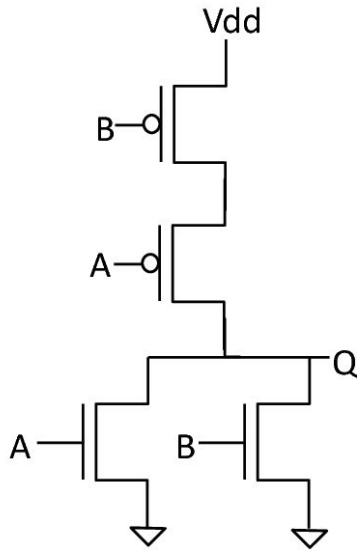


NAND Gate

A 3-input NAND gate with transistors (figure below)



A 2-input NOR gate with transistors (figure below)



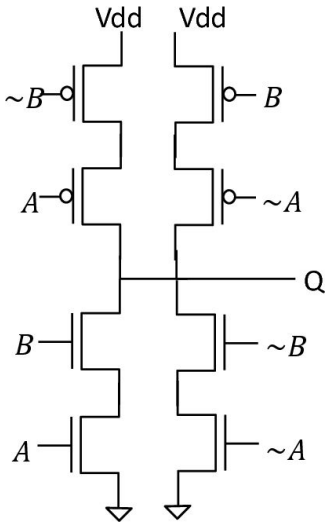
NOR Gate

Delays (NOT ON EXAM)

having 2 paths means more current and faster

gates delays and transistor delays vary based on inputs

A 2-input XOR gate with transistors



Transistor count

Basic elements

NAND2 (2-input NAND gate) takes 4 transistors

NOR2 takes 4 transistors

...

Combined logic gates

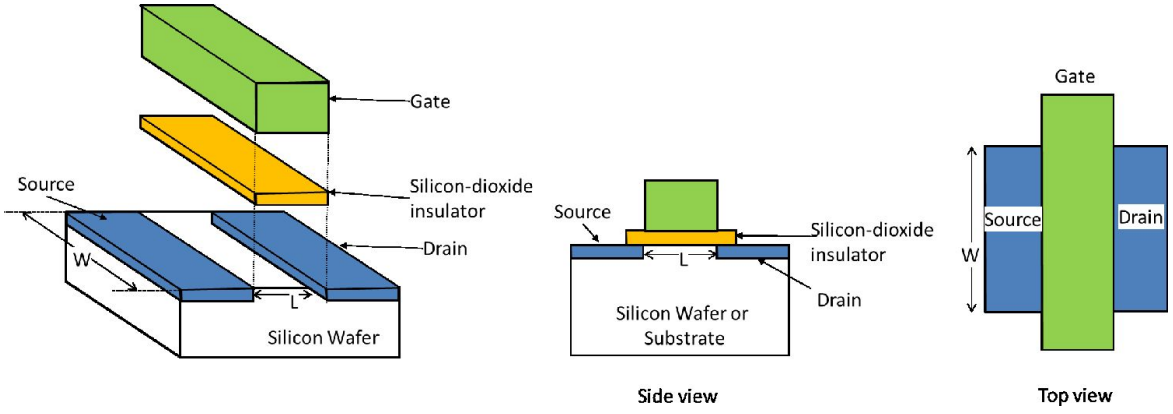
FA 1-bit takes 74 transistors

...

...

Total takes 1,326,612 transistors

Transistor physical diagram

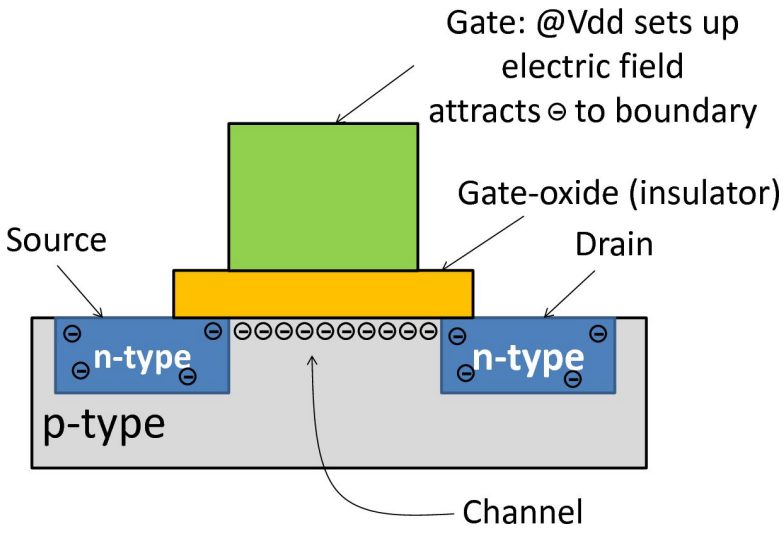


gate oxide allows the gate to set up an electrical field for electrons to flow

distance between source to drain is the length and technology node

width is usually twice the length

build faster transistor by increasing width



the insulator (shown in yellow in the figure above) prevents electrons from flowing to gate terminal

transistor acts like a switch, capable of representing 0 and 1, so binary logic

World's first transistor experiments ran from Nov 17th to Dec 23rd in 1947.

Transistor innovations enable technology cadence

finFET uses multiple insulators to create electric field, used for <28nm transistors

Moore's law: an observation made by Gordon Moore that it will be cost effective to double the number of transistors on a single chip every 24 months

In practice, reduce length and width by 1.41X to reduce area by 2X, and reduce thickness

Dennard scaling: while you make a transistor smaller, you can also reduce the supply voltage of the transistor

Power consumption = $CV^2 frequency$

Bad news: Dennard scaling has ended as we can't simply reduce voltage anymore

Moore's law is also likely ending

Good news: good for this field since it is important to use transistor efficiently to build power-efficient and high-performance computers