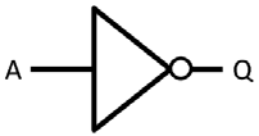
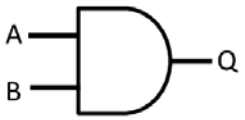
NOT GATE



A	B	Q
0	0	1
0	1	0

Text notation: ~

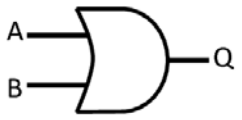
AND GATE



A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

Text notation: ·

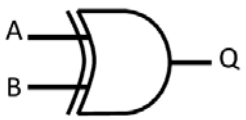
OR GATE



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

Text notation: +

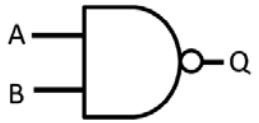
XOR GATE



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

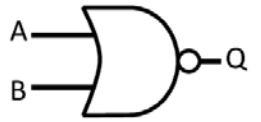
Text notation: ⊕

NAND GATE



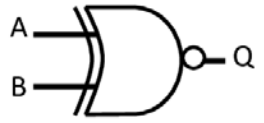
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

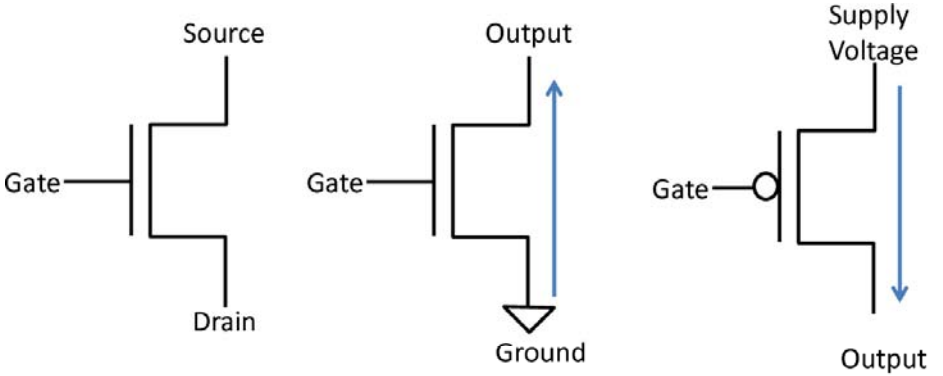
XNOR GATE



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Using other gates

De Morgan's law	~(AB) = ~A + ~B ~(A + B) = (~A)(~B)



Transistor terminals

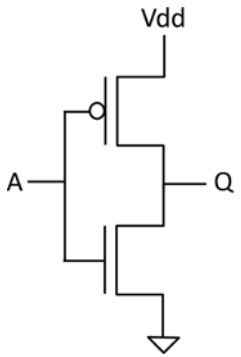
N-type transistor

Gate	Behavior
1	Closed Output=0
0	Open Output=Z

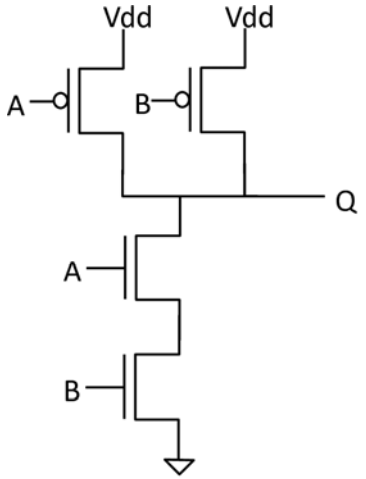
P-type transistor

Gate	Behavior
0	Closed Output=1
1	Open Output=Z

NOT

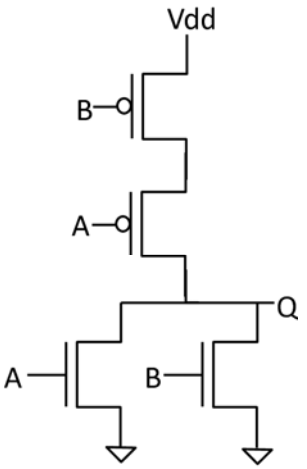


NAND



NAND Gate

NOR



NOR Gate