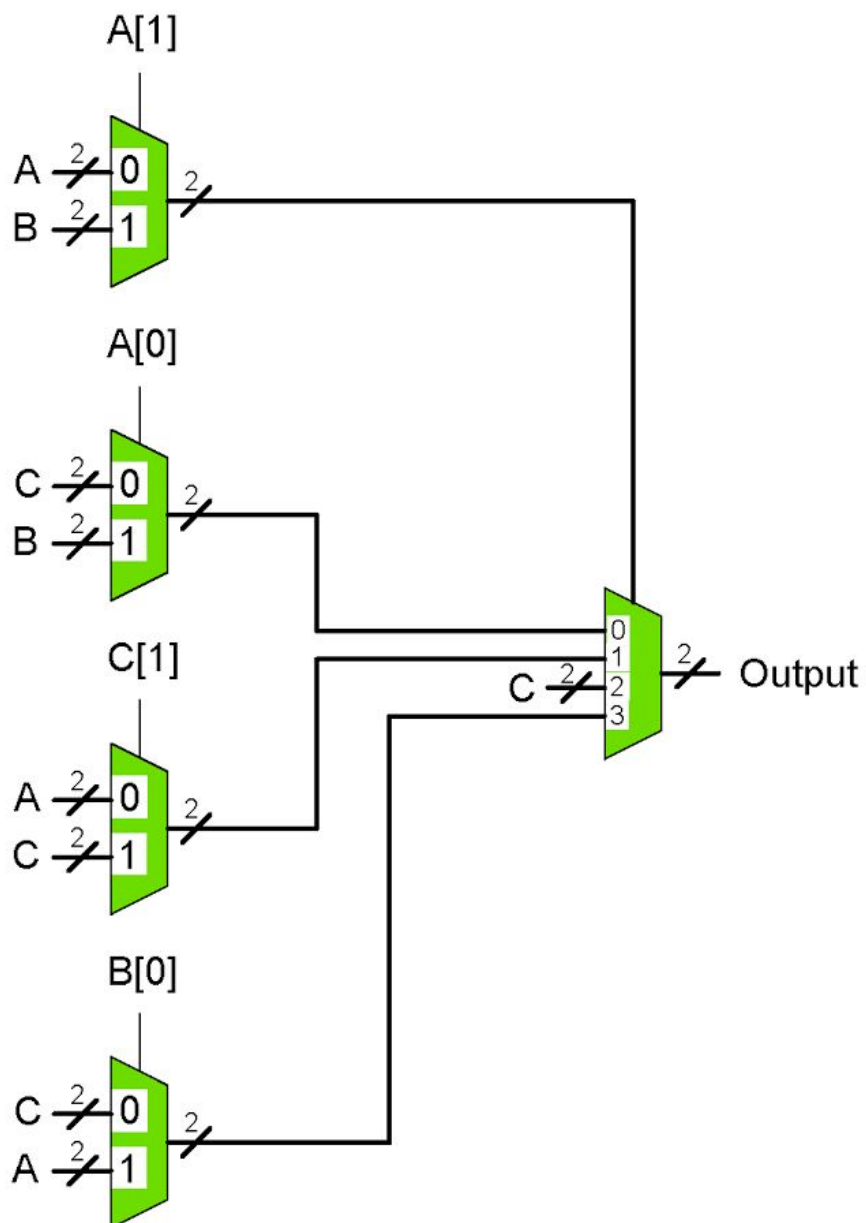


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1. What is microarchitecture?

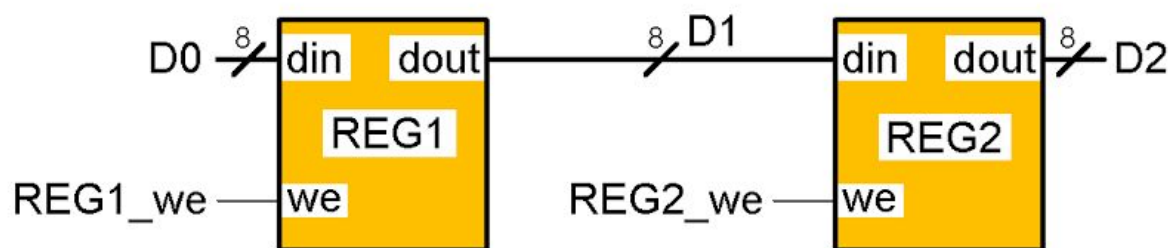
2. The diagram below shows many muxes. If $A = 0b10$, $B = 0b11$, and $C = 0b00$, then what is Output?



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3. In the diagram below shows 2 registers (REG1 and REG2), 3 inputs (D0, REG1_we, and REG2_we), and 2 (intermediate) outputs (D1 and D2). Complete the table below.

Time	0	1	2	3	4	5	6	7
D0	1	2	3	5	8	13	21	34
REG1_we	0	1	0	1	0	1	0	0
REG2_we	0	0	1	1	1	0	0	1
D1	55							
D2	89							



4. Encode the following from assembly to machine code.

```

subi r28,1      ; decrement down counter
breq 1          ; go print 1s counter if done with 8 bits
rjmp -8         ; loop to check next bit

```

5. Decode the following from machine code to assembly.

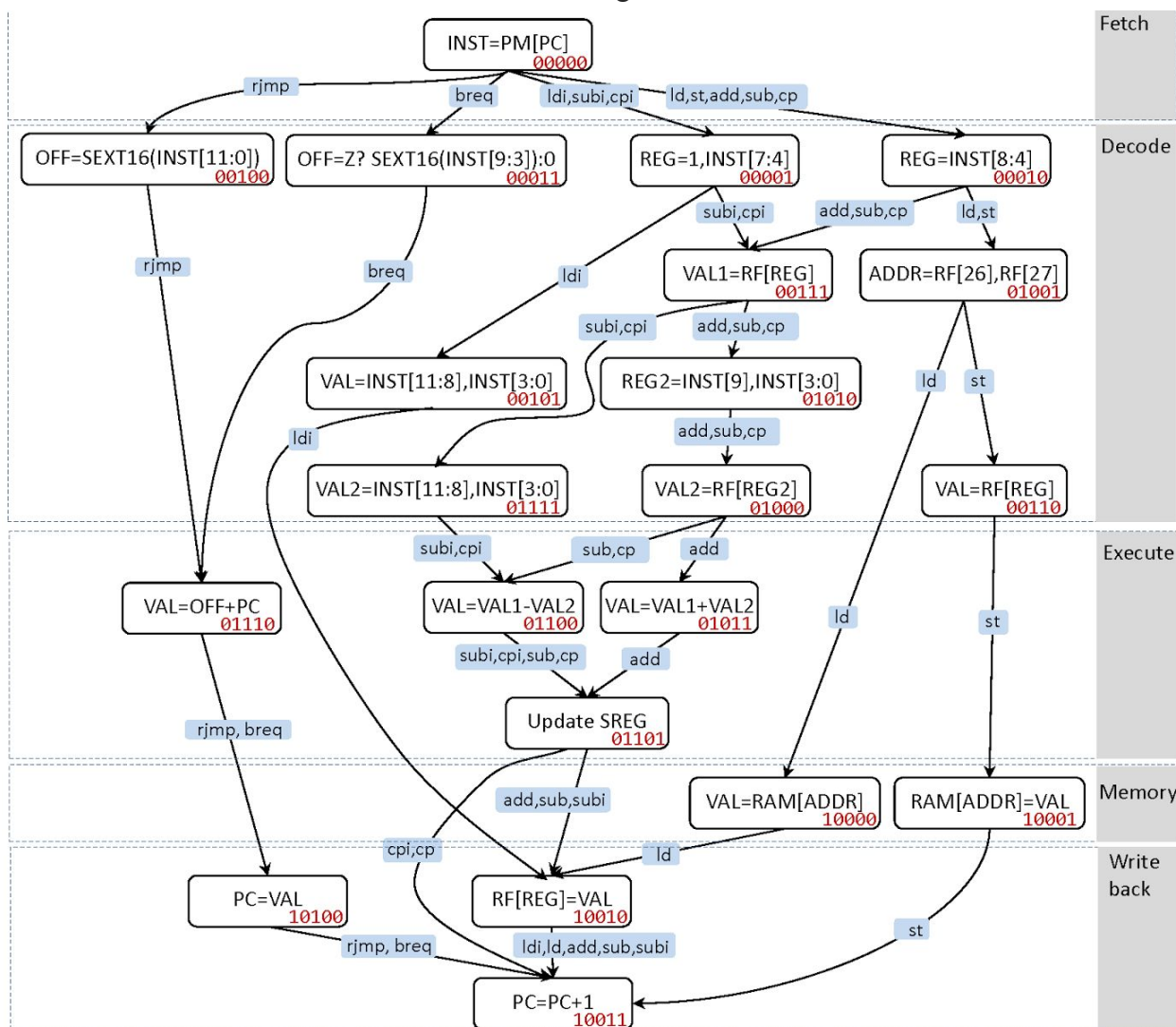
```

1110000011001000 (0xE0C8)
0010111111011110 (0x2FDE)

```

6. This question walks through the process of implementing a new instruction in our microarchitecture. That new instruction will be asr (arithmetic shift right). There is more than 1 correct answer.

a. Describe any/all new states we need to add to our state machine to implement asr. Draw/include them in the state machine diagram below.



b. If you have nothing better to do over this weekend, then think about (or repeat) part a for different instructions.

- and
- andi
- com
- dec

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7. Trace the following instructions (they are borrowed and modified from lecture26-27). Do not be concern with the cycle (i.e. it is okay to start from either 0 or 1. It is also okay with either reset it after each instruction or continue counting up for the entire program).

```
ldi r16, 45      ; 0xE20D
ldi r17, 23      ; 0xE117
ldi r18, 11      ; 0xE02B
add r17, r18     ; 0x0F12
cp r17, r16      ; 0x1710
breq 4           ; 0xF021
rjmp -4          ; 0xCFFC
```

[illegible]

