Homework 5 - Due at Lecture on Wednesday, March 21

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You must do this homework in groups of **two**. Please hand in ONE copy of the homework that lists the **section number**, **full** names (as they appear in Learn@UW) and **UW ID** numbers of all students. You must **staple** all pages of your homework together to receive full credit

Problem 1 (4 points)
The following LC-3 Program has been loaded into memory:

ADDRESS	INSTRUCTION
x5000	1001 0010 0011 1111
x5001	0001 0010 0110 0001
x5002	0001 0010 0100 0010
x5003	0000 0110 0000 0110

a. If the initial contents of the registers are:
R0 is 4; R1 is 3; R2 is 0; R3 is 5.
Which condition codes are set and what is the value of PC after the instruction at 0x5003 is executed?

b. If the initial contents of the registers are:
R0 is 3; R1 is 0; R2 is 5; R3 is 4.
Which condition codes are set and what is the value of PC after the instruction at 0x5003 is executed?

Problem 2 (6 points)
Most ISAs have instructions that does nothing. It is usually called NOP (No Operation). The instruction is fetched, decoded and executed. But it does not do anything. State whether each of the following instructions could be used as NOP and explain why / why not. (Note: Each Instruction is executed individually, independent of each other).

a) 0001 1011 0110 0000
b) 0001 1010 1110 0000
c) 0101 1001 0000 0100
d) 0101 0010 0110 0000
e) 0101 1111 1111 1111
f) 0000 0000 0010 1101

Problem 3 (3 points)

Assume a memory has an addressability of 64 bits. What does that tell you about the size of the MAR and MDR?

Problem 4 (4 points)

The program below performs multiplication via repeated addition on registers R1 and R2 and stores the result in R0 (i.e. R0 ← R1 * R2). Enter the missing machine language instructions and comments to complete the code (All lines should be commented).

ADDRESS	ISA INSTRUCTION
x3000	0101 0000 0010 0000 ; Clear R0
x3001	0001 0010 0110 0000 ; R1 ← R1 + 0
x3002	0000 0100 0000 0011 ; BRz x3006
x3003	0001 0000 0000 0010 ;
x3004	
x3005	
x3006	1111 0000 0010 0101 ; TRAP

Problem 5 (4 points)

An LDR instruction, located at x4000, uses R4 as its base register. The value currently in R4 is x4022.

a. What is the largest address that this instruction can load from?

b. Suppose we redefine the LDR offset to be zero-extended unsigned number, rather than sign-extended 2's complement number. Then what would be the largest address that this instruction could load from?

c. With the new definition of part b, what would be the smallest address that this instruction could load from?

Problem 6 (3 points)

Express the final value in register R0 in terms of R1 and R2 (e.g. R0 = R1 + R2) after the execution of the following program.

0001 1010 0100 0001
0001 1100 1010 0010
1001 1101 1011 1111
0001 1101 1010 0001
0001 0001 0100 0110

Problem 7 (6 points)

We are about to execute the following program.

ADDRESS	ISA INSTRUCTION
x3000	1110 0000 0001 0100 ; LEA R0, x014
x3001	0010 0010 0001 0100 ; LD R1, x014
x3002	0110 0100 0000 0010 ; LDR R2, R0, x02
x3003	1010 0110 0001 0001 ; LDI R3, x011

x3004	1111 0000 0010 0101 ; HALT

The State of the Machine before the program starts is given below:

MEMORY ADDRESS	MEMORY CONTENTS
x3010	x9876
x3011	x3258
x3012	x0000
x3013	x4567
x3014	x3017
x3015	x3018
x3016	x92FE
x3017	x92FF
x3018	x0020
x3019	x1220
x301A	x0001

What will be the final contents of registers R0 to R3 when we reach the HALT instruction? Write your answers in **hexadecimal** format. The initial register contents are given below.

REGISTER	INITIAL CONTENTS	FINAL CONTENTS
R0	x200E	
R1	x200E	
R2	x3001	
R3	x3001	