Homework 3 - Due at Lecture on Fri, Feb 24

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You must do this homework in groups of **two**. Please hand in ONE copy of the homework that lists the **section number**, **full** names (as they appear in Learn@UW) and **UW ID** numbers of all students. You must **staple** all pages of your homework together to receive full credit

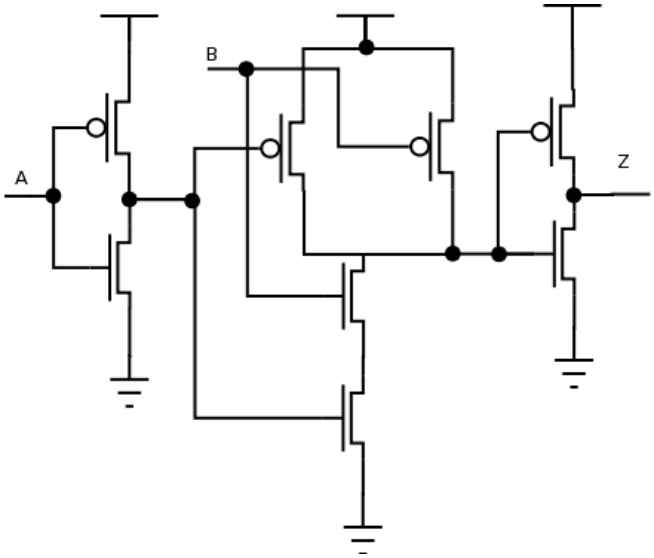
Problem 1 (2 points)

a. What is the decimal equivalent of the following IEEE floating point number: **0x42F74000**
123.625

b. What is the 32-bit IEEE floating point representation of the decimal number **-629.375**?
0xC41D5800

Problem 2 (4 points)

Given the following transistor level circuit:



a. Fill out the truth table for Z

A	B	Z
0	0	0
0	1	1
1	0	0
1	1	0

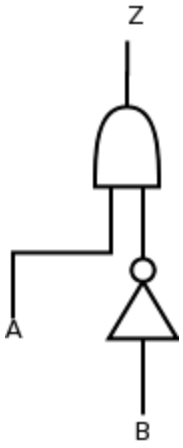
b. What is Z in terms of A and B
Z = NOT (A) AND B

Problem 3 (4 points)
Given the logic equation Z = A AND NOT(NOT(A) OR B)

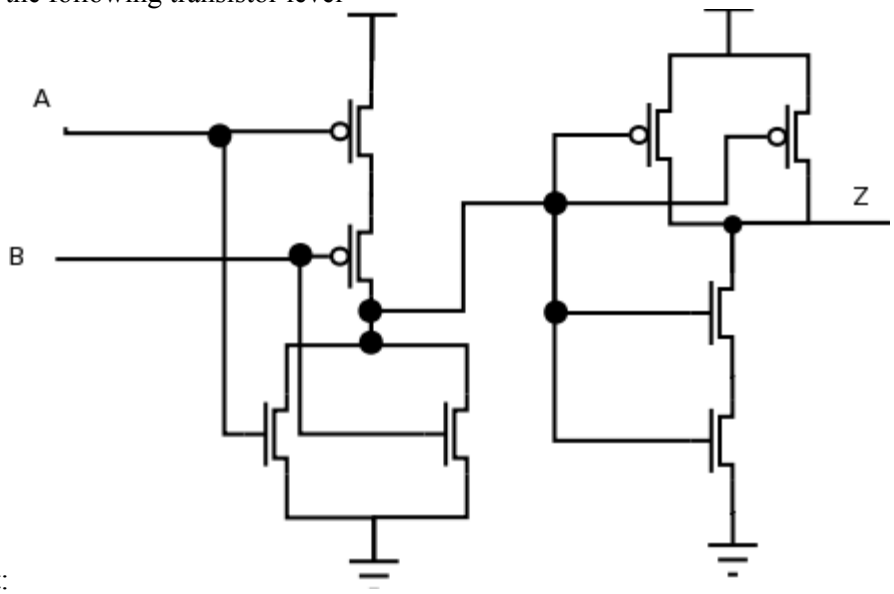
a. Fill out the truth table for Z

A	B	Z
0	0	0
0	1	0
1	0	1
1	1	0

b. Draw the gate-level circuit for Z using 2-input AND/OR gates and NOT gates



Problem 4 (4 points)
Given the following transistor level



circuit:

a. Fill out the truth table for Z

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

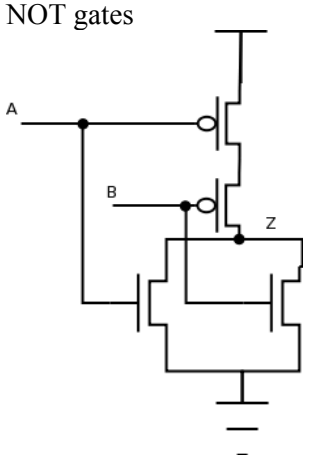
b. What is Z in terms of A and B
Z = A OR B

Problem 5 (4 points)
Given the logic equation Z = NOT(A OR (NOT(A) AND B))

a. Fill out the truth table for Z

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

b. Draw the transistor-level circuit for Z using a **minimal** number of 2-input NAND/NOR gates and NOT gates

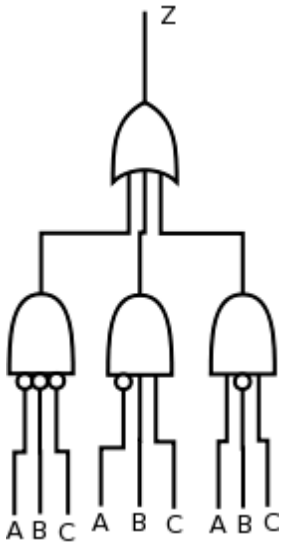


Problem 6 (6 points)
Suppose A, B, and C are inputs to logic function Z with the following truth table:

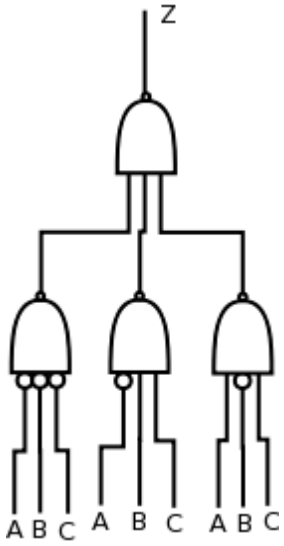
A	B	C	Z

0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

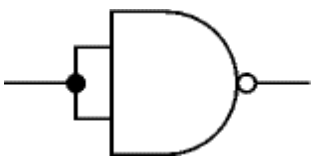
a. Draw the gate-level circuit using NOT gates and 3-input AND and OR gates.



b. Convert the circuit of part a into one that uses only NAND gates.



Where the bubbles =



Problem 7 (2 points)
Suppose A, B, and C are inputs to a logic function that outputs Z = 1 when the total number of 1s among the inputs is exactly two.

Fill out the truth table for Z:

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Write the logic expression for Z (e.g. Z = A AND B)
Z = (NOT(A) AND B AND C) OR (A AND NOT(B) AND C) OR (A AND B AND NOT(C))

Problem 8 (2 points)
If the number of address bits in memory is increased by 4 bits and the addressability is halved, how is the size of memory affected?

Size of memory = 2^(# address bits) * addressability
Thus, the new size of memory is 2^4*2^-1 times the old size -> 2^3 = 8 times larger than before