

CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Examination 2

In Class (50 minutes)

Friday, Mar 09, 2012

Weight: 17.5%

NO: BOOK(S), NOTE(S), CALCULATORS OF ANY SORT.

This exam has 12 pages, including a blank page at the end. Plan your time carefully, since some problems are longer than others. You must turn in pages 1 to 11.

LAST NAME: _____

FIRST NAME: _____

SECTION: _____

CAMPUS ID# _____

EMAIL ID _____

Question	Maximum Points	Points
1	2	
2	2	
3	4	
4	4	
5	4	
6	5	
7	4	
8	3	
9	2	
Bonus	3	
Total (excluding bonus)	30	

Problem 1 (2 Points)

Write the AND-OR logic expression for the output Y, as a function of the inputs A, B, and C, corresponding to the following truth table. You need not simplify the expression.

(AND-OR logic expression is of the form $Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \dots\dots\dots$), where $\bar{A}$ is NOT (A).

Inputs			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

Problem 2 (2 Points)

Suppose a 64-bit instruction takes the following format:

OPCODE	DR	SR1	SR2	UNUSED
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If there are 525 opcodes and 265 registers,

- a. What is the minimum number of bits required to represent the OPCODE?

$$525 < 2^{10} \Rightarrow \mathbf{10 \text{ Bits.}}$$

- b. What is the minimum number of bits required to represent the Source Register, SR1?

$$265 < 2^9 \Rightarrow \mathbf{9 \text{ Bits.}}$$

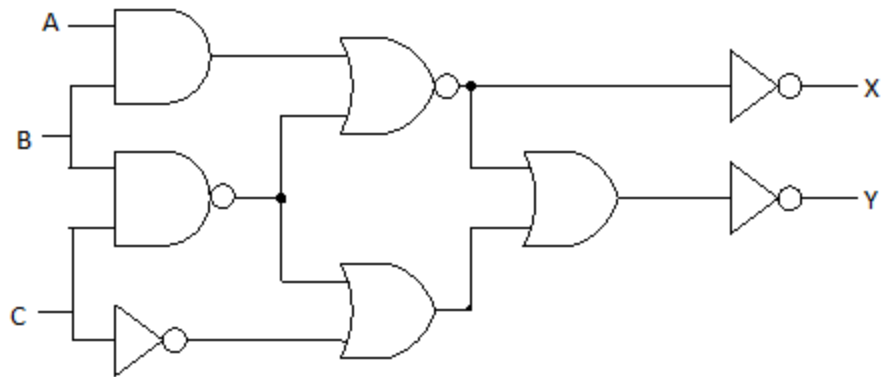
- c. What is the minimum number of bits required to represent the Destination Register, DR?

$$265 < 2^9 \Rightarrow \mathbf{9 \text{ Bits.}}$$

- d. What is maximum number of UNUSED bits in the instruction encoding?

$$(64 - 10 - 9 - 9 - 9) = \mathbf{27 \text{ Bits.}}$$

Problem 3 (4 Points)



For the gate level circuit shown, fill out the following truth table for X and Y.

Inputs			Outputs	
A	B	C	X	Y
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The logic equation reduces to $X = A + \bar{B} + \bar{C}$ and $Y = ABC$.

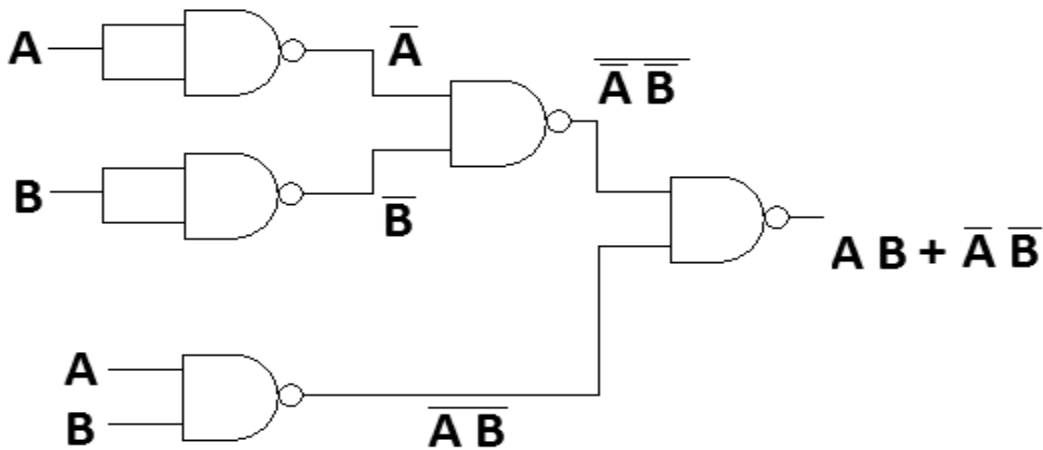
Problem 4 (4 Points)

Design a gate level circuit which takes two inputs A and B and gives an output of '1' if both the inputs are same and '0' otherwise. Use exactly 5 two input NAND Gates. No other gates are allowed. (Show all the steps to get Partial credits).

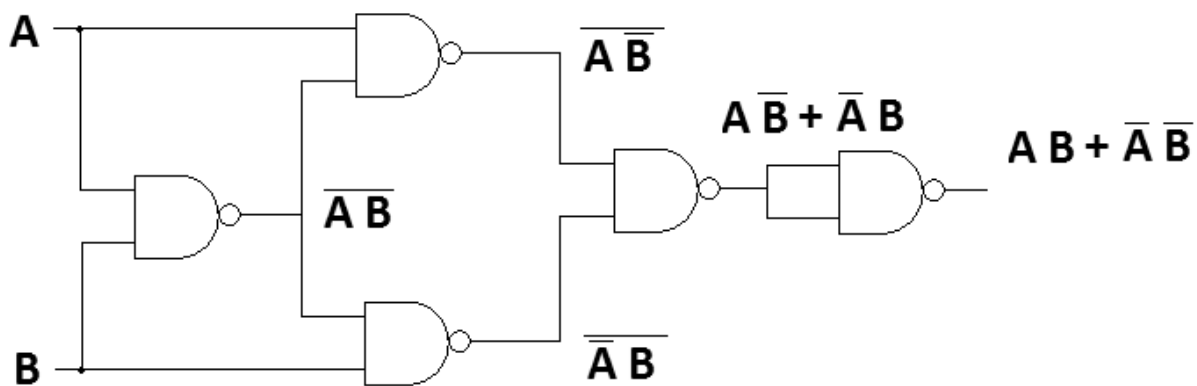
Hint: First draw the truth table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Two Possible Solutions.

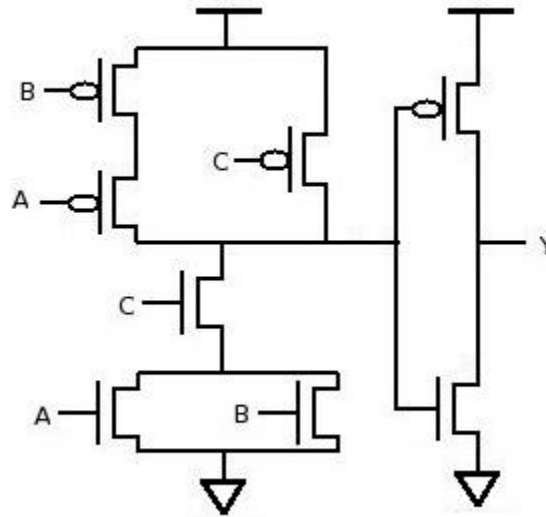


(OR)



Problem 5 (4 Points)

Given the transistor level circuit below:



a) Fill out the following truth table.

Inputs			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b) Write the logical expression for the output Y with respect to inputs A, B, and C.

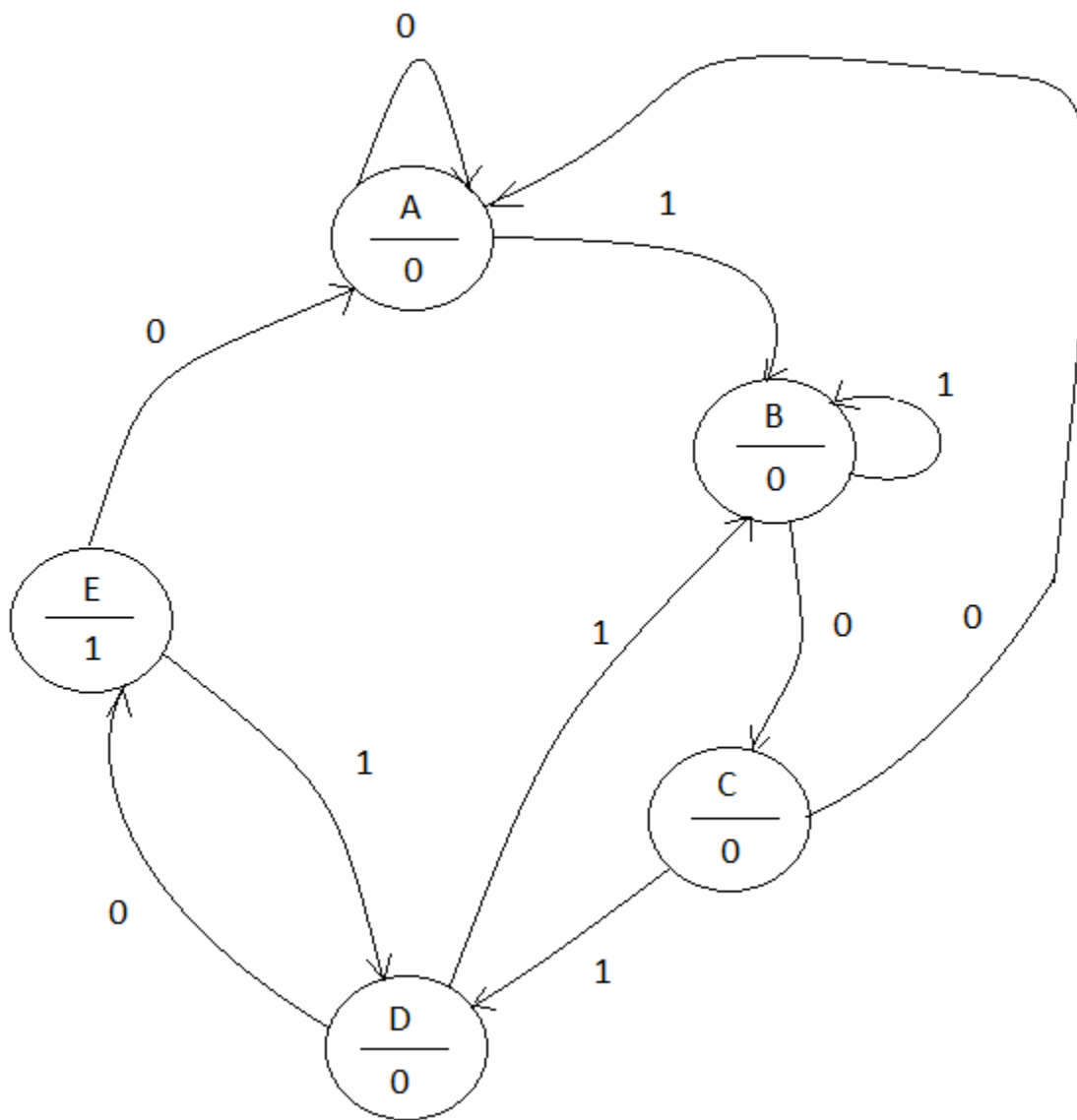
$$Y = (A + B) \cdot C$$

Problem 6 (5 Points)

Draw a finite state machine for recognizing the bit sequence “**1010**”. The machine takes one input every clock cycle which can be 1 or 0. The machine outputs a ‘1’ when the sequence **1010** is recognized; otherwise it outputs a ‘0’.

IMPORTANT: The machine should also recognize overlapping input sequences.

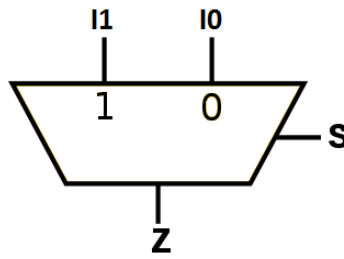
Sample Input	1010 1011 1101 0110
Sample Output	0001 0100 0000 1000



Problem 7 (4 Points)

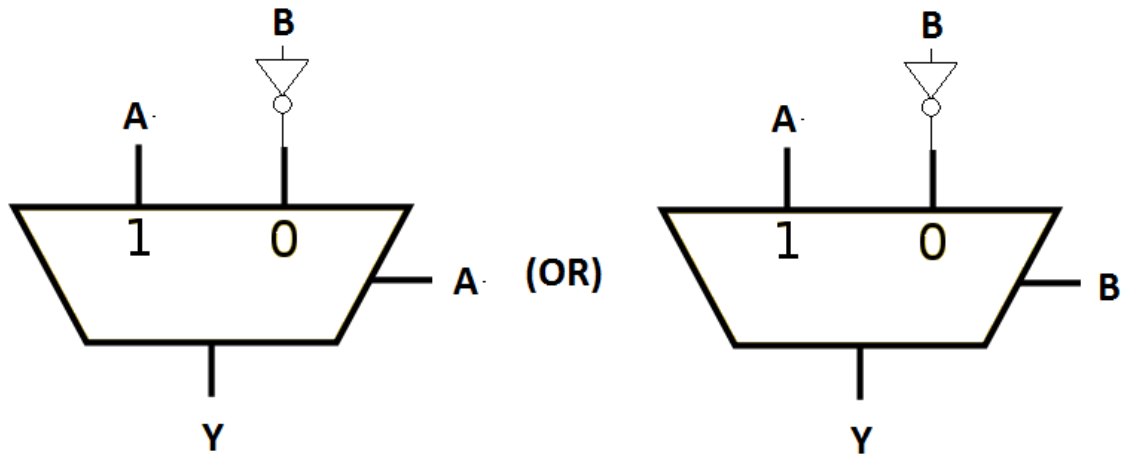
Implement the following truth table using **one** 2:1 MUX block and **one** NOT gate. No other logic gates or blocks should be used. **Do not connect logic '1' or logic '0' directly as input to the MUX.**

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1



2:1 MUX BLOCK

Two Possible Solutions.



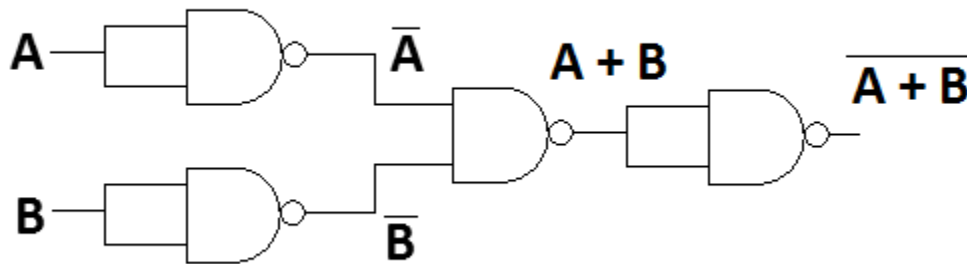
Problem 8 (3 Points)

- a. Minimum number of flip flops required to detect the 9-bit sequence “101000111” is **4**.
- b. Number of address bits required to address a memory with an address space containing 4096 locations is **12**.
- c. In a Von Neumann model machine, the Program Counter (PC) holds **the address of the next instruction**.

Problem 9 (2 Points)

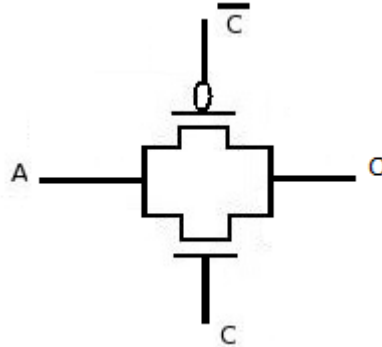
Assume that you have a set of NAND gates and no other logic gates are available. What is the minimum number of two-input NAND gates required to implement a two-input NOR function?

4 NAND gates are required.



Bonus Problem (3 Points)

a) What does the below circuit implement. Write its output in the form of a truth table. Inputs are A and C. Output is O.

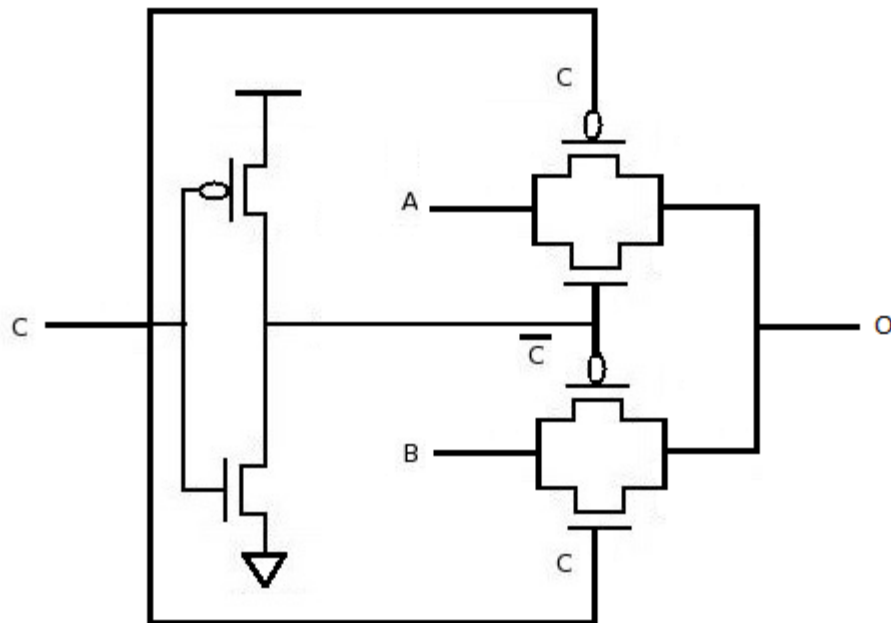


A	C	O
0	0	Z
0	1	0
1	0	Z
1	1	1

Z – High Impedance.

This is called a transmission gate. It transmits the value of A to the output when C is set to 1.

b) What does the below circuit implement. Write its output in the form of a truth table. Inputs are A, B, and C. Output is O. You will notice that it is using the circuit we showed in part



Inputs			Output
A	B	C	O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

This circuit implements a 2-input Multiplexer (2: 1 MUX) where C is the **Select** input. A is Input I0 and B is Input I1.

c) Write the output for the circuit in part (b) as a logic expression in terms of A, B, and C. You may use $\bar{A}$, $\bar{B}$, and $\bar{C}$ in this formula.

$$O = \bar{C}A + CB.$$

SCRATCH PAGE: