Problem 1 (6 points)

Write LC-3 instructions in hex for implementing the following tasks.

1. Move the value in R1 into R5 (Give a single instruction)
2. Store the 2's complement of R4 into R0 without overwriting R4
3. Load the value at 0x0003 into R1

Problem 2 (3 points)

Suppose the following LC-3 program is loaded into memory starting at location x30FF:

\[
\begin{align*}
\text{x30FF:} & \quad 1110 \ 0010 \ 0000 \ 0001 \\
\text{x3100:} & \quad 0110 \ 0100 \ 0100 \ 0010 \\
\text{x3101:} & \quad 1111 \ 0000 \ 0010 \ 0101 \\
\text{x3102:} & \quad 0001 \ 0100 \ 0100 \ 0001 \\
\text{x3103:} & \quad 0001 \ 0100 \ 1000 \ 0010 
\end{align*}
\]

If the program is executed, what is the value in R2 at the end of execution?

Problem 3 (2 points)

A memory’s addressability is 32 bits. What does that tell about the size of the MAR and MDR?

Problem 4 (2 points)

We wish to execute a single LC-3 instruction that will subtract the decimal number 18 from register 1 and put the result into register 2. Can we do it? If yes, show how it would be done. If not, explain why not.

Problem 5 (4 points)
Let’s say we have a memory consisting of 1024 locations and each location contains 16 bits.

a. How many bits are required for the address?

b. If we use the PC-relative addressing mode, and want to allow control transfer between instructions 25 locations away, how many bits of a branch instruction are needed to specify the PC-relative offset?

**Problem 6 (2 points)**

Consider a 16 bit processor (each instruction is 16 bits wide). A typical instruction looks like ADD Destination, Source 1, Source 2, where destination, source 1 and source 2 are registers. If the first 4-bits are used to differentiate instructions (Opcode), what is the maximum number of registers that the processor can support?

**Problem 7 (4 points)**

A LD instruction in LC-3 is located at 0x4200.

a. What are the largest and smallest addresses from where the data can be loaded using this instruction?

b. If LC-3 used unsigned number for offset instead of 2s complement number, what would be the largest and smallest address from where the data can be loaded using this instruction?

**Problem 8 (4 points)**

The LC-3 does not have an opcode for logical function OR. That is, there is no instruction in the LC-3 ISA that performs the OR operation. However, we can write a sequence of instructions to implement the OR operation. The four instruction sequence below performs the OR of the contents of register 1 and register 2 and puts the result in register 4. Fill in the two missing instructions so that the four instruction sequence will do the OR operation.

1)  1001 011 001 111111
2)  
3) 0101 110 011 000 101
4)  

**Problem 9 (3 points)**
What does the following LC-3 instruction do? (Be specific; that is, give specific register numbers or memory locations.)

<table>
<thead>
<tr>
<th>Address</th>
<th>Binary</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x450A</td>
<td>0011 0110 0000 0111</td>
<td>0x3607</td>
</tr>
</tbody>
</table>