CS/ECE 252: INTRODUCTION TO COMPUTER ENGINEERING

UNIVERSITY OF WISCONSIN—MADISON

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Midterm Examination 2

In Class (50 minutes)

Wednesday, March 12, 2014

Weight: 17.5%

NO: BOOK(S), NOTE(S), OR CALCULATORS OF ANY SORT.

The exam has **eleven** pages. **Circle your final answers**. Plan your time carefully since some problems are longer than others. You **must turn in the pages 1-11**. Use the blank sides of the exam for scratch work.

LAST NAME: ______________________________

FIRST NAME: ______________________________

ID# ______________________________

Problem 1 (4 points)

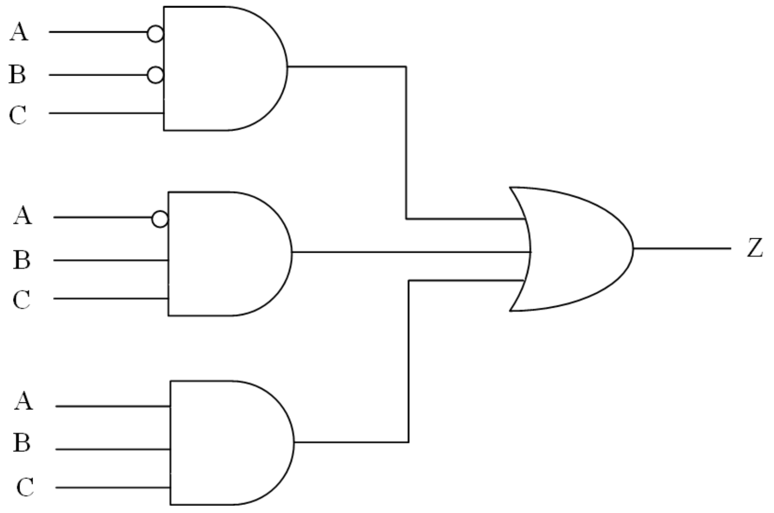
Use the truth table to answer the following questions.

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

a. (2 points) Write the Boolean expression for Z (in terms of A, B, and C) corresponding to the truth table. You don't need to reduce the expression.

Z = ((NOT(A)) AND (NOT(B)) AND C)) OR ((NOT(A)) AND B AND C) OR (A AND B AND C))

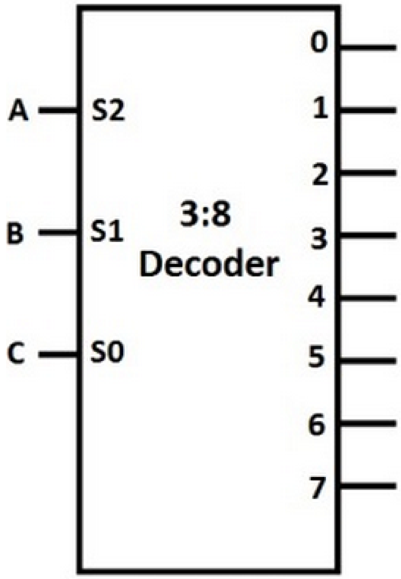
b. (2 points) Draw the logic gate-level circuit which corresponds to the truth table. Do not simplify the expression

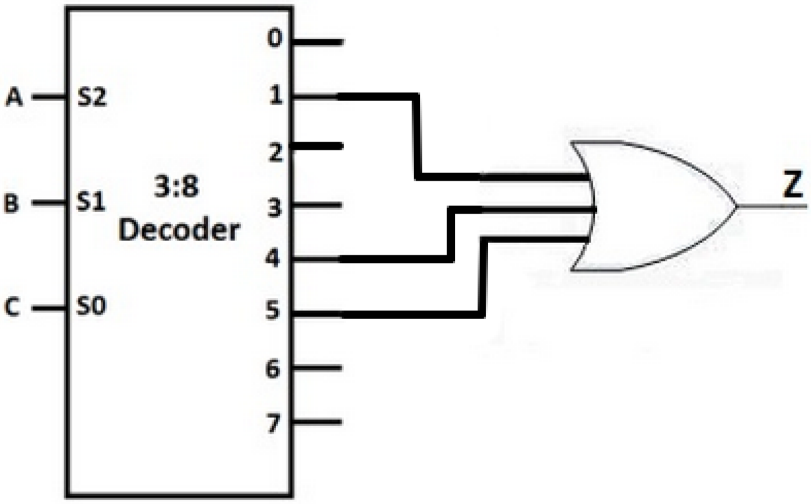


Problem 2 (3 points)

Implement the truth table below, with inputs A, B, and C and output Z, using a 3:8 decoder (as pictured below) and a 3-input OR gate.

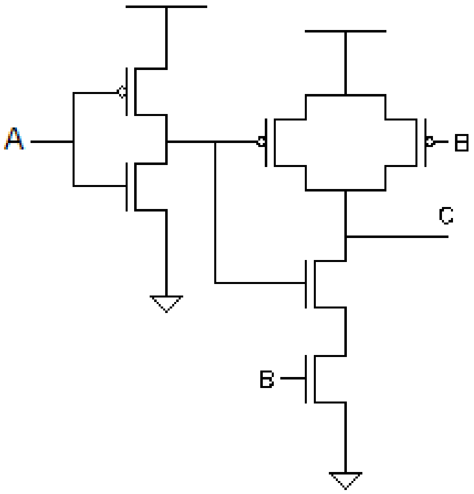
A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0





Problem 3 (3 points)

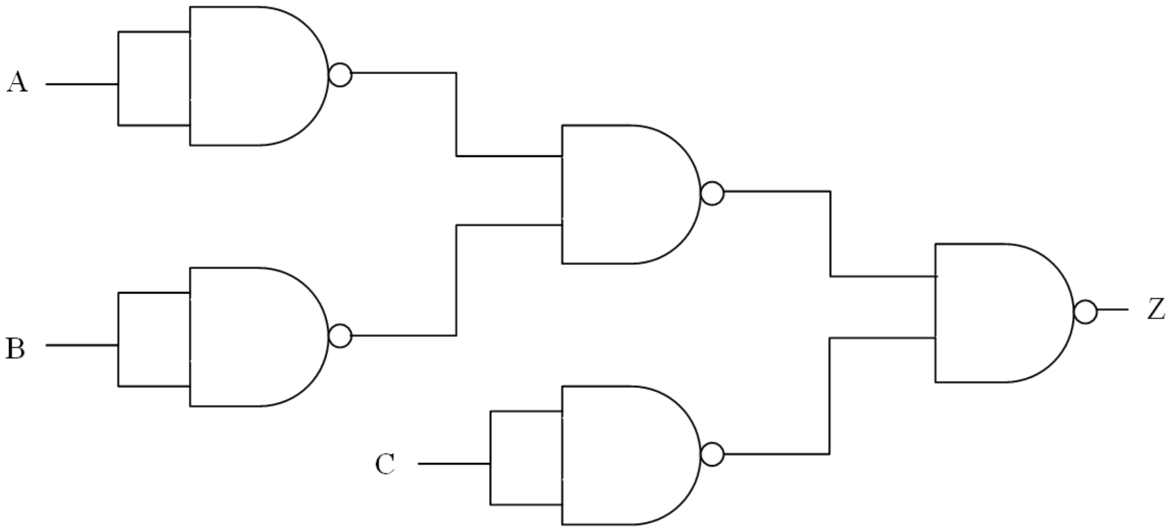
Complete the truth table for the following transistor level circuit:



A	B	C
0	0	1
0	1	0
1	0	1
1	1	1

Problem 4 (3 points)

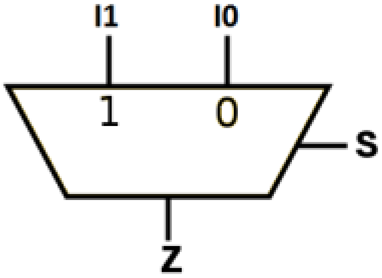
Given the logic equation Z = (NOT(A OR B)) OR C
Draw the gate-level circuit for Z using only 2-input NAND gates (Hint: DeMorgan's Law).



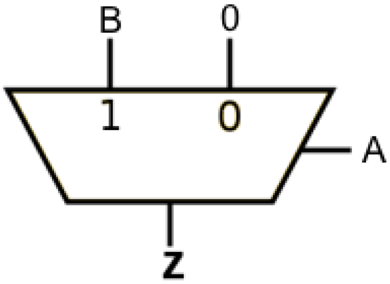
Problem 5 (4 points)

Implement the following truth table using a 2:1 MUX block.

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1



2:1 MUX BLOCK



Problem 6 (4 points)

Suppose a 64-bit instruction takes the following format:

OPCODE	SR	DR	IMM

If there are 201 opcodes and 64 registers,

a) What is the minimum number of bits required to represent the OPCODE?

201 Opcodes < 256 = 2^8 8 bits opcode

b) What is the minimum number of bits required to represent the SR register?

64 registers = 2^6 6 bits SR register

c) What is the maximum number of bits that can be used to represent the immediate field (IMM)?

64 - 8 - 6 - 6 = 44 44 bits IMM

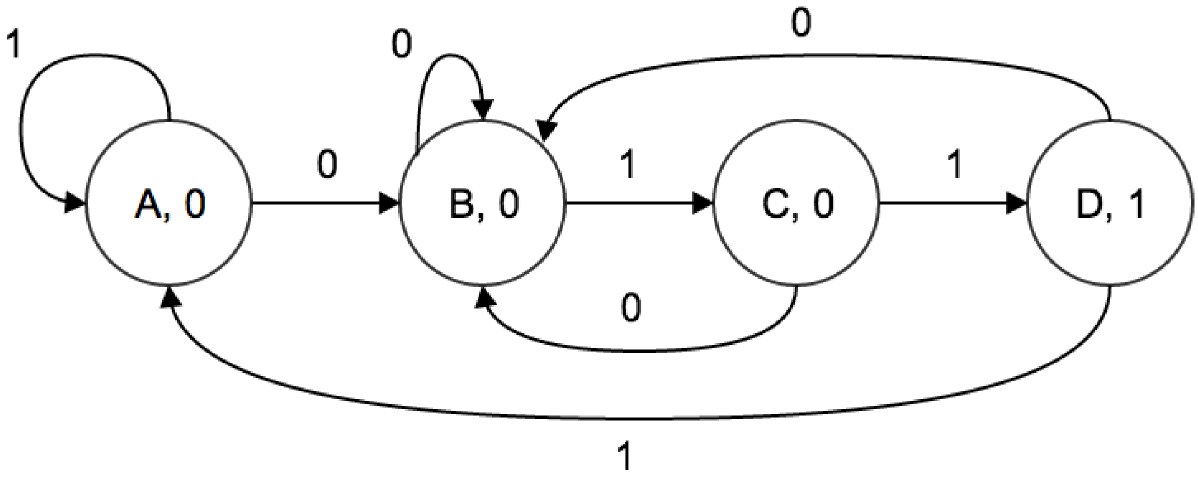
d. If the immediate (IMM) uses one's complement representation, what is the smallest number that can be represented in the IMM field?

- (2^43 - 1)

Problem 7 (4 points)

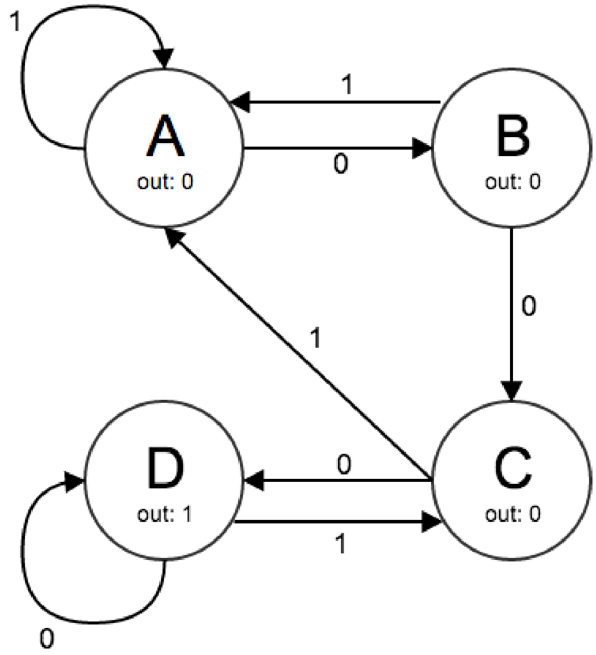
Draw a finite state machine for recognizing the bit sequence "**011**". The machine takes one input every clock cycle which can be 1 or 0. The machine outputs a '1' when the sequence **011** is recognized; otherwise it outputs a '0'.

Sample Input	0111101011
Sample Output	0010000001



Problem 8 (2 points)

Consider the finite state machine drawn below. State A has output 0, state B has output 0, state C has output 0, and state D has output 1.



Fill out the next state column in the table below for this state machine.

Current State	Input	Next State
A	0	B
A	1	A
B	0	C
B	1	A
C	0	D
C	1	A
D	0	D
D	1	C

Problem 9 (3 points)

1. Which of the following consists of all of the structures needed to manage the processing that is carried out by the computer?
    a. the control unit
    b. the processing unit
    c. memory
    d. input/output
2. How many registers does the processing unit of the LC-3 have?
    a. 4
    b. 6
    c. 8
    d. 16
3. In the instruction cycle, what does the "evaluate address" phase do?
    a. obtains the source operands needed to process the instruction.
    b. carries out the execution of the instruction.
    c. examines the instruction in order to figure out what the microarchitecture is being asked to do.
    d. computes the address of the memory location that is needed to process the instruction.