HW4 Solutions (CS552 Spring 2013)

Problem 4

```
xor   $1, $2, $3
and   $4, $5, $6
sub   $7, $4, $5
add   $5, $1, $5
sw    $4, 100($7)
or    $4, $7, $4
```

There are 10 total dependencies, 6 of which are true.

True Dependencies (Read After Write):
1. xor$1 -> add$1
2. and$4 -> sub$4
3. and$4 -> sw$4
4. sub$7 -> sw$7
5. and$4 -> or$4
6. sub$7 -> or$7

Anti Dependencies (Write After Read):
7. sub$5 -> add$5
8. sub$4 -> or$4
8. and -> add
9. sw -> or

Output Dependency (Write After Write):
10. and$4 -> or$4

In the pipeline of Figure 4.41 (page 355 of COD4e), only dependencies 2 and 4 result in hazards. Dependencies 1 and 3 would normally result in a hazard but are already resolved by previous stalls.

Note: Since, we are considering the pipeline in Page 355, the result of previous instruction is available only at the end of WB stage.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
xor $1, $2, $3	IF	ID	EX	M	WB										
and $4, $5, $6		IF	ID	EX	M	WB									
sub $7, $4, $5			IF	ID*	ID*	ID*	ID*	EX	M	WB					

add $5, $1, $5				IF	IF*	IF*	IF*	ID	EX	M	WB				
sw $4, 100($7)					*`	*	*	IF	ID	ID*	ID*	EX	M	WB	
or $4, $7, $4									IF	ID	ID*	ID*	EX	M	WB

For the pipeline with forwarding (Figure 4.60 on page 375 of COD4e), all hazards are eliminated and 5 cycles are saved.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
xor $1, $2, $3	IF	ID	EX	M	WB										
and $4, $5, $6		IF	ID	EX	M	WB									
sub $7, $4, $5			IF	ID	EX	M	WB								
add $5, $1, $5				IF	ID	EX	M	WB							
sw $4, 100($7)					IF	ID	EX	M	WB						
or $4, $7, $4						IF	ID	EX	M	WB					

Problem 5

a)

Instructions involved	Register Involved	Type of data dependency
I1 & I2	$3	True(RAW)
I1 & I4	$3	True(RAW)
I2 & I3	$5	True(RAW)
I2 & I4	$5	Output(WAW)
I1 & I3	$6	Anti(WAR)
I3 & I4	$6	True(RAW)
I3 & I4	$5	Anti(WAR)

b)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
add $3,$4,$6	IF	ID	EX	M	WB										
sub $5,$3,$2				IF	ID	EX	M	WB							
lw $6,100($5)							IF	ID	EX	M	WB				
add $5,$6,$3										IF	ID	EX	M	WB	

c)

Instruction No.	**Register Involved**	**Forwarding pipeline register**	**No of stalled cycles with forwarding**
I1 & I2	$3	EX/MEM	0
I2 & I3	$5	EX/MEM	0
I3 & I4	$6	MEM /WB	1

Problem 6

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
lw $s1,8($s0)	IF	ID	EX	M	WB										
sub $s0,$s1,$S2		IF	ID	ID*	EX	M	WB								
add $s0,$s0,$s1				IF	ID	EX	M	WB							
Check if Forward(F) or stall(S)			S		F	F									

Problem 7

On branch not taken:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
beq	IF	ID	EX	M	WB										
add		*	*	*	IF	ID	EX	M	WB						

sub						IF	ID	EX	M	WB					
or							IF	ID	EX	M	WB				
add								IF	ID	ID*	ID*	EX	M	WB	

On branch taken:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
beq	IF	ID	EX	M	WB										
add		*	*	*	IF	ID	EX	M	WB						

Problem 8

A stall and flush can occur at the same time. This results in both cooperating and conflicting actions. Recall that a flush will turn all pipe stages into a nop and load the PC with a new value, while a stall will maintain the state of pipe stages prior to the stalling stage, turn the stage following into a nop, and keep the PC unchanged. The cooperating nop actions need no further attention, however an arbitration mechanism for dealing with conflicting actions must be implemented. The flush actions should take priority because it's action removes the hazard that causes the stall. To make sure this works correctly, the hazard detection unit that decides on a stall should take the flush signal into account.

Problem 9

s1 != s2 – So, branches to Label

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
bne $s1,$s2,LABEL	IF	ID	EX	M	WB										
add $t2,$t1,$s1 - (Flushed)		~~IF~~													
sw $t2,4($s1)															
j EXIT															
LABEL: lw $s1,4($s6)			IF	ID	EX	M	WB								
EXIT: addi $s1,$s1,4				*	IF	ID	EX	M	WB						

Problem 10

a) Always Not taken = 6/15 = 40%

b) '1' BIT PREDICTOR

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Trace	T	T	N	T	T	T	N	T	N	T	T	N	N	N	T
Predict	T	T	T	N	T	T	T	N	T	N	T	T	N	N	N
Outcome	1	1	0	0	1	1	0	0	0	0	1	0	1	1	0

Prediction accuracy for 1 bit predictor = 7/15 = 46.67%

c) '2' BIT PREDICTOR

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Trace	T	T	N	T	T	T	N	T	N	T	T	N	N	N	T
Predict	T	T	T	T	T	T	T	T	T	T	T	T	T	N	N
Outcome	1	1	0	1	1	1	0	1	0	1	1	0	0	1	0

Prediction accuracy for 1 bit predictor = 9/15 = 60% **Problem 11**

Same as midterm exam problem

	Cycle																			
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
add $1, $2, $3	F	D	X	M	W															
sub $4, $2, $5		F	D	D	D	X	M	W												
or $6, $1, $4			F	F	F	D	X	M	W											
and $7, $9, $8						F	D	D	X	M	W									
lw $9, 4($7)							F	F	D	D	D	X	M	W						
lw $1, 16($9)									F	F	F	D	D	D	X	M	W			
sw $1, 4($7)												F	F	F	D	D	D	X	M	W

Problem 12

- Assembly instructions problem