U. Wisconsin CS/ECE 552
Introduction to Computer Architecture

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Miscellaneous (5.5, 5.7, 5.6, & 6.8)
www.cs.wisc.edu/~karu/courses/cs552

Slides combined and enhanced by Karu Sankaralingam from work by Falsafi, Hill, Marculescu, Nagle, Patterson, Roth, Rutenbar, Schmidt, Shen, Sohi, Sorin, Thottethodi, Vijaykumar, & Wood
Outline

• Multicycle Design (5.5)

• Implementing Control & Microprogramming (5.7)

• Exceptions (5.6)

• Exceptions in a Pipeline (6.8)
Multicycle Approach (No Pipelining)

- Break up the instructions into steps, each step takes a cycle
  - balance the amount of work to be done
  - restrict each cycle to use only one major functional unit
- At the end of a cycle
  - store values for use in later cycles
  - introduce additional “internal” registers
Multicycle Approach

• We will be reusing functional units
  - ALU used to compute address and to increment PC
  - Memory used for instruction and data
• Our control signals will not be determined solely by instruction
  - e.g., what should the ALU do for a “subtract” instruction?
• We’ll use a finite state machine for control
### What Instructions Need to Do

<table>
<thead>
<tr>
<th>Step name</th>
<th>Action for R-type instructions</th>
<th>Action for memory-reference instructions</th>
<th>Action for branches</th>
<th>Action for jumps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction fetch</td>
<td>IR = Memory[PC]</td>
<td>PC = PC + 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instruction decode/register fetch</td>
<td></td>
<td>A = Reg [IR[25-21]]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>B = Reg [IR[20-16]]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ALUOut = PC + (sign-extend (IR[15-0]) &lt;&lt; 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Execution, address computation, branch/jump completion</td>
<td>ALUOut = A op B</td>
<td>ALUOut = A + sign-extend (IR[15-0])</td>
<td>if (A ==B) then PC = ALUOut</td>
<td>PC = PC [31-28] II (IR[25-0] &lt;&lt; 2)</td>
</tr>
<tr>
<td>Memory access or R-type completion</td>
<td>Reg [IR[15-11]] = ALUOut</td>
<td>Load: MDR = Memory[ALUOut] or Store: Memory [ALUOut] = B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory read completion</td>
<td></td>
<td>Load: Reg[IR[20-16]] = MDR</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
FSM view of Control

IR <= MEM[PC]  “instruction fetch”

A <= R[rs]  B <= R[rt]  “decode / operand fetch”

R[rd] <= S  PC <= PC + 4

R[rt] <= S  PC <= PC + 4

S <= A fun B

S <= A or ZX

S <= A + SX

S <= A + SX

M <= MEM[S]

MEM[S] <= B

PC <= PC + 4

PC <= PC + 4

PC <= PC + 4

PC <= PC + 4

(PC <= PC + SX || 00)

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(6)
Multicycle Datapath

- Minimizes Hardware: 1 memory, 1 adder

**Ideal Memory**
- WrAdr
- Din
- Dout
- MemWr
- IRWr
- RegDst
- RegWr
- ALUOp
- Control

**Instruction Reg**
- PCWr
- IRWr
- RegDst
- RegWr
- ALUSelA
- ALUSelB

**Reg File**
- Ra
- Rb
- Rw
- busA
- busW
- busB

**ALU**
- ALU Out
- ALUOp
- ALUSelA
- ALUSelB

**ALU Control**
- Zero
- Target

**Mux**
- 0
- 1

**ExtOp**
- ExtOp

**MemtoReg**
- MemtoReg

**Zero**
- Zero
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Implementing the Control

- Value of control signals is dependent upon:
  - what instruction is being executed
  - which step is being performed

- Use the information we’ve accumulated to specify a finite state machine
  - specify the finite state machine graphically, or
  - use microprogramming

- Implementation can be derived from specification
Finite State Machine for Multicycle Control

- Implementation
- State bits
  - D-flipflops
- Control Logic
  - Comb. Block
  - Use PLA or ROM
Alternative: Microprogramming

- Sequence of RTL steps
  - program using microinstructions
Macroinstruction interpretation

User program plus Data

this can change!

one of these is mapped into one of these

AND microsequence

e.g., Fetch Calc Operand Addr
Fetch Operand(s)
Calculate
Save Answer(s)
Microprogramming

- A specification methodology (alternate to FSM)
  - appropriate if hundreds of opcodes, modes, cycles, etc.
  - signals specified symbolically using microinstructions
  - Microassembler?
Microprogramming Pros and Cons

- Ease of design
- Flexibility
  - Easy to adapt to changes in organization, timing, technology
  - Can make changes late in design cycle, or even in the field
- Can implement very powerful instruction sets (just more control memory)
- Generality
  - Can implement multiple instruction sets on same machine.
  - Can tailor instruction set to application.
- Compatibility
  - Many organizations, same instruction set
- Costly to implement
- Slow
Next time: memory
Control: Summary

Control is the hard part

Initial Representation
- Finite State Diagram
- Microprogram

Sequencing Control
- Explicit Next State Function
- Microprogram counter + Dispatch ROMs

Logic Representation
- Logic Equations
- Truth Tables

Implementation Technique
- PLA
- ROM

Technique
- “hardwired control”
- “microprogrammed control”
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Exceptions

• Exception = unprogrammed control transfer
  - system takes action to handle the exception
    • must record the address of the offending instruction
  - returns control to user
  - must save & restore user state
• Allows construction of a “user virtual machine”

normal control flow:
  sequential, jumps, branches, calls, returns
Interrupt, Exception, Trap?

• Interrupts
  - caused by external events
  - asynchronous to program execution
  - may be handled between instructions
  - simply suspend and resume user program

• Traps
  - caused by internal events
    • exceptional conditions (overflow)
    • errors (parity)
    • faults (non-resident page)
  - synchronous to program execution
  - condition must be remedied by the handler
  - instruction may be retried or simulated and program continued or program may be aborted

• MIPS convention:
  - External: Interrupts
  - Internal: Exception
Exception Semantics

- MIPS architecture defines the instruction as having no effect if the instruction causes an exception.
- When get to virtual memory we will see that certain classes of exceptions must prevent the instruction from changing the machine state.
- This aspect of handling exceptions becomes complex and potentially limits performance => why it is hard
  - Precise interrupts vs Imprecise interrupts
MIPS Exceptions

• All exceptions jump to same handler code
  - “Cause” register
• We consider
  - Illegal instructions
  - Arithmetic overflows
• Handler behavior
  - Save PC of offending instruction (How? PC+4 has already been written to PC)
  - Use special register EPC (why not use $31 like jal?)
  - Set cause register appropriately (0=ILL; 1=OVF)
  - Jump to handler at fixed address
Control FSM

IR <= MEM[PC]
PC <= PC + 4

A <= R[rs]
B <= R[rt]
S <= PC + SX || 00

S <= A fun B
R[rd] <= S

SW

S <= A + SX
LW

S <= A fun B
SW

M <= MEM[S]
R[rt] <= M
MEM[S] <= B

EPC <= PC - 4
PC <= exp_addr
cause <= 0

If (A=B)
PC <= S

EPC <= PC - 4
PC <= exp_addr
cause <= 1

overflow

overflow

undefined instruction
Other issues

- Vectored exceptions
  - “cause” folded into handler address
  - Different causes jump to different handlers
- User vs kernel mode
- Software issues
  - Disabling exceptions in handler
- Returning from interrupt
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Exceptions

• Semantics
  - No instruction after the exception causing instruction may execute
  - Every instruction preceding the exception causing instruction must complete execution
  - Set cause register
  - Jump to exception handler address
• Multiple instructions (exceptions) in a cycle!
Datapath modifications

- Pipeline complications
- What stage is exception detected?
  - Overflow?
    - In EX stage, also squash (convert to nop) EX stage
  - Illegal Instruction?
    - In ID stage, squash (convert to nop) ID stage
    - Similar to RAW hazard
  - What about external interrupts?
- Overflow in instruction i, illegal instruction in instruction i+1
  - Simultaneous exceptions
  - Hardware sorting
Walkthrough (1 of 2)

lw $16, 50($7)    
slt $15, $6, $7    
add $1, $2, $1    
or $13, ...      
and $12, ...

Clock 5

• All three instructions converted to nop

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Walkthrough (2 of 2)

sw $25, 1000($0)  bubble (nop)  bubble  bubble  or $13, ...

Clock 6

• Fetch next instruction from handler PC (MIPS)

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Pipelined Processor

- Phew!

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