

Cache Parameters

	L1-cache	L2-cache
Block size	16-64 bytes	64-128 bytes
Total size (kb)	16-64	256-4096
Hit time	1-3 cycles	7-25 cycles
Miss penalty	7-25 cycles	100-1000 cycles
Miss rate	2% to 5%	0.1% to 2%

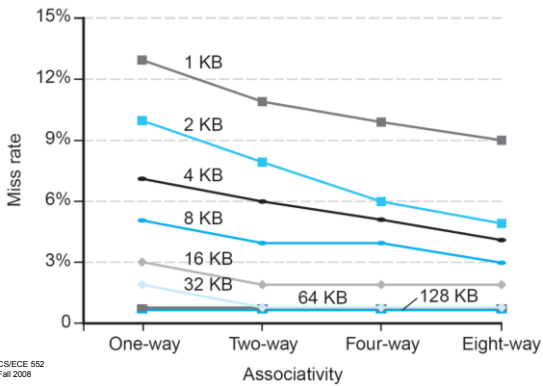
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Cache sizes

Processor	L1-cache	L2 (7 to 14 cycles latency)
Pentium M	32KB, 8-way, 3-cycles	2MB 8-way
PentiumIII	16KB, 4-way, 2 cycles	256 KB, 8-way
Pentium 4	8KB, 4-way, 2 cycles	256KB, 8-way
Core 2	32 KB, 8-way, 3 cycles	4MB, 16-way (@65nm) 16MB, 24-way (@45nm)

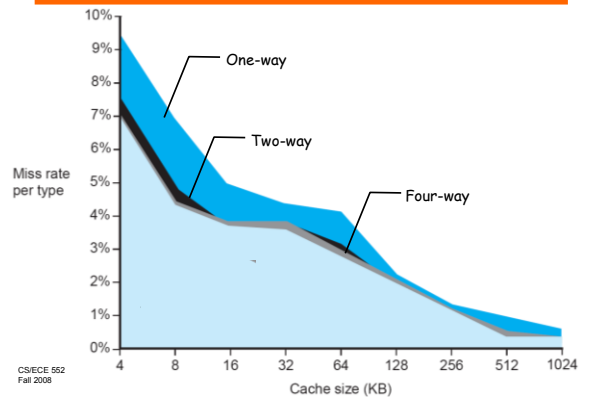
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Cache Performance (1)



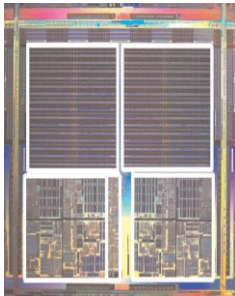
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Cache Performance (2)



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UltraSPARC IV+

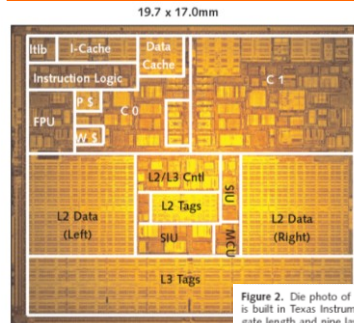


Figure 2. Die photo of the UltraSPARC IV+. The dual-core processor is built in Texas Instruments' 90nm bulk process, which has a 37nm gate length and nine layers of metal. The processor is built with 295 million transistors. Still, the die is 5% smaller than that of the U5 IV. The initial chips will be available at 1.8GHz and 1.65GHz, with a 2+GHz part coming later. The power is only 90W at 1.8GHz (1.1V), helped by using aggressive, dynamic power-management features. Sun had first silicon in 1H04.

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Itanium 2

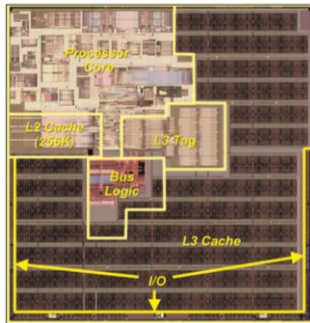


Figure 4. The Madison/9M version of the Itanium 2 is shown in the die photo. The integrated 9MB L3 cache can clearly be seen wrapping around on the right side and bottom of the die.

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