CS/ECE 552: Introduction to Computer Architecture
Department of Computer Sciences
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Mid-term Examination
In-Class
March 10, 2011
Approximate Weight: 25%

1 hour 15 minutes

CLOSED BOOK. You can bring one-cheat sheet (8.5 x 11 page).

Exam is **one-sided, total of 9 numbered pages**. Plan your time carefully.
One blank page included in the end for rough work. Also use left-side blank pages for rough work.

NAME: _____

Email: _____

Problem number	Maximum points	Actual points
1	8	
2	8	
3	8	
4	10	
5	17	
6	10	
7	25	
8	4	
Total	**90**	

Problem 1 (8 points)

Consider a workload with 15% stores, 15% loads, 15% branches, and 55% other integer instructions.
Consider two machines BASE and NEW.
On BASE, let stores take *1 cycle*, loads *2 cycles*, branches 3 cycles, and others 1 cycle.
On NEW, let stores take *2 cycles*, loads *1 cycle*, branches 3 cycles, and others 1 cycle.
In this case, the speedup of NEW with respect to BASE is S. **Write an expression for S.**

Problem 2 (8 points)
What are structural hazards, data hazards, and control hazards?

Problem 3 (8 points)
Define the performance metric MIPS and explain why it is not a good metric for comparing two different machines

Problem 4: (10 points)
Assume we make an enhancement to a computer so that some mode of execution is improved by a factor of 4.

a) Under what circumstances will overall program speedup be 2?
b) If the enhanced mode contributes to 50% of the time (and this 50% is percentage of the total execution time when the enhanced mode is used), what is the overall speedup? What percentage of the original execution time is converted to the faster mode?

Problem 5: (12 points)

Part A: Most compiler writers wish the MIPS architecture had 64 or even 128 registers. Assume we want to design a new MIPS-2005 architecture with 64 registers, but preserve the general structure of the instruction formats (but not the sizes of all the fields). What might the MIPS-2005 instruction formats look like? Show the 3 instruction formats and how the size of the fields changes.

Part B (5 points):

What are the most significant changes in what the new MIPS-2005 ISA can express?

Problem 6 (10 points)
Consider an implementation of the MIPS instruction set which uses a pipelined datapath. Cycle time is 250ps. The machine has a CPI of 1.0 in the absence of control and data hazards. However, taken branch instructions incur 3 stall cycles (bubble) and **loads followed by a dependent instruction incur 2 stall cycle (bubble)**.

For the two workloads below, assume that **60% of branches are taken** and **50% of loads are followed by a dependent instruction**. Compute the CPI for the pipelined datapath. Show your work.

Worload	% branches	% loads	%stores	% other	CPI
W1	15	20	30	35	
W2	10	30	10	40	

Problem 7: (25 points)

High performance datapaths use bypass paths (also known as data forwarding logic) to reduce pipeline stalls. However, bypass paths are relatively expensive, especially in some wire constrained technologies. To reduce the cost (and potential cycle time impact), some architects have explored omitting some of the possible bypass paths. Consider the datapath illustrated above (note that the PC update logic and all control logic is intentionally omitted). This pipelined datapath is similar to the one in the book, *but only has bypass paths on one side of the ALU.* Assume that the register file internally bypasses the value, so that if register $i is read and written in the same cycle, then the read returns the new value. Assume that the control logic bypasses the data as soon as possible using the given forwarding data paths, and stalls in decode otherwise. You may NOT add additional data paths.

In this problem, you will look at how a program snippet performs on this pipeline. Recall that R-format instructions have the form:

```
opcode rd, rs, rt
```

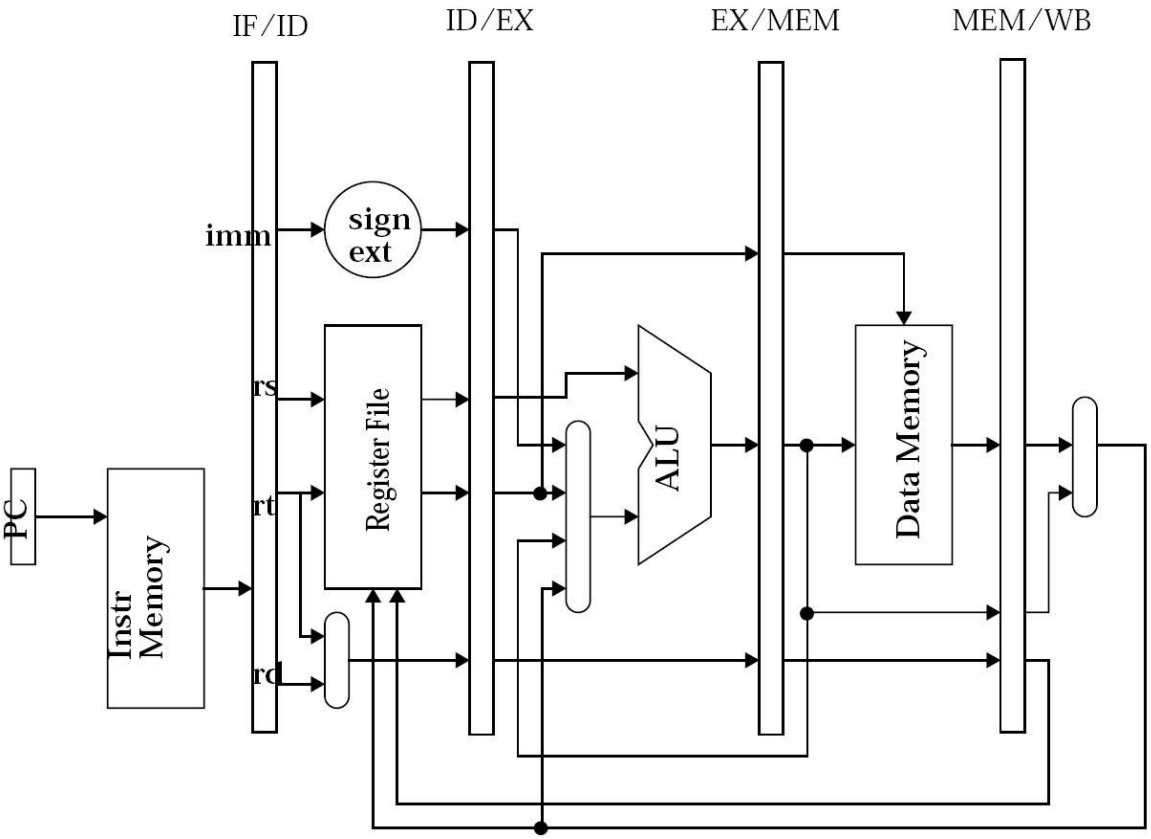
and I-format instructions have the form

```
opcode rt, imm(rs)
```

or

```
opcode rt, rs, imm
```

Use the table on the next page to show how the given instruction sequence flows through the pipeline and where stalls are necessary to resolve hazards.



	Cycle																			
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
add $1, $2, $3	F	D	X	M	W															
sub $4, $2, $5		F	D																	
or $6, $1, $4																				
and $7, $9, $8																				
lw $9, 4($7)																				
lw $1, 16($9)																				
sw $1, 4($7)																				

Consider the code and pipeline above. Show the execution of this code on the pipeline above.
Use the letters, F, D, X, M, and W.

For each cycle where a stall occurs explain why.

Problem 8: (4 points)

Consider a processor with only one memory which is used for both instructions and data, and this memory has only one port to it. Consider a 5-stage pipeline that we have been using. **For this problem use the conventional datapath we have discussed in class which allows forward of both operands and from the Mem stage and WB stage.** Write out a detailed pipeline diagram with the stalls as in the previous problem's table for the instruction sequence below:

	Cycle																			
Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ld $1, 4($3)	F	D	X	M	W															
sub $4, $1, $5		F	D																	
ld $6, 8($9)																				
and $7, $9, $8																				
add $1, $3, $4																				

Consider the code and pipeline above. Show the execution of this code on the pipeline above.
Use the letters, F, D, X, M, and W.

For each cycle where a stall occurs explain why.

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