Lecture 9: Speculation Recovery and Memory Disambiguation

- **Last Time**
  - More sophisticated branch prediction algorithms

- **Today**
  - Yeh and Patt paper
  - Branch target prediction
  - Speculation recovery
  - Speculation recovery (reorder buffer)
  - Memory disambiguation
  - Microprocessor case studies
    - Alpha 21264, Pentium 4

Slides courtesy of Stephen W. Keckler, UT-Austin

Control Speculation

- **Fetch**: use branch prediction to keep instruction window full
- **Issue**: out-of-order
  - Non-speculative and speculative instructions in pipe
  - Speculative instructions can complete *before* non-speculative ones
  - Mix and match instructions across multiple basic blocks
- **Problem**: What happens if the branch prediction was wrong!
Speculation Recovery

- Another use of the reorder buffer
  - Execute instructions out-of-order
  - Maintain instruction in-order in reorder buffer
  - Commit instructions in order
  - If branch is mis-predicted
    - Invalidate all reorder buffer entries after branch
      - (effectively flushing the pipeline)
    - Begin fetching at correct target
- Misprediction penalty can be effectively quite large
  - Consider the opportunity cost
  - i.e. 10 cycles at 4 instructions per cycle is 40 issue slots wasted!

Retirement and Re-order Buffers

- Must commit instructions in order
  - check exceptions
  - update visible register state
  - update memory
- Maintain slots as a circular buffer
  - commit instruction at head when it is finished
  - fetch new instructions to tail
Tomasulo’s algorithm

… with ROB
Dynamic scheduling

- RAW/WAW/WAR faults
  - Register renaming
  - Additional physical registers

- LW R9, 0(R10)
  ADD R10,R1,R2
  SW R4,0(R3)
  LW R5,0(R6)
  ADD R7,R5,R8

- Any other problems?
  - What about memory

Dynamic Scheduling and Memory Operations

- Reordering memory instructions
  - LD/LD is OK
  - LD/ST could cause RAW or WAR hazard
  - ST/ST could case WAW hazard

- Danger only if instructions use the same address!

- Basic idea
  - Keep track of addresses for memory instructions
    - Allow LD to issue early
    - Defer ST to memory until instruction commits

- LD can get data from store buffer too!
OOO Processing

- Dynamic scheduling
- Register renaming
- Branch prediction
- Speculation recovery
- Memory disambiguation

Alpha 21264 Pipeline (1)
Alpha 21264 Pipeline (2)

Alpha 21264 Pipeline (3)
Alpha 21264 Pipeline (4)

Pentium4 Pipeline
Branch prediction

CPI analysis
Clock speed vs. Performance

Summary

• Speculation recovery
• 21264 microarchitecture
  - Control speculation
  - Data speculation
  - Latency speculation
  - Recovery
• Pentium4 pipeline

• Next Time
  - ILP limits and beyond
  - Seznec paper and Yaeger paper